technical manual

ELDORADO

ELDORADO ELECTRODATA CORPORATION
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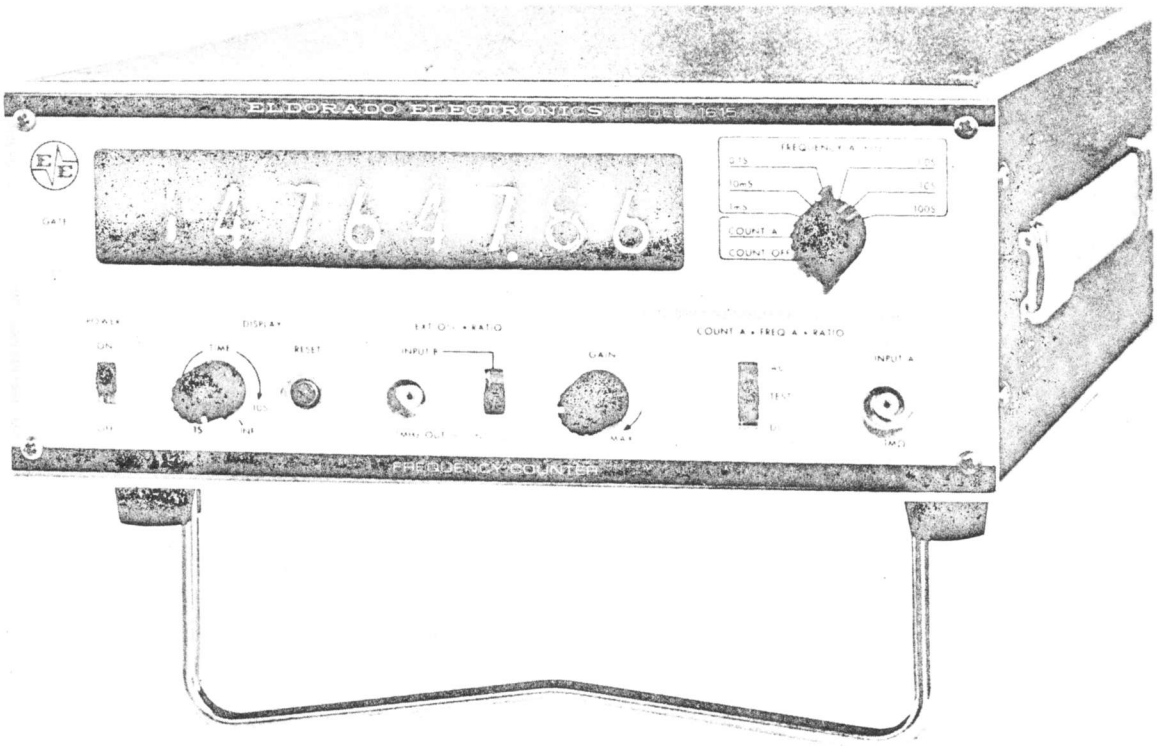
M3171-134109

TECHNICAL MANUAL

MODEL 1615

FREQUENCY COUNTER



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ADDENDUM
OPTION K

Option K provides increased sensitivity and is further broken down into five catagories. Option K, K1, K2, K3 and K4. The following table defines the characteristics of each option.

OPTION K
MODEL 1605, 1607
Sensitivity: 5 mV rms
Range: DC - 100 kHz
Channel: A
Overload: 1V rms
Maximum Input: +2V rms
Input Impedance: 50kΩ
Controls: Switch selectable, rear panel.

*OPTION K2
MODEL 1615, 1650
Sensitivity: 50 mV rms
Range: 1 kHz - 200 MHz
Channel: A
Overload: 300 mV rms
Maximum Input: 2.2V rms (+20 dBm)
Input Impedance: 50Ω
Controls: Automatic

*OPTION K4
MODEL 1650
Sensitivity: 10 mV rms
Range: 25 MHz - 500 MHz
Channel: C
Overload: 250 mV rms
Maximum Input: 2.2V rms (+20 dBm)
Input Impedance: 50Ω
Controls: Automatic

OPTION K1
MODEL 1615, 1650
Sensitivity: 35-50 mV rms
Range: 20 Hz - 136 MHz
(136 MHz - 200 MHz 100 mV rms)
Channel: A
Overload: 10V rms 20 Hz - 500 Hz
5V rms 500 Hz - 200 MHz
Maximum Input: 20 Hz - 500 Hz, 100V rms
500 Hz - 200 MHz, 10V rms
Input Impedance: 1MΩ
Controls: Sensitivity control, front panel.
Visual Display: May cause a 1 to appear in the least significant digit with no input signal applied.

*OPTION K3
MODEL 1615, 1650
Sensitivity: 10 mV rms
Range: 1 kHz - 200 MHz
Channel: A
Overload: 300 mV rms
Maximum Input: 2.2V rms (+20 dBm)
Input Impedance: 50Ω
Controls: Automatic

* Options K2, K3 and K4 are exclusive, however both Option K1 and K4 may be installed in one instrument.

K = Standard Eldorado amplifier, see schematic in manual.

K1 = Standard Eldorado amplifier, modified to specified frequency, see schematic in manual.

K2 = Contains 1 each UA-105 Avantek High Gain Amplifier.

K3 = Contains 1 each UA-105 and 1 each UA-106 Avantek High Gain Amplifiers.

K4 = Contains 1 each UA-105 and 1 each UA-106 Avantek High Gain Amplifiers

When K2, K3 or K4 are installed, input levels to ≤300 mV for K2 and K3 or 250 mV for K4, are accepted. Inputs >400 mV for K2 and K3 and 300 mV for K4, applied to the Avantek amplifier may cause frequency doubling resulting in erroneous readings. If the input signal exceeds 250 and/or 300 mV some method of attenuation should be used.

When Option K1 is supplied, a 1 in the first digit (LSD) may be present when no frequency is applied.

ERRATA

MODELS 1615 - 1650

Table of Options pages 1-5 and 1-6 Model 1615 and pages 1-6 and 1-7 Model 1650.

Change Option P1 and P2 Reset Inhibit as follows:

Reset Inhibit: +1V @ 1KΩ maximum source resistance to +30V @ 30KΩ maximum source resistance to prevent automatic reset until data recording equipment has completed its recording cycle. Release level; -5V to -30V or open circuit (>20KΩ).

Table 2-2 and 2-3 pages 2-4 and 2-5 Model 1615 and pages 2-5 and 2-6 Model 1650.

Change Note 6 as follows:

Reset Inhibit: Accepts an inhibit level of +1 volt if supplied from less than 1K ohm resistance or +6V to +20V from any source resistance.

Input A Schematic C-11-05403:

Delete L102 and L106 and replace with a jumper.

Delete CR109 and R114, bridge CR109 with a jumper to complete coupling from Q107 to Q108.

CR113 is an X component and can be either a 1N695 diode, a 10 ohm resistor or a short circuit.

Change C106 from 15 pF to 33 pF.

Change R102 from 102Ω to 82Ω.

MODEL 1650 ONLY

To improve the input sensitivity of the C channel to 100 mV across the band from 50 MHz to 500 MHz the following changes have been made to the 500 MHz Prescaler circuits.

500 MHz Prescaler Schematic D-11-05406

Change CR1 from FD700 to HPA2900

Change Q1 from 2N3137 to 2N3563

Change R3 from 56Ω to 430Ω 1/2 watt

Change R6 from 390Ω to 750Ω 1/2 watt

Change the Channel C Sensitivity Specification on Page 1-3 to 100 mV rms from 50 MHz to 500 MHz.

INITIAL TESTING OF UNHEATED CRYSTAL OSCILLATORS
(Non-Ovenized)

Extensive testing of the aging rates of the unheated type crystal oscillators has recently been completed. Based on this research, verification of the published aging rate can be accurately determined within a reduced time interval. The following procedure will validate the initial aging specifications.

1. Attach a thermometer or temperature sensing device to the crystal case.

2. Apply instrument power for a twenty four hour period.

3. Measure the crystal's external temperature to within 1° C.

4. Measure the crystal oscillator's frequency to within 1 part in 10^7 (0.1 Hz).

5. After one week's continuous operation again measure the crystal temperature and output frequency.

6. The two frequencies will be within 2 parts in 10^6 (2 Hz), taking into consideration a temperature coefficient of $\pm 0.5 \times 10^{-6}$/° C.

7. The above test confirms the published oscillator specifications.

FEDERAL COMMUNICATIONS COMMISSION SUPPLEMENT

SCOPE:

Measurement techniques for Eldorado FCC-type approved frequency monitoring devices in commercial AM and FM broadcast stations.

GENERAL:

The use of instrumentation approved by the FCC as frequency monitors for commercial AM and FM broadcast equipment in itself is not sufficient. Required in addition to type approval is the implementing of the proper measurement techniques to ensure accuracy of measurements as required by the FCC. Because of the wide variations in transmitting and receiving equipment as presently being used in the broadcast industry this supplement cannot discuss all of the possible variations in the application of this equipment as a frequency monitoring instrument. The following outline suggests generally accepted proper measurement techniques. It is assumed that technically competent users will be in operation of this equipment, therefore a detailed discussion of how and why a frequency counter works is not incorporated in this addendum. Technical information on this level is incorporated in the basic text of the associated technical manual.

SAMPLING POINTS AND CAUTIONS:

Frequency and test points are provided by the manufacturer of the transmitting or receiving equipment (refer to the equipment manual). A caution to be offered at this point is to ensure that (1) the input signal to the counter is of sufficient level as defined in the specifications section of this manual to allow accurate measurements and (2) a completely opposite consideration to observe is that this input level does not exceed the capabilities of the input circuitry of the frequency monitoring device. Harm to both personnel and equipment could result if a high level voltage or RF is applied. If high level voltage or RF radiation is present, an inductive pick up with a DC blocking capacitor is an accepted method of sampling the frequency. It is generally not advisable to DC couple the RF source to the frequency counter. Working in a low power oscillator section of a transmitter, a direct connection could load the circuit and inadvertently cause a frequency shift. The output from the frequency doubling or buffer stage is the recommended point to monitor the frequency. Normally sufficient signal is available at this stage to make accurate measurements and a buffer situation exists between the doubler and the primary oscillator. Under no circumstances should a

frequency monitoring device of this type be directly connected to the power amplifier output stage or at the base of the radiating antenna, unless proper safeguards are observed to block the high level voltages and RF energy. Frequency monitors should be connected to the sampler output from the appropriate stage of the transmitter. This monitoring point should be operating on the nominal channel frequency, rather than a submultiple of that frequency.

To prevent erroneous readings the input signals applied to the frequency counter must be of the carrier frequency only at a stage prior to injection of the modulating frequency. Since digital frequency counters count input events they cannot discriminate between CW inputs and MCW inputs. During the period the counter is gated on (gate time) all input signals are counted by the count circuits and ultimately displayed as the input frequency. If the input contains both the carrier frequency and the modulation frequency the counter will count the resultant signal (MCW) rather than the desired CW signal. Therefore, all carrier frequencies should be monitored with zero modulation or at a point prior to modulation injection.

WARM-UP REQUIREMENTS:

Before accurate measurements can be made both the RF source to be measured and the frequency monitor have to warm up and stabilize.

The warm up to stabilize time required by the RF source to be monitored will be detailed in that equipment manual. The Eldorado type-approved instruments require a warm up time of one hour from a cold start. If the Eldorado frequency counter has been allowed to remain plugged into active AC mains, even when the instrument has been turned off, the proportional crystal oven has maintained a stabilized temperature, thus allowing accurate measurements to be made within 20 minutes after initial turn on. Because of all solid state construction, it is acceptable to allow the frequency counter to remain on at all times.

CALIBRATION:

It is recommended that a 6 month scheduled calibration cycle be established to ensure stability and accuracy of readings as required by the FCC. The governing accuracy factor being the 1 MHz crystal controlled time base. This 1 MHz crystal oscillator should be checked against a frequency standard with a stability rating better than the oscillator stability supplied in this instrument (normally five to ten times more accurate).

warranty

Eldorado instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. The liability of Eldorado under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer and has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Eldorado shall have the right of final determination as to the existence and cause of a defect. In no event shall Eldorado be liable for collateral or consequential damages. In order to expedite the rapid turnaround of your unit, please obtain a Returned Material Authorization (RMA) number by contacting the Customer Service Department. In all correspondence or telephone calls, a model number and serial number is required. Address all correspondence to Customer Service Department, Eldorado Electrodata Corporation, 601 Chalomar Road, Concord, California 94520, Phone (415) 686-4200, TWX 910-481-9476.

The instrument should be shipped prepaid with the return form attached to the packing container. When the instrument is repaired it will be returned to you best way prepaid.

This warranty is in lieu of any other warranty, express, implied, or statutory, and no agreement extending or modifying it will be binding upon Eldorado unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Eldorado instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the instrument is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company. In any case where damage occurs in transit with the instrument in packing case, Eldorado's obligations under warranty are dependent on the customer's immediately notifying the carrier so that inspection can be made and a claim filed.

REPAIR SERVICE

Experienced service personnel and special test equipment are available at the factory to perform any necessary repairs. Every effort will be made to expedite the repair of instruments returned for servicing. Repair work will be performed only upon receipt of a written purchase order or authorization. Utilize the same procedure for returning an instrument for service as for warranty return. After receipt of the unit the Customer Service Department will issue a quotation of repair costs for your approval.

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This manual is packaged with instrument Serial Number _____.

This instrument is a Model 1615 Frequency Counter.

It contains options:

Option C
Option D
Option E
Option P1
Option P2
Option R6
Option Y2

Special Modification Number _____.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

MODELS 1615 - 1650

ERRATA

Input A Schematic C-11-05403:

Delete L102 and L106 and replace with a jumper.

Delete CR109 and R114, bridge CR109 with a jumper to complete coupling from Q107 to Q108.

CR113 is an X component and can be either a 1N695 diode, a 10 ohm resistor or a short circuit.

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MODEL 1650 ONLY

To improve the input sensitivity of the C channel to 100 mV across the band from 50 MHz to 500 MHz the following changes have been made to the 500 MHz Prescaler circuits.

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SECTION 1

INTRODUCTION and SPECIFICATIONS

CRYSTAL OSCILLATOR	STORED DISPLAY
INTEGRATED CIRCUITS	0.01 Hz RESOLUTION
HIGH INPUT IMPEDANCE	VARIABLE GAIN
LOW POWER	LIGHT WEIGHT

SELF TEST FUNCTION

This new general purpose counter uses integrated circuits extensively providing a light, compact, and rugged instrument package with low power consumption and high reliability. The Model 1615 will measure Frequency, Ratio and Totalize.

The 1615 has a maximum counting rate of 200 MHz. Gate times of 1 ms through 100 s provide resolution to 0.01 Hz. A bench mounted instrument, with well defined front panel mounted operating controls, can also be equipped for rack mount installation. The six decade digital display features stored display during the measurement cycle with the readout in kHz and an automatically positioned decimal point.

Optional features include a choice of three high stability oven controlled crystal oscillators for greater stability requirements. Two digital printout options compatible to vertually all recording devices. Expansion of the visual display to eight decades and the previously mentioned rack mounting kit.

SPECIFICATIONS

FUNCTIONS	Totalize - Frequency - Ratio

TOTALIZE MEASUREMENT

Input:	A channel.
Maximum Count Displayed:	999,999.
Maximum Counting Rate:	200 MHz.
Count A:	Count on function continuously counts inputs until count off.
Count Off:	Inhibits input.
Accuracy:	Absolute.
Self Test:	Counts internal 1 MHz clock pulses.

FREQUENCY

Input:	A channel.
Frequency Range:	20 Hz to 200 MHz.
Gate Times:	1 ms, 10 ms, 0.1 s, 1.0 s, 10 s, and 100 s.
Visual Display:	Reads in kHz with automatically positioned decimal point.
Accuracy:	± 1 count ± oscillator stability.
Self Test:	Measures 1 MHz internal oscillator frequencies.

RATIO A/B

Inputs:	A and B channels.
Frequency Range:	
A input:	20 Hz to 200 MHz.
B input:	10 Hz to 2 MHz.
Visual Display:	Indicates $\frac{A}{B}$ x the mode switch setting. 10^3 through 10^8 (1 ms - 100 s mode switch settings).
Accuracy:	± 1 count of input A ± trigger error of input B/multiplier.

INPUT CHARACTERISTICS

Channel A	Frequency and Ratio Numerator input.
Frequency Range:	20 Hz to 200 MHz.
Sensitivity:	100 mV rms for sinewave input. 0.3V peak for positive or negative inputs (4 ns minimum width).

INPUT CHARACTERISTICS

Channel A (continued)

Dynamic Range:	Typically >40 dB.
Maximum Operating Input:	100V rms.
Maximum Input Without Damage:	100V rms.
Coupling:	ac.
Impedance:	≃1 Megohm shunted by 20 pF.
Gain Control:	Variable control permits changing input sensitivity from 100 mV rms to 10V rms.
Connector:	Front panel mounted BNC.

Channel B: External Time Base input and Ratio denominator.

Frequency Range:	dc to 2 MHz.
Sensitivity:	1.0V rms for sinewave inputs, 3.0V peak for positive pulses (250 ns minimum width).
Maximum Operating Input:	5V rms.
Maximum Input Without Damage:	50V rms.
Coupling:	dc.
Impedance:	≃10kΩ.
Switch Selection:	Front panel slide switch must be in the Input B position.
Connector:	Front panel mounted BNC.

1 MHz OSCILLATOR STABILITY

Aging rate after 30 days operation:	$\pm 1 \times 10^{-6}$/month. $\pm 3 \times 10^{-8}$/day.
Temperature:	$\pm 2 \times 10^{-7}$/° C from 16° C to 32° C after 30 minutes operation.
	$\pm 2 \times 10^{-5}$ over 0° C to +55° C range.
Line Voltage:	$\pm 1 \times 10^{-6}$ for 10% change.
Signal Output:	1 MHz, ≃2V rms, 1kΩ source. Available at B input connector when switched to Int. Osc. position. When option C, D or E oscillators are installed output signal amplitude is ≃2V peak-to-peak.

EXTERNAL OSCILLATOR: Switch selectable. Front panel switch selects either use of the internal oscillator or use of an external oscillator. Signal applied to B Channel Input. See Channel B input characteristics.

Connector: Front panel mounted BNC.

RESET	
Automatic:	After display time.
Manual:	Front panel pushbutton.
VISUAL DISPLAY	
Numerical:	Six decades of in-line long life digital display indicators with automatically positioned decimal point. Readings are in kHz.
Gate:	Gate lamp indicates count gate open.
Display Time:	Continuously variable from less than 0.1 second to approximately 10 seconds independent of gate time. Display time control includes an infinite display time position.
Storage:	Display storage holds readings between samples.
POWER REQUIREMENTS	115Vac ±10%, 50-60 Hz or 230Vac ±10%, 50-60 Hz; selection of 230Vac provided by internal wiring change. Power, 42 watts.
ENVIRONMENTAL	
Operating:	0° C to +55° C.
Storage:	-55° C to +80° C.
MECHANICAL	
Dimensions:	3.5" x 8.4" x 11" (HxWxD) without bail.
	6" x 8.4" x 11" (HxWxD) with bail extended.
Weight:	Net 6 lbs. Shipping 12 lbs.
ACCESSORIES SUPPLIED	1 each 3 to 2 prong cord adapter.
	1 each Technical Manual.

TABLE OF OPTIONS

OPTION C: Internal 1 MHz crystal oscillator. Available only with 115Vac operation. Provides oscillator stability of:

Short Term: $\pm 7 \times 10^{-9}$ average per 10 second period.

Long Term: $\pm 3 \times 10^{-8}$ per week after 45 days operation.

Temperature: $\pm 5 \times 10^{-9}$/° C over temperature range of 0° C to +50° C.

Adds 14 watts to power consumption.

OPTION D: Internal 1 MHz crystal oscillator. Proportional oven. Provides oscillator stability of:

Short Term: $\pm 5 \times 10^{-11}$ rms for 1 second averaging.

Long Term: $\pm 2 \times 10^{-9}$ per day after 48 hours operation.

Temperature: $\pm 2 \times 10^{-10}$/° C average over temperature range from -5° C to +55° C.

Adds 2 watts to power consumption after warmup.

OPTION E: Internal 1 MHz crystal oscillator. Proportional oven. Provides oscillator stability of:

Short Term: $\pm 5 \times 10^{-11}$ rms for 1 second averaging.

Long Term: $\pm 1 \times 10^{-9}$ per day after 48 hours operation.

Temperature: $\pm 2 \times 10^{-10}$/° C average over temperature range from -5° C to +55° C.

Adds 2 watts to power consumption after warmup.

OPTION P1: Provides low level BCD output at rear panel connector. 1-2-4-8 positive true, positive zone logic: "0" = 0.2V nominal, 5 mA maximum current sinking; "1" =+3.6V unloaded 2 mA maximum source, when measured between appropriate data word pin and reference pin of the output connector.

Reset Inhibit: 0V @ 1kΩ maximum source resistance to +30V @ 30kΩ maximum source resistance to prevent automatic reset until data recording equipment has completed its recording cycle. Release level; -5V to -30V or open circuit (>20kΩ).

Print Command: Negative 12V step when measured between print command pin and reference pin of the output connector.

Connector: Amphenol 50 pin #57-40500.

OPTION P2: Provides high level BCD output at the rear panel connector. 1-2-4-8 positive true negative zone logic: "0" = -12V nominal 22kΩ maximum source resistance; "1" = -0.2V nominal 5 mA maximum sink when measured between appropriate data word pin and reference pin of the output connector.

Reset Inhibit: 0V @ 1kΩ maximum source resistance to +30V @ 30kΩ maximum source resistance to prevent automatic reset until data recording equipment has completed its recording cycle. Release level; -5V to -30V or open circuit (>20kΩ).

Print Command: Negative 12V step when measured between print command pin and reference pin of the output connector.

Connector: Amphenol 50 pin #57-40500.

This option will provide drive to the following printers:

Beckman Model 1453; Clary Model 7000, with option II logic and standard print command; CMC Model 410A with logic 4a; Franklin Model 1200 with reverse logic; HP Model 562A with option 22 logic boards, one option 30 connector with Eldorado option P/D cable or one HP option 32 BCD input cable; HP Model 5050A with option 01 installed and option 31 input cable; and Monroe Model 10-40-M1-0-k.

OPTION R6: Provides rack mounting hardware for mounting in a 19" rack width.

OPTION Y2: Expands visual display to eight decades.

Accessory Cable Options for the above listed P2 Options.

Option P/A: For Beckman Model 1453 Printers.
One foot cable terminated at one end with an Amphenol 57-30500 and on the other end with a DPX-40 Cannon connector.

Option P/B: For Clary 7000, Franklin 1200, and Monroe 10-40 Printers.
Six foot cable terminated at one end with an Amphenol 57-30500 and open with tinned leads at the other end.

Option P/C: For CMC 410A Printers.
One foot cable terminated at one end with an Amphenol 57-30500 and with two Amphenol 57-40500 connectors at the other end.

Option P/D: For HP 562A Printers.
One foot cable terminated at one end with an Amphenol 57-30500 and with two Amphenol 57-40500 connectors at the other end.

Option P/E: For HP 5050A Printers.
One foot cable terminated at one end with an Amphenol 57-30500 and with two Amphenol 57-40500 connectors at the other end.

SECTION 2

INSTALLATION AND OPERATION

SECTION 2

INSTALLATION and OPERATION

2.1 GENERAL

This section described Incoming Inspection, Installation, and Operation of the Model 1615 Frequency Counter.

2.2 INCOMING INSPECTION

Prior to packaging for shipment, this instrument received extensive operational, alignment and calibration tests, and was in perfect working order.

Upon receipt a visual inspection for damage incurred in shipment, and an inventory of the package contents as listed on the packing slip should be made. If the instrument has been damaged, notify carrier immediately (see warranty).

2.2.1 Incoming Operational Check

The following procedure outlines an overall operational check of the instrument. No special test equipment or tools are needed.

a. Connect the instrument to the proper ac power source.

b. Place the Power ON/OFF Switch to the ON position.

c. Position the Display potentiometer at a minimum setting.

d. Place the oscillator selector switch to the internal oscillator position.

e. Place the "Test/Normal" Switch to the Test position.

f. Place the Mode Switch to the Count Off position.

g. Place the Mode Switch to the Count A position and observe the display. Count will accumulate.

h. Place the Mode Switch to the Frequency 1 ms position. Observe the display reads 001000.* or 00001000.* for eight digit instruments.

i. Place the Mode Switch to the Frequency 10 ms position. Observe the display reads 01000.0* or 0001000.0* for eight digit instruments.

j. Place the Mode Switch to the Frequency 0.1 s position. Observe the display reads 1000.00 or 001000.00 for eight digit instruments.

k. Place the Mode Switch to the Frequency 1.0 s position. Observe the display reads 01000.000*.

l. Place the Mode Switch to the Frequency 10 s position. Observe the display reads 1000.0000*.

m. Place the Mode Switch to the Frequency 100 s position. Observe the display reads 000.00000*.

n. This completes the operational check.

* ±1 count

2.3 INSTALLATION

The Model 1615 is shipped for bench mounting with a self locking elevating bail installed. Only connection to the ac power source and signal input cables are required for installation.

2.4 OPERATION

Operation after initial installation is by front panel controls and switches. A comp'ete description of each control is supplied in Table 2-1.

TABLE 2-1
MODEL 1615 FREQUENCY COUNTER
OPERATING CONTROLS

CONTROLS	FUNCTION
POWER	Power ON/OFF slide switch.
DISPLAY Two Controls	
Time	Display time potentiometer and switch. Varies display time from 0.1 second to 10 seconds, instrument is automatically reset at the end of display time. Also, in the full clockwise position switch is activated providing an infinite display time and inhibiting the automatic reset function.
Reset	Manual reset pushbutton. Overrides all controls and resets the instrument.
EXT OSC • RATIO	
Input B/1 MHz Out	BNC connector allows monitoring of the internal oscillator or injection of: an external reference 1 MHz oscillator or Ratio B channel inputs.
Input B/Int. Osc. Switch	Slide switch selects either use of the internal oscillator (BNC output = 1 MHz) or use of: an external oscillator or Ratio B inputs.
COUNT A • FREQ A • RATIO	
A channel input controls	
Gain	Channel A input sensitivity control, provides variable trigger level from 100 mV rms to 10V rms.

NORM • TEST

Normal/Test function switch. Provides coupling to the input circuits. In the TEST position connects the internal 1 MHz oscillator to the input circuits removing any signal input on the BNC. In the NORMAL position routes Input BNC to Input Circuits.

Input A

A channel input BNC connector. 1 MΩ impedance.

FREQUENCY A (kHz)

Mode Switch

Eight position rotary switch programs instrument to a mode of operation.

Provides for:

Count A/Count Off. Places instrument in Totalizer Mode. Count A provides continuous accumulation of input A signals. Count Off inhibits the input.

1 ms. Time base setting for frequency measurements. Provides for 1 kHz resolution of input A signals, also positions decimal point.

10 ms. Time base setting for frequency measurements. Provides for 100 Hz resolution of input A signals and positions the decimal point.

0.1 s. Time base setting for frequency measurements. Provides for 10 Hz resolution of input A signals and positions the decimal point.

1 s. Time base setting for the frequency measurements. Provides for 1 Hz resolution of input A signals and positions the decimal point.

10 s. Time base setting for the frequency meaaurements. Provides for 0.1 Hz resolution of input A signals and positions the decimal point.

100 s. Time base setting for frequency measurements. Provides for 0.01 Hz resolution of input A signals and positions the decimal point.

GATE

Gate indicator lamp. Provides front panel display of gate open time.

VISUAL DISPLAY

Provides six decades of in-line digital display indicators (eight with option Y2) with decimal point. Display reads in kHz in all positions of the mode switch.

TABLE 2-2

OPTION P1, CONNECTOR WIRING

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	10^0_0 1 bit	26	10^0_0 4 bit
2	10^1_0 2 bit	27	10^1_0 8 bit
3	10^1_1 1 bit	28	10^1_1 4 bit
4	10^1_2 2 bit	29	10^2_2 8 bit
5	10^2_2 1 bit	30	10^2_2 4 bit
6	10^2_3 2 bit	31	10^3_3 8 bit
7	10^3_3 1 bit	32	10^3_3 4 bit
8	10^4_4 2 bit	33	10^4_4 8 bit
9	10^4_4 1 bit	34	10^4_4 4 bit
10	10^5_5 2 bit	35	10^5_5 8 bit
11	10^5_5 1 bit	36	10^5_5 4 bit
12	10^6_6 2 bit	37	10^6_6 8 bit
13	10^6_6 1 bit	38	10^6_6 4 bit
14	10^7_7 2 bit	39	10^7_7 8 bit
15	10^7_7 1 bit	40	10^7_7 4 bit
16	10^7 2 bit	41	10^7 8 bit
17	Decimal 1 bit	42	Decimal 4 bit
18	Decimal 2 bit	43	Decimal 8 bit
19	Legend 1 bit	44	Legend 4 bit
20	Legend 2 bit	45	Legend 8 bit
21	NC	46	NC
22	+ Inhibit	47	NC
23	NC	48	Print Command
24	-9V Reference	49	NC
25	+ Reference (ground)	50	Ground

NOTES:

1. 10^0 is least significant digit and appears as the digit farthest to the right.
2. -9V Reference - Obtained from a resistor network consisting of 1.5k ohms in series with -12V with 4.7k ohms to ground.
3. Binary Data. 1-2-4-8 BCD; binary "0" = 0V (±0.7V), binary "1" = +3.6V (±0.7V).
4. Decimal Point and Legend - One digit each, 1-2-4-8 BCD; Binary "0" = -12V nominal, Binary "1" = -0.2V nominal. Output resistance is 22k ohm maximum.
5. Print Command = Negative going step at end of count cycle from 0V to -12V nominal with fall time less than 1 microsecond; 5k ohm internal resistance. Return to 0 volt remains longer than 15 microseconds.
6. Reset Inhibit:- Accepts an inhibit level of 0 volts if supplied from less than 1k ohm resistance or -6V to -30V from any source resistance.
7. Inhibit Release - Accepts a release level of 0 volts to -6V if from greater than 20k ohm resistance or -6V to -30V from any source resistance.
8. Output connector is Amphenol 57-40500. Mating connector is Amphenol 57-30500.
9. Printer Format - Standard: LDXXXXXXX:

   L = Legend X = Data

   1 = μs, 2 = ms, 3 = s, 4 = MHz, 5 = kHz

   D = Decimal Point, position from right.

TABLE 2-3

OPTION P2, CONNECTOR WIRING

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	10^0_0 1 bit	26	10^0_0 4 bit
2	10^1_0 2 bit	27	10^1_0 8 bit
3	10^1_1 1 bit	28	10^1_1 4 bit
4	10^2_2 2 bit	29	10^2_2 8 bit
5	10^2_2 1 bit	30	10^2_2 4 bit
6	10^3_3 2 bit	31	10^3_3 8 bit
7	10^3_3 1 bit	32	10^3_3 4 bit
8	10^4_4 2 bit	33	10^4_4 8 bit
9	10^4_4 1 bit	34	10^4_4 4 bit
10	10^5_5 2 bit	35	10^5_5 8 bit
11	10^5_5 1 bit	36	10^5_5 4 bit
12	10^6_6 2 bit	37	10^6_6 8 bit
13	10^6_6 1 bit	38	10^6_6 4 bit
14	10^7_7 2 bit	39	10^7_7 8 bit
15	10^7_7 1 bit	40	10^7_7 4 bit
16	10^{7} 2 bit	41	10^{7} 8 bit
17	Decimal 1 bit	42	Decimal 4 bit
18	Decimal 2 bit	43	Decimal 8 bit
19	Legend 1 bit	44	Legend 4 bit
20	Legend 2 bit	45	Legend 8 bit
21	NC	46	NC
22	+ inhibit	47	NC
23	NC	48	Print Command
24	-9V Reference	49	NC
25	+ Reference (ground)	50	Ground

NOTES:

1. 10^0 is least significant digit and appears as the digit farthest to the right.
2. -9V Reference - Obtained from a resistor network consisting of 1.5k ohms in series with -12V with 4.7k ohms to ground.
3. Binary Data - 1-2-4-8 BCD; binary "0" = -12V, binary "1" = -0.2V nominal.
4. Decimal Point and Legend - One digit each, 1-2-4-8 BCD; Binary "0" = -12V nominal, Binary "1" = -0.2V nominal. Output resistance is 22k ohm maximum.
5. Print Command - Negative going step at end of count cycle from 0V to -12V nominal with fall time less than 1 microsecond; 5k ohm internal resistance. Return to 0 volt remains longer than 15 microseconds.
6. Reset Inhibit:- Accepts an inhibit level of 0 volts is supplied from less than 1k ohm resistance; to +30V at up to 30k ohm resistance.
7. Inhibit Release - Accepts a release level of 0 volts to -6V if from greater than 20k ohm resistance or -6V to -30V from any source resistance.
8. Output connector is Amphenol 57-40500. Mating connector is Amphenol 57-30500.
9. Printer Format - Standard: LDXXXXXXX:

   L = Legend X = Data

   1 = μs, 2 = ms, 3 = s, 4 = MHz, 5 = kHz

   D = Decimal Point, position from right.

SECTION 3

THEORY OF OPERATION

SECTION 3
THEORY OF OPERATION

3.1 GENERAL

This section of the manual describes the Model 1615 Frequency Counter theory of operation from a block diagram analysis.

The Model 1615 Frequency Counter is designed to perform frequency measurements to 200 MHz, with time base selections of 1 ms through 100 seconds in decade steps, and to perform totalizing of random events at rates to 200 MHz. Operation in either the Count Mode or frequency mode is controlled by the front panel Mode switch which programs respective circuits throughout the instrument. Ratio measurements are also possible in the frequency modes when an external signal is applied to the external oscillator input (B input) connector.

The visual display is presented on six in-line digital display indicators with automatic decimal points for a reading in kHz. Stored display is featured with updating, once per measurement, accomplished by a store command pulse. Display Time, independent of gate time, is variable from 0.1 second to 10 seconds with a switched infinite position. Reset is automatic and produced by the trailing edge of the display time pulse. In the infinite display setting automatic reset is not produced and the instrument requires a manually generated reset trigger.

3.2 BLOCK DIAGRAM

A simplified block diagram is shown on figure 3-1, for more detailed circuit description and identification of circuit components and locations refer to the respective schematics. As shown on figure 3-1 the Model 1615 consist of: The Input Circuits; the Time Base and Control Circuits and the Count Chain Circuits.

The input circuits consists of a high gain, wide band frequency amplifier. Inputs from 20 Hz to 200 MHz over a dynamic sensitivity range of 100 mV rms to 10V rms are readily accepted. A unique combination of input attenuators, variable gain control, and frequency compensation provide for wide band amplification with high noise rejection capability.

The time base and control circuits develope: the time base gates, 1 ms through 100 seconds, for frequency measurements; gate control, for count measurements; the store command; print command and automatic reset signals.

The count chain circuits perform: counting of the input signal, storage, and converting it to decimal data for display on the visual digital display indicators.

3.2.1 Circuit Operation

Operation is in two basic modes, i.e. Count or Frequency. A third mode of operation is the Ratio Mode which is similar to operating in the Frequency Mode. In either mode of operation count signal flow through the Input Circuits is controlled (gated) by the Start Stop Flip-flop in the Control Logic: In the "count" mode this gate is manually produced by manipulation of the Mode switch. In the "Count A" position the Start Stop Flip-flop is set (gate on) and in the Count Off position the flip-flop is reset (gate off). In the Frequency Modes the gate is automatically controlled by the time base counter circuits. The input circuits are gated on at Start time and off at Stop time. At Stop time the BCD data is transferred to the storage circuits, decoded and coupled to the visual display indicators. Unless placed in the infinite display setting a new measurement cycle is automatically initiated with the reset signal.

3.2.2. Input Circuits Operation (see Input A Schematic C-11-05491)

The input trigger amplifier consists of: The input attenuators, and limiter network; the wide band input amplifier stage; the shaper amplifiers and count chain driver and the gate circuits.

Input signals are coupled to Q101 the input FET amplifier via the input attenuator and gain control network. The gain control potentiometer R127 functions as a voltage divider for the attenuator network bias control. The input signal is developed across the variable impedance produced by the relative conduction state of the attenuator diodes CR103 and CR104. Increasing the conduction of the attenuator diodes reduces the load impedance and thus increases the attenuation. Dual attenuation with both high and low frequency compensation provides a more uniform flat response over the entire band The attenuator network performs the dual function of gain control and limiting, thus preventing overdriving of the input amplifier. Less than unity gain is realized with limiting (due to CR103 and CR104) occurring at 0.7 volts.

The input FET Q101 and amplifier stages Q102, Q103 and Q104 function as a wide band amplifier with an overall gain of ten. DC feedback coupled through Q111 compensates for any temperature drift experienced in the amplifier. Q111 is a comparator stage and monitors the output of Q104. Q111's output is filtered by the frequency bypassing

action of C112, 113 and 114. Both high and low frequency compensation is employed to provide a flat response over the entire band.

Q104's output is coupled to the dual schmitt trigger shaper stages Q105-Q108. Operation of Q105, 106 is controlled by the gate signal applied to the gate switch Q110. During gate on time Q110 is turned off which allows the schmitt trigger to operate. At gate off time Q110 is turned on thereby gating off the schmitt trigger stage.

The output from the shaper circuits is coupled to the emitter follower ring driver amplifier Q109. Q109 performs the dual function of producing the count signal to the count chain and setting the quinary ring bias level. R105 the ring counter level adjust is set to provide optimum triggering of the ring counter for all count ranges.

R105 should not require adjustment and normally should not be adjusted in the field. A rough alignment of R105 can be obtained by making note of the position of R105 at 20 Hz and 200 MHz that allows the counter to operate correctly at both frequencies for the same adjustment setting.

3.2.3 Time Base and Control Logic Operation. (see Time Base schematic D-11-05495)

The Time Base and Control Logic contains: The 1 MHz reference oscillator circuits; the time base dividers; the store command generator; the display timer, manual and automatic reset generator; and the control logic.

The time base circuits are continuous running frequency dividers. The time base gate selected is determined by the mode switch setting. Opening the gate permits accumulation of input counts whereas closing the gate stops the counting action and produces the store command signal and display timer enabling. The end of the display cycle generates the automatic reset signal which initiates a new measurement cycle. In the "Count" mode the control circuit is continuously enabled producing a gate on condition and the store command signal line is held in an enable state allowing the count chain to follow the accumulating count procession in the count chain.

1 MHz Reference Oscillator Circuitry. The reference oscillator is a modified 1 MHz crystal controlled colpitts oscillator. The 1 MHz crystal and Q1 through Q4 make up the oscillator circuits. Q1 and FET source follower provides the amplification and feedback to sustain oscillations with Q2 an emitter follower providing, isolation for the

frequency determining circuits and drive to the load. The 1 MHz Test signal is also taken from this output. The clock output is ac coupled to the shaper Q3 and 4 through the Int/Ext oscillator selector switch. J3 the internal monitor/external input (B input) connector is also wired to this junction. The shaped clock output from the collector of Q4 is used to drive the divide-by-1000 counting unit.

Time Base Counter. The time base counter contains a divide-by-1000 counting unit and five DCU's interconnected in cascade to provide gate times of 1 millisecond to 100 seconds. In frequency operation these are selected by the mode switch. Clock outputs of 1 millisecond, 100 milliseconds, 0.1 seconds, 1 second, 10 seconds or 100 seconds are coupled as start and stop signals to the start stop control flip-flop here-in-after referred to as the control flip-flop. The divide-by-1000 CU contains 10 cascaded binaries, MC1 - MC5 with feed back to stages 4 and 5, which produce an output for every 1000 clock inputs. This 1 millisecond clock is coupled to the 10 millisecond DCU (MC10 and MC11) and the mode switch. The output of the 10 millisecond DCU is coupled to the 0.1 second DCU (MC8 and MC9) and the mode switch. The output of the 0.1 second DCU is coupled to the 1 second DCU (MC6 and MC7) and the mode switch. The output of the 1 second DCU is coupled to the 10 second DCU (MC14 and MC15) and the mode switch. The output of the 10 second DCU is coupled to the 100 second DCU (MC12 and MC13) and the mode switch. The mode switch is an eight position rotary switch. In the frequency mode positions the clock output from the time base counters is routed via the mode switch, to the control flip-flop.

3.2.3.1 Control and Display Flip-flop Operation. The control and display flip-flops are derived from an MC790P Dual J-K Flip-flop integrated circuit. After reset both flip-flops are enabled and will toggle on negative going inputs. The first clock output after reset from the time base counter (1 ms through 100 s whatever) sets the control flip-flop. This complements the output levels, (pin 8 goes low and pin 9 goes high) and gates on Q5, the gate lamp driver, and the input circuits gate shaper Q6 and Q7. The gate lamp provides visual indication, at the front panel, of gating action. The input gate shaper couples an inhibit gate to Q111 of the input circuits thereby allowing input signals through to the count chain by gating Q111 off. The next clock input (negative transition) to the control flip-flop toggles it back to the reset state. Complementing the control flip-flop from the set state to the reset state couples a negative going trigger to the display flip-flop which sets it, and enables the store command circuits. Setting the display flip-flop inhibits the control flip-flop and enables the display timer.

The display flip-flop inhibits the control flip-flop until the reset signal resets the display flip-flop. At the end of the display time a reset pulse is generated. This returns all circuits to a normal state and allows a new measurement cycle by removing the inhibit level applied to the control flip-flop.

3.2.3.2 Store Command. The store command circuits consist of: The input gate MC17D, the one shot trigger circuit C8, R22-24 and CR7 and the 8 microsecond one shot MC16A and C7. The closing of the gate (resetting the control flip-flop) enables MC17D. MC17D's output is differentiated by R24 and C8 and coupled as the negative trigger pulse via CR7 to the store command one-shot MC16A. MC16A is an MC788P wired in a one-shot configuration with regenerative feedback through C8 holding it on for approximately 8 microseconds. The 6 to 8 microsecond pulse output from MC16A is routed to the count chain buffer storage elements as the store command signal. This transfers the stored data to the visual display circuits.

3.2.3.3 Display Timer and Reset Generator Operation. Setting the display flip-flop complements its output with pin 14 going low and pin 13 going high. This performs the dual function of inhibiting the start flip-flop, thus preventing the continuous clock outputs from the time base from generating a new measurement; and turns Q9 on which enables the display timer circuits. The display timer is basically a relaxation oscillator comprised of: The display time control potentiometer R34, the timing capacitor C13 and the switching element Q11 a uni-junction transistor (UJT). The switch S3 is concentric with the display potentiometer and is opened in the full clock wise position of the control. This inhibits display timer action and requires a manual reset to initiate a measurement cycle.

In the quiescent state: Q10 is off, Q11 is off and the capacitor C13 is in a neutral state (no charge). Setting the display flip-flop turns on Q10 and allows the timing capacitor to charge through the high resistive path of the display potentiometer and R32. When the charge on C13 reaches the emitter peak point voltage Q11 turns on. This discharges the timing capacitor through the relatively low resistance of the UJT and develops the trigger pulse for the reset generator. MC16B (the other half of the store command chip) is also wired in a one-shot configuration and provides a reset pulse approximately 28 microseconds wide. This signal is coupled through the emitter follower reset line driver Q12 and distributed throughout the instrument.

3.2.3.4 Gate Shaper Circuit Q6 and Q7. The gate shaper compensates for gating ambiguity caused by the fall time characteristics of the gate off signal. The gate on gate off rise and fall time constants are very different with a much longer fall time for the gate off signal as compared to the gate on rise time. This non-linearity, when used to gate increments at 5 nanosecond (200 MHz) rates, can cause counting errors as great as ±4 counts. Q6, Q7 and C6 function as an integrating network and is used to delay the rise time characteristics of the gate on signal. Integrating the leading edge of the gate allows for balancing the inequities between the two edges; and permits adjustment of the gate to within ±1 count errors. C6 is normally a factory adjust (requiring a phased locked signal) and should not require field calibration.

3.2.4 Count Chain and Display Circuits (see schematics D-11-05493).
The count chain circuits consist of the decade counters, decoding matrices and storage elements for counting the input signals and providing the necessary binary to decimal conversion for stored display of the decoded information.

3.2.4.1 The decade counters consist of six cascaded DCU's (decade counting units). In the first DCU's, due to the high speed requirement, a combination of discrete and micrologic circuitry is employed.

The 10^0 DCU is a Qui-binary discrete circuit with Q220 through Q228 and CR221 through CR225 making up the quinary ring. The N/5 count is coupled via the binary driver Q216 and Q217 to the binary element MC21. The binary weighted information is coupled by the encoding gates, comprised of: the resistive network R225 through R234, the gate transistors Q203 through Q213 and encoding diodes CR201 through CR216; as four line 1-2-4-8 BCD to the storage register MC32.

The 10^1 DCU is a bi-quinary hybrid DCU comprised of MC20 an MC1013P micrologic, and the quinary stage MC18 and MC19. The 1-2-4-8 BCD output is coupled to the Storage register MC33.

The 10^2 through 10^5 DCU's are CμL 9958 micrologic decade counters MC39 through MC43.

The 10^0 through 10^5 storage registers are CμL 9959 Buffer Storage elements MC32 through MC37. Here the 1-2-4-8 BCD data is stored and coupled to the decoding matrix for visual readout. The store command signal enables the storage elements once each

measurement cycle (at gate closure time) thus updating the register with the new measurement information.

The 10^0 through 10^5 decoding matrices are CμL 9960 decimal decoding drivers MC24 through MC29. Here the four line 1-2-4-8 BCD is decoded into a decimal number and drives the appropriate cathode of the gas filled readout tube displaying the number.

3.2.4.2 Decimal Display. The visual display consist of six decades of digital display tubes with built-in decimal points. Which decimal point in which tube lights is controlled by the Mode Switch. See the Time Base and Control Logic Schematic D-11-05495. Section B of S1 is returned to ground and as the mode switch is positioned the appropriate decimal light is turned on in the display tube. See paragraph 2.2.1 for the decimal point location and the visual display for each switch position. This section of S1 also controlls the decimal point for printers when printer option P1 or P2 is installed.

3.2.4.3 Count Chain reset. Because of the hybrid nature in circuit construction of the count chain logic, four different reset signals are developed. These are coincident with "Reset" and are shaped and referenced to particular dc levels for proper reset toggling of the various flip-flops and discrete circuits employed. MC17C, Q218, and Q219 and their respective differentiating circuits provide three separate reset signals for the discrete count chain and the MECL micrologics MC20 and MC21. Q218's output is shaped, to a positive 6 volt reset trigger, by CR205 and C201 and clamped to a -6 volt reference level by CR226. Q218's output is also routed to alternate stages of the quinary ring (Q221 and Q225) via C203. However, R240 and R241 reference this pulse to a -6 volts. The negative going output from Q219 is coupled to the remaining stages (Q223, Q227 and Q229) of the quinary ring via C205. This pulse is reference to +6 volts by R244 and R245. The remaining 10^1 through 10^5 decade counters are reset directly by the reset generator output.

3.2.5 Power Supply Operation (see schematic C-11-05384)

The Model 1615 power supply develops the regulated -12Vdc, +12Vdc, +3.6Vdc and the unregulated 210Vdc voltages. A fourth regulated voltage, a -5.2Vdc is developed by CR226.

The power transformer T1 has a dual primary and can be wired for 230Vac or 115Vac operation. Three secondary windings provide the voltage distribution for the appropriate

outputs. The +12, -12 and +3.6 volt supplies are series regulators and are calibrated by R5 and R7. The -12V supply is the reference source and should be calibrated first.

-12 Volt operation

The -12 volt regulated supply consist of: The fullwave rectifier circuit CR6 and 8 and filter capacitor C4; the series pass element Q4 and the error sense amplifier circuit Q3. CR5 and R5 set the reference bias for Q3. Q3 in turn controls the bias on the series pass element Q4. The conduction of Q4 provides a constant -12 volt output. Any change in the output level is detected by the sense amplifier and applied as a change in bias on Q4. This increases or decreases the conduction (increasing or decreasing the IR drop) of Q4 to compensate for the change and correct it.

+12 Volt operation

The +12 volt supply is similar to the -12 volt supply with R7 providing the calibration control. Q5 is the series pass element and Q6, 7 and 9 the error sense amplifier circuitry.

+3.6 Volt operation

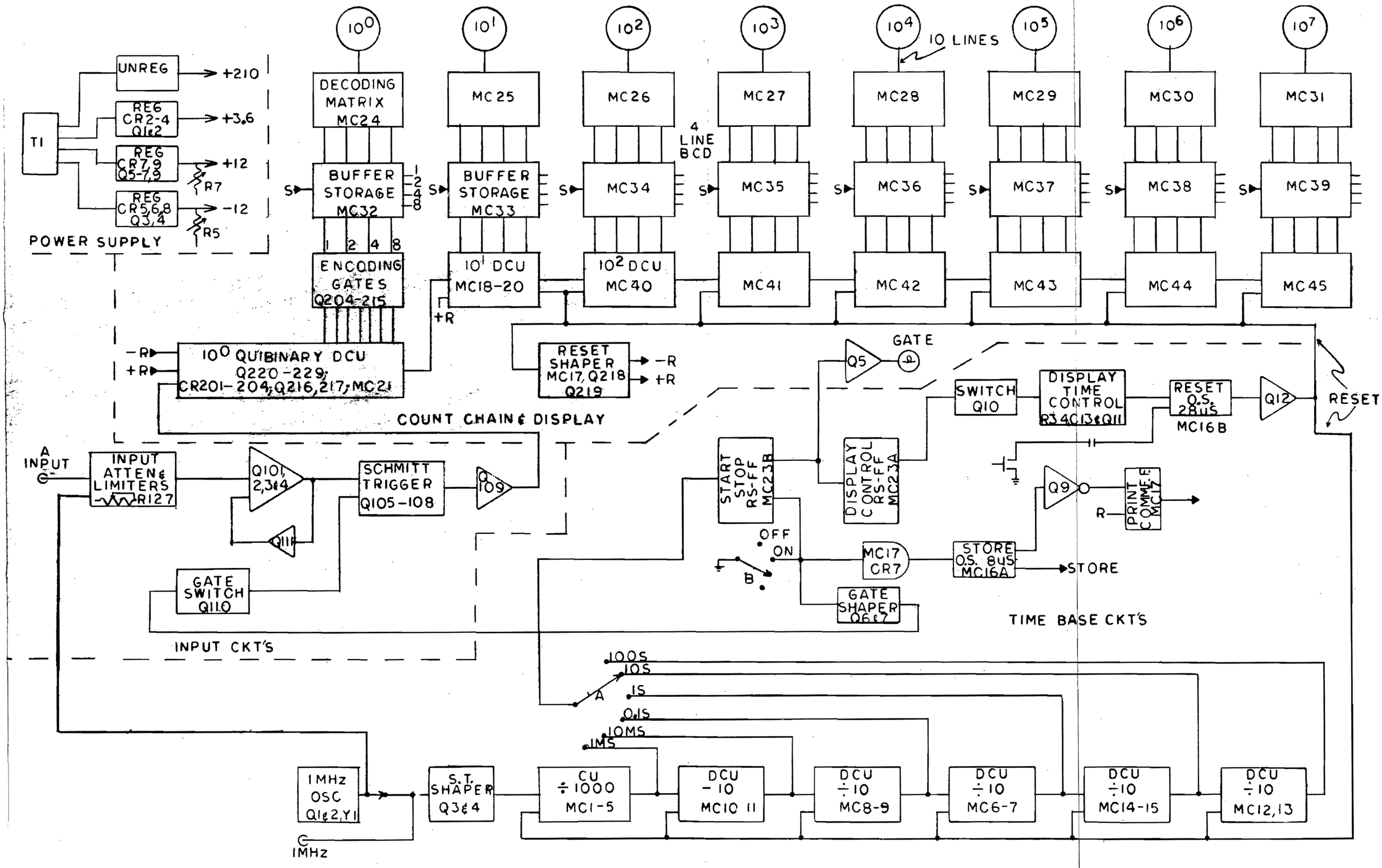
The +3.6 volt supply is regulated but not adjustable. CR4 and R4 provide the reference bias to the error sensing amplifier Q2, thereby, controlling the conduction of the series pass element Q1.

-5.2 Volt operation

The -5.2 volt regulated supply is a zener regulated (CR226) output taken from the -12 volt supply and is used by the MECL logic in 10^0 and 10^1 DCU's in the count chain circuits.

+210 Volt operation

The +210 volt supply is developed by the halfwave rectifier circuit CR1 and R2. The output is applied as the excitation voltage for the digital display indicators.



MODEL 1615
FIGURE 3-1 SIMPLIFIED BLOCK DIAGRAM

SECTION 4

MAINTENANCE AND CALIBRATION

SECTION 4

MAINTENANCE AND CALIBRATION

4.1 GENERAL

This section outlines maintenance test and calibration procedures, component location drawings and parts removal/replacement techniques.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance is the systematic care, servicing, and inspection of the equipment to prevent the occurance of trouble, to reduce down time and to assure that the equipment is servicable. When implemented into a meaningful schedule these checks and services provide significant operational data on the instrument to help prevent instrument failure and improve reliability. The severity of the environment will determine the frequency of the maintenance.

4.2.1 Cleaning. Clean the equipment by brushing, wiping with a lint free cloth, vacuuming or by blowing with compressed air. Solvents (non-corrosive) may be used for additional cleaning action if necessary. The following materials, or their equivalents, are used for maintenance.

Lint free cloth
Stiff (non-metallic) bristle brush
Solvent (alcohol and water 50/50)
RP Filter coat
Compressed air (filtered, moisture-and-oil-free, 30 psi maximum)
WARNING: When using solvents provide adequate ventilation and skin protection.

4.2.2 Preventive Maintenance Checks

Monthly (as deemed appropriate) maintenance schedule.

1. Check the tightness and general condition of all external connectors.
2. Operate in the Self Test mode and observe that the mechanical action of each switch is smooth and free of external or internal binding and no excessive looseness is apparent.
3. Check the 1 MHz output with a frequency standard.
4. Check for unobstructed airflow and blower operation.

Quarterly maintenance schedule.

1. Power transformer and power supply. Inspect wiring on the power transformer, inspect filter capacitors, no dirt, corrosion or oil should be evident, check for signs of overheating.
2. Inspect all internal and external connectors for mechanical condition.
3. Inspect the air filter and blower, no dirt, etc.
4. Inspect cords cables and wires for chafed, cracked or frayed insulation.
5. Perform incoming operational check as outlined in Section 2.

4.3 TEST PROCEDURE/CALIBRATION

Test and calibration of electronic equipment should be performed to maintain optimum overall operational efficiency. Testing, to seek out circuit abnormalities; and calibration, to return the system to within published specifications. Indiscriminate tweaking, probing, etc., is ill advised and rather than improving operation the opposite can result.

A list of test equipment includes: any voltmeter or DVM (3% accuracy), almost any oscilloscope (to 10 MHz) an audio and RF signal generator, a 1 MHz frequency standard and a 200 MHz Multiplier Test Jig (coherent to the 1 MHz time base reference oscillator).

CAUTIONS:

1. This instrument contains transistorized circuits. If any equipment item does not have an isolation transformer in its power supply circuit, connect one in the power input circuit.
2. Never connect test equipment (other than oscilloscopes, multimeters and VTM's) outputs directly to a transistor circuit, use a coupling capacitor.
3. Make test equipment connections with care so that shorts will not be caused by test equipment connectors. When making contact to the circuit under test, tape or sleeve (spaghetti) test prods or clips to leave as little area exposed as possible to minimize inadvertant shorts.
4. The equipment must be turned off before removing any plug-in component, PCB, micrologic, transistor, etc.

4.3.1 Power Supply

This unit has five operating voltages from regulated and non-regulated supplies. Test points are identified and screened on the PCB see schematic and PCB component location diagrams.

Apply power (115Vac, 60 Hz) and measure the power supply outputs as listed below:

+210Vdc = +210Vdc ± 20 Vdc
+12Vdc = +12Vdc ± 0.15Vdc
+3.6Vdc = +3.6Vdc ±0.36Vdc
-5.2Vdc = -5.2Vdc ± 0.15Vdc
-12Vdc = -12Vdc ± -.15Vdc

With an oscilloscope check for ripple on the supplies. Ripple should be less than 100 mV/P-P on the +12, -12 and +3.6 volt regulated supplies. The +210 volt supply is used for readout illumination and ripple in excess of 40V P-P is normal.

Power Supply Calibration

The -12Vdc supply is the reference source for both the +12 and +3.6 volt supplies and must be calibrated first.

-12Vdc: Adjust R5 for -12Vdc ± 0.15Vdc
+12Vdc: Adjust R7 for +12Vdc ± 0.15Vdc
This should bring the +3.6 volts to within ±0.36 volts of 3.6Vdc.

The -5.2Vdc supply is developed by CR226 a 5.2V zener diode, no adjustment is required. Replace diode if level is out of tolerance.

4.3.2 Time Base Test and Reference Oscillator Calibration

Test the time base circuits for proper counting of the reference oscillator to produce the appropriate time base gates.

a. Connect an oscilloscope to the Oscillator Monitor BNC (slide switch set to Int. Osc.) and monitor the frequency and amplitude of the output for 1 MHz at ≃6V peak-to-peak.
b. Apply a 100 kHz test signal input to the Input A BNC and observe the visual display for the proper readout on each setting (1 ms through 100 s) of the frequency selector switch. For six digit instruments use 10 kHz and for the 100 s setting use 1 kHz.
c. Monitor the gate light operation on time base settings above 0.1s.

Reference Oscillator Calibration

a. Connect the 1 MHz frequency standard to the oscilloscope external trigger input.

b. Connect a cable between the 1 MHz output connector and the oscilloscope vertical input. Place the oscillator switch to the Int. Position.

c. Monitor the scope and adjust C1 so that as nearly as possible the trace stops moving. Scope sweep should stabilize for≃ 8 to 10 seconds.

4.3.3 Storage Transfer, Display Time and Reset Test.

Store commands and reset signals are automatic in the frequency modes.

a. Store Command - With an oscilloscope monitor the output, pin 12, of MC16A for a +2 volt, 2 - 8 microsecond width store command signal.

b. Reset - With an oscilloscope monitor the reset output, Test point R, for a +1.5V (±0.3V) 27 microsecond (±5 μs) pulse.

c. Display Time - In the Self Test frequency mode setting >0.1 s observe the gate lamp for gate off time of <0.1 second to >10 seconds while varing the Display Time Control.

4.3.4 Gating Error

Rated accuracy of ±1 count ± oscillator stability is checked by monitoring the visual display while measuring a 200 MHz input signal. To nullify the effect of oscillator stability the 200 MHz test signal must be coherent to the 1 MHz reference oscillator. This is accomplished by using the internal oscillator output, multipling it by 200 and feeding it back as the input to the A input connector. An alternate method would be to use an external 1 MHz for the reference time base source (fed into input B) and multiply this up to 200 MHz for the A input signal. What ever the method, the visual display should read 200000 kHz ± 1 count.

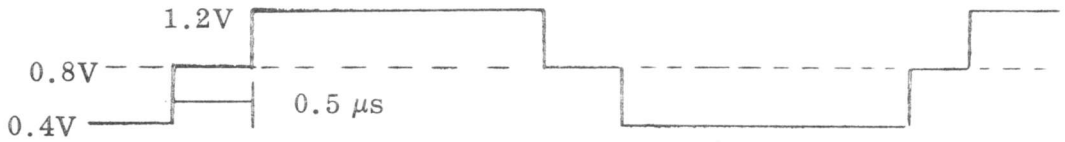
Gating Error Adjust. This adjustment (C6) is normally considered a factory adjust and should not require adjusting. If component replacement necessitates calibration, trim C6 for an optimum reading ± 1 count at 200 MHz. This adjustment should only be made under conditions as outlined above and only if replacement of circuit components makes it mandatory.

4.3.5 Count Chain Ring Counter Bias Adjust

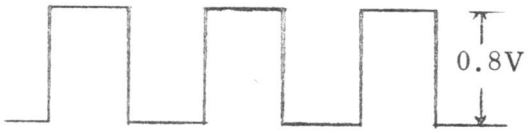
This is normally a one time factory adjust. The 10^0 DCU of the count chain provides the divide-by-ten function from a Qui-binary counter. The quinary ring contains precision

components and matched transistors. If, however, repairs or aging necessitate adjusting R105 procede as follows:

a. With a dc coupled oscilloscope observe the ring drive the ring output signals. The ring output, at any of the 150 Ω ring bias resistors R246-R250 should be:



The ring drive input signal should be:



b. While observing these signals adjust R105 to optimize this condition:

4.4 PARTS REMOVAL AND REPLACEMENT TECHNIQUES

Removal and/or replacement of component parts within the instrument are removable with tools normally found on any work bench.

The following precautionary procedures should be observed.

a. Use a pencil-type solder iron with 40 watts maximum capacity. Do not use a soldering gun; damaging voltages can be induced in components and heat generated will damage the PCB.

b. When soldering transistors leads, micromodules, etc., solder quickly. Whenever wiring permits, use a heat sink (long nose pliers, etc.) between the solder joint and the component. Use approximately the same length and dress of transistor leads as used originally.

c. When desoldering work quickly and do not overheat PCB wiring.

d. When installing a shielded wire, reconnect shield to the same tie point that it was removed from. Dress all wires in the same manner as removed. Route all wires in the same route as removed.

4.4.1 Micromodule Removal and Replacement - Removal and replacement of the micromodule is simplified by the use of proper tools. Although a soldering iron, small long nose pliers, small diagonals and a round tooth pick will do the job, the use of a rectangular soldering tip and a vacuum solder pick-up bulb (vacuum bulb) can greatly simplify the task.

To remove a micromodule:

a. Working from the top of the PCB, cut all leads on the micromodule at the plastic case.
b. Remove each lead from the PCB by heating with a soldering iron and withdrawing leads from the PCB (from the top) with small long nose pliers.
c. Remove all excess solder with a vacuum bulb or by heating holes and reaming clean with a round tooth pick.

To replace a micromodule:

a. Remove all excess solder from the PCB holes with soldering iron and vacuum bulb.
b. Insert replacement micromodule. Refer to component layout drawing for proper pin (pin 1) orientation.
c. Using small tip individually solder all connections from the bottom of the board.

Alternate procedure to remove a micromodule:

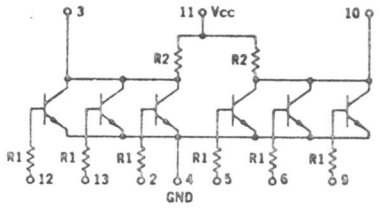
a. Using a solder iron with a special rectangular tip, apply heat simultaneously to all the micromodule connections.
b. Lift or pry micromodule out.
c. Remove excess solder with vacuum bulb.
d. Apply heat with caution, do not overheat PCB.

SECTION 5

SCHEMATICS

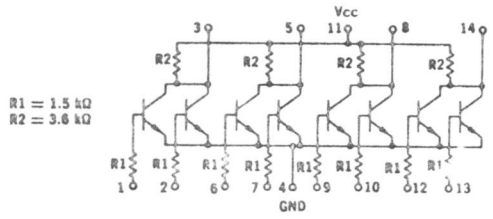
Integrated Circuits Schematic Equivalents MC715P - MC725P.

MC715P — DUAL 3-INPUT GATE



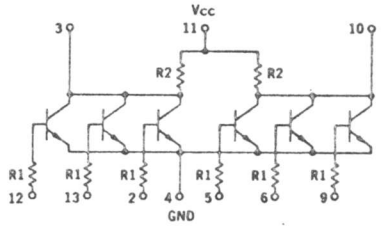
R1 = 450 Ω
R2 = 640 Ω

MC717P — QUAD 2-INPUT GATE



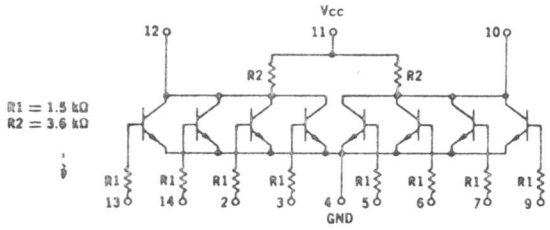
R1 = 1.5 kΩ
R2 = 3.6 kΩ

MC718P — DUAL 3-INPUT GATE



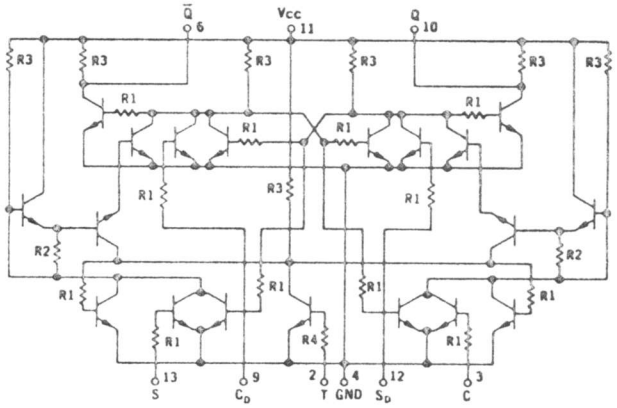
R1 = 1.5 kΩ
R2 = 3.6 kΩ

MC719P — DUAL 4-INPUT GATE



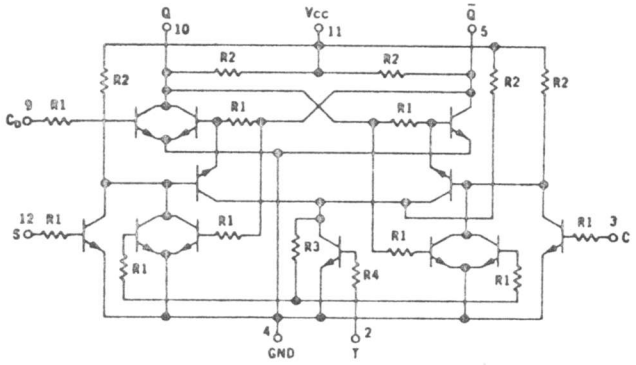
R1 = 1.5 kΩ
R2 = 3.6 kΩ

MC722P — J-K FLIP-FLOP



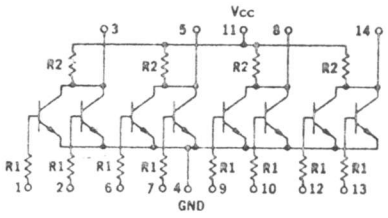
R1 = 1.5 kΩ
R2 = 2.0 kΩ
R3 = 3.6 kΩ
R4 = 750 Ω

MC723P — J-K FLIP-FLOP



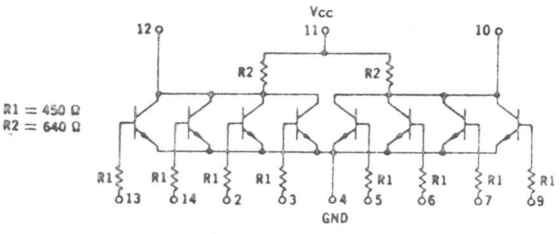
R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω

MC724P — QUAD 2-INPUT GATE



R1 = 450 Ω
R2 = 640 Ω

MC725P DUAL 4-INPUT GATE

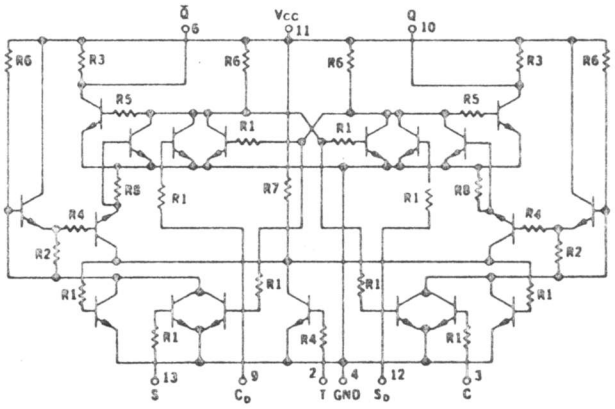


R1 = 450 Ω
R2 = 640 Ω

RESISTOR VALUES ARE TYPICAL.

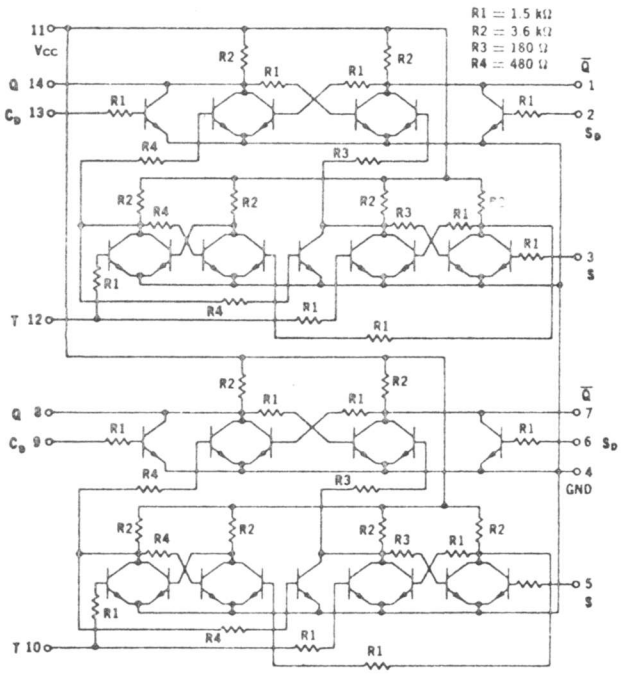
Integrated Circuits Schematic Equivalents MC726P - MC787P.

MC726P — J-K FLIP-FLOP

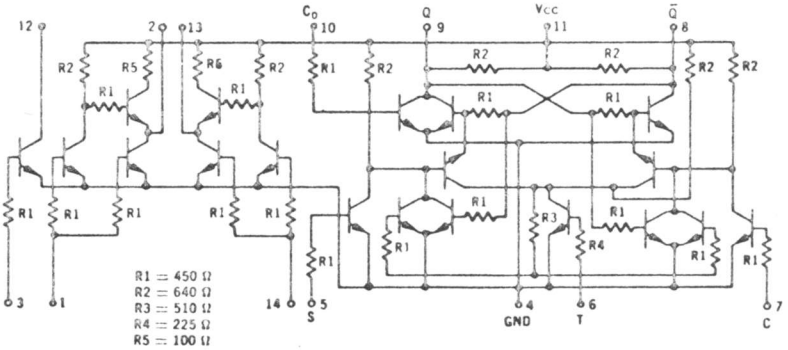


R1 = 600 Ω
R2 = 2 kΩ
R3 = 640 Ω
R4 = 300 Ω
R5 = 550 Ω
R6 = 900 Ω
R7 = 700 Ω
R8 = 3 kΩ

MC778P — DUAL TYPE "D" FLIP-FLOP

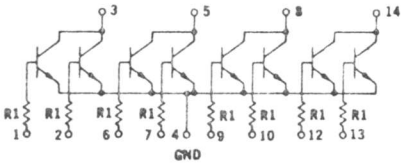


MC779P — MULTIFUNCTION (1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)



R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω
R5 = 100 Ω

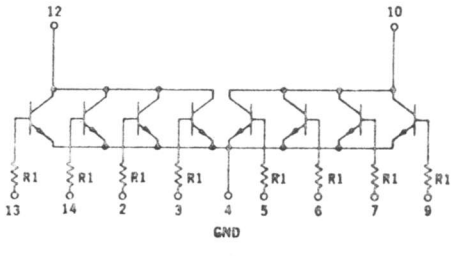
MC785P — QUAD 2-INPUT EXPANDER



R1 = 450 Ω

Vcc connection to pin 11 not shown

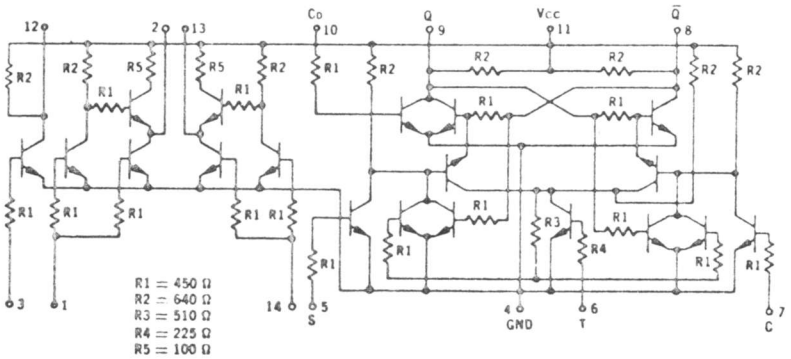
MC786P — DUAL 4-INPUT EXPANDER



R1 = 450 Ω

Vcc connection to pin 11 not shown

MC787P — MULTIFUNCTION (1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)

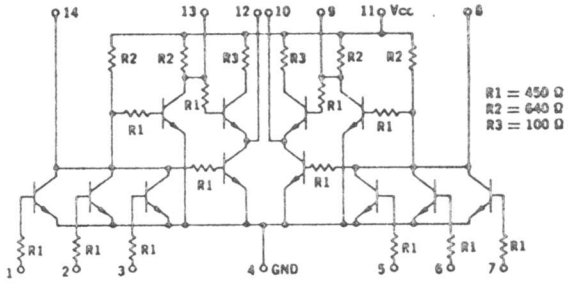


R1 = 450 Ω
R2 = 640 Ω
R3 = 510 Ω
R4 = 225 Ω
R5 = 100 Ω

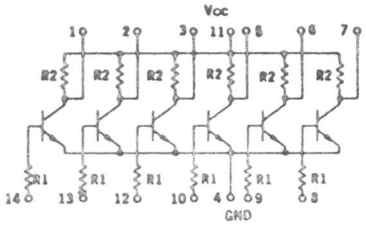
RESISTOR VALUES ARE TYPICAL.

Integrated Circuits Schematic Equivalents MC788P - MC799P.

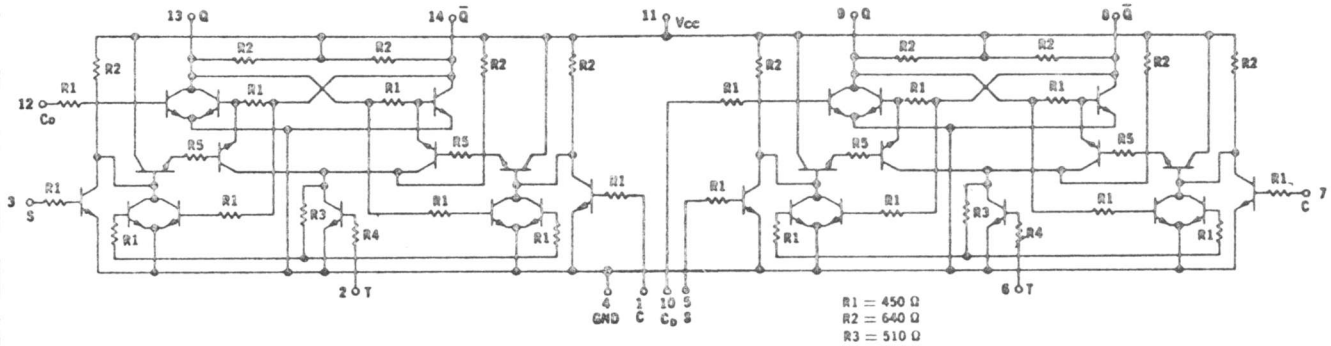
MC788P — DUAL 3-INPUT BUFFER
(NON-INVERTING)



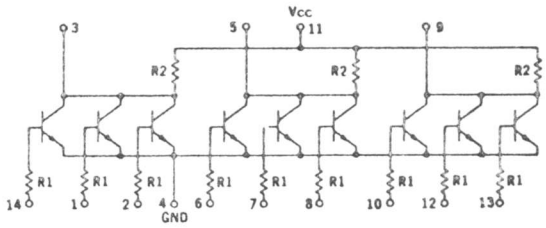
MC789P — HEX INVERTER



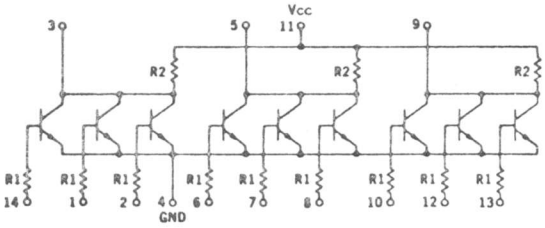
MC790P — DUAL J-K FLIP-FLOP



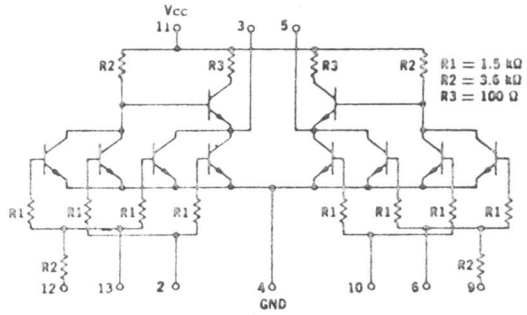
MC792P — TRIPLE 3-INPUT GATE



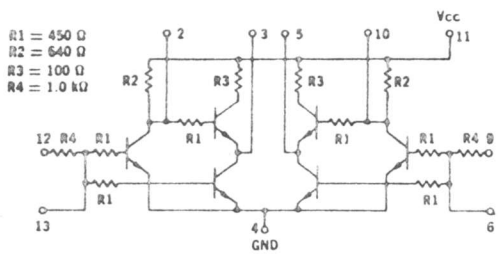
MC793P — TRIPLE 3-INPUT GATE



MC798P — DUAL 2-INPUT BUFFER



MC799P — DUAL BUFFER



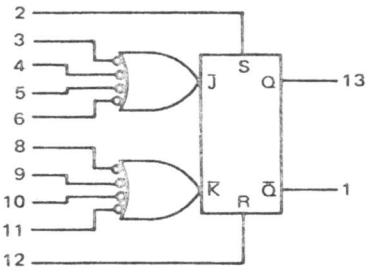
RESISTOR VALUES ARE TYPICAL.

Integrated Circuits Schematic Equivalent

MC1013
MC1213

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\overline{J}$ and $\overline{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ Inputs Are Static

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

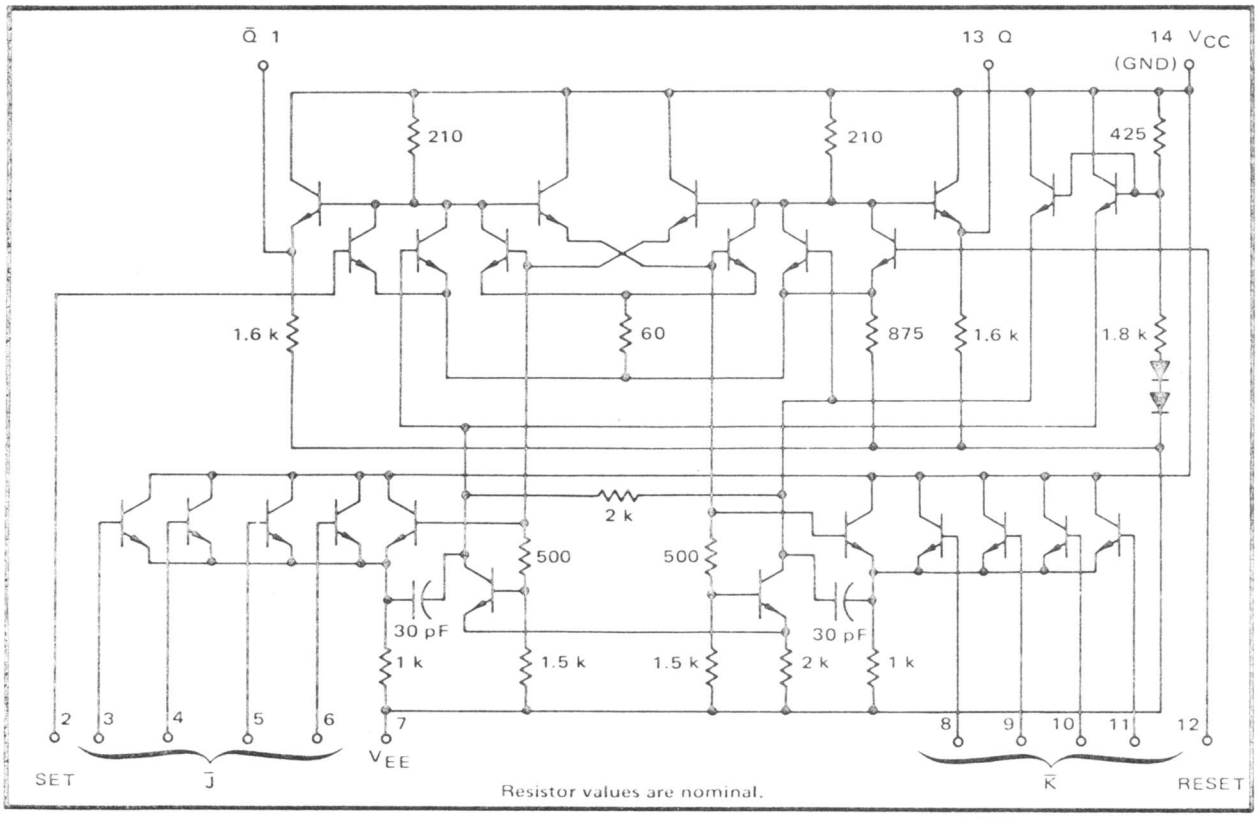
Pin No.	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

*Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
**$\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

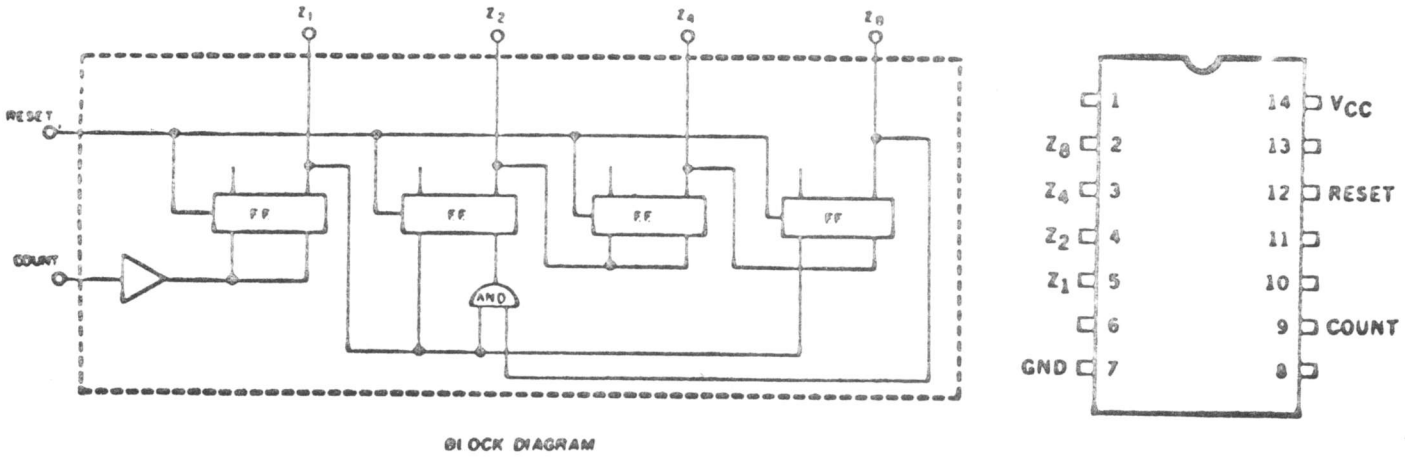
The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

CIRCUIT SCHEMATIC



Resistor values are nominal.

Integrated Circuits Schematic Equivalent CμL 9958

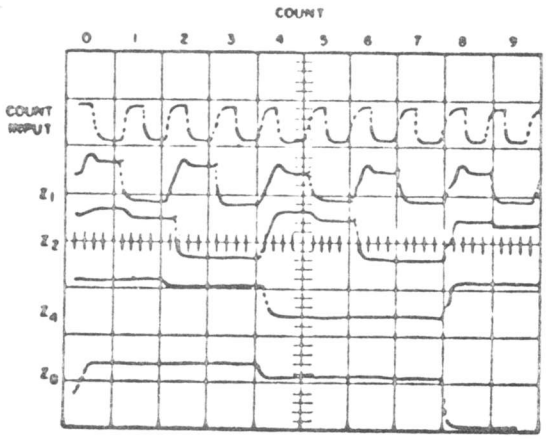


BLOCK DIAGRAM

	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L

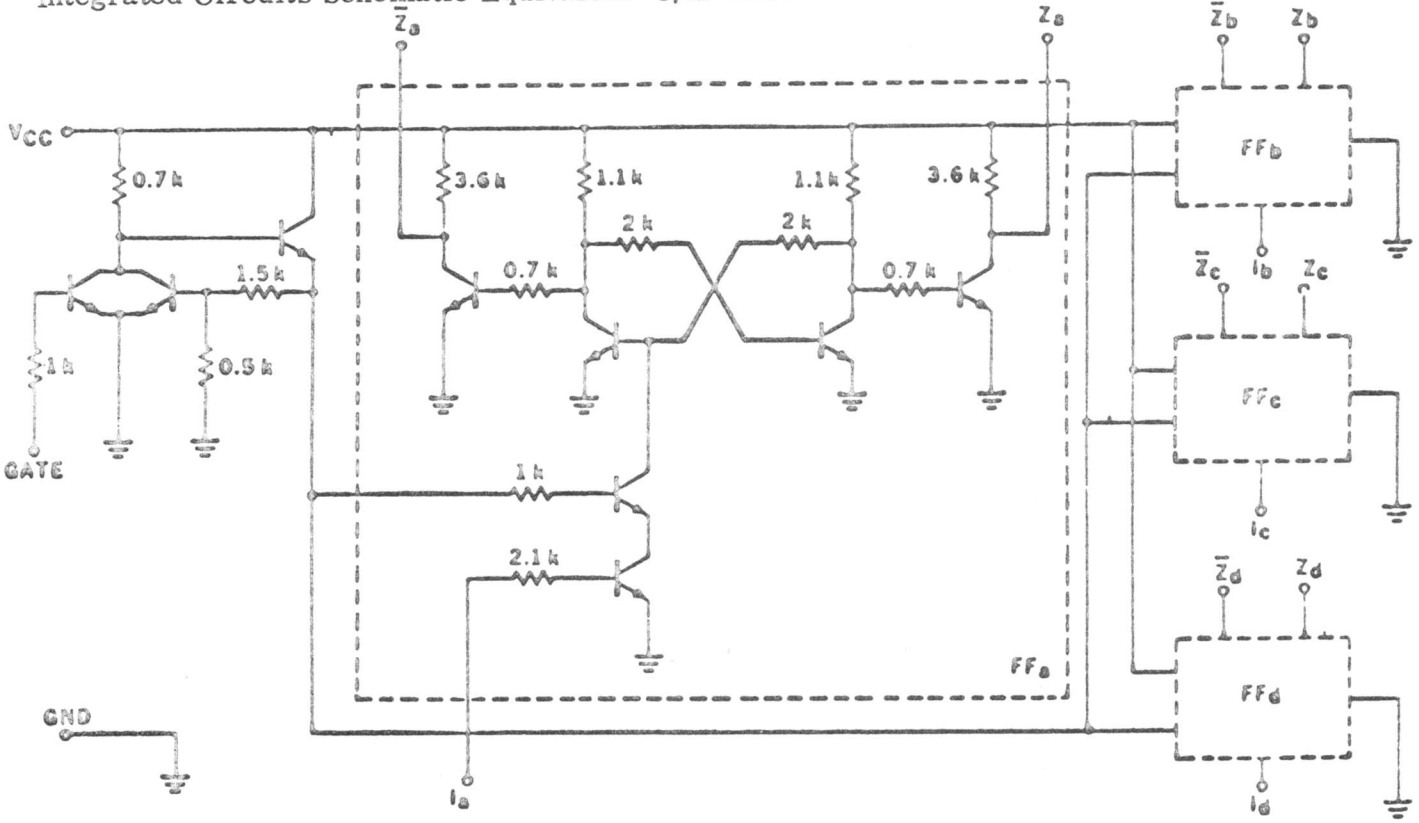
(H = HIGH L = LOW)

TRUTH TABLE

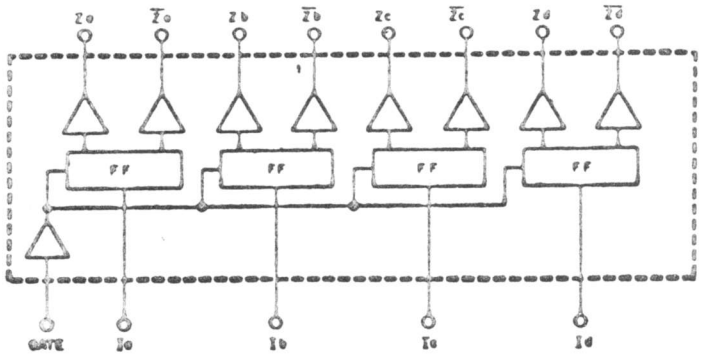


Circuit Block Diagram and Pin Number Functions CμL 9958

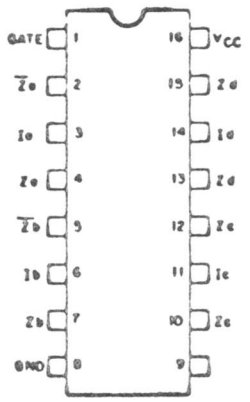
Integrated Circuits Schematic Equivalent CμL 9959



Schematic Diagram Buffer Storage Unit CμL 9959



BLOCK DIAGRAM



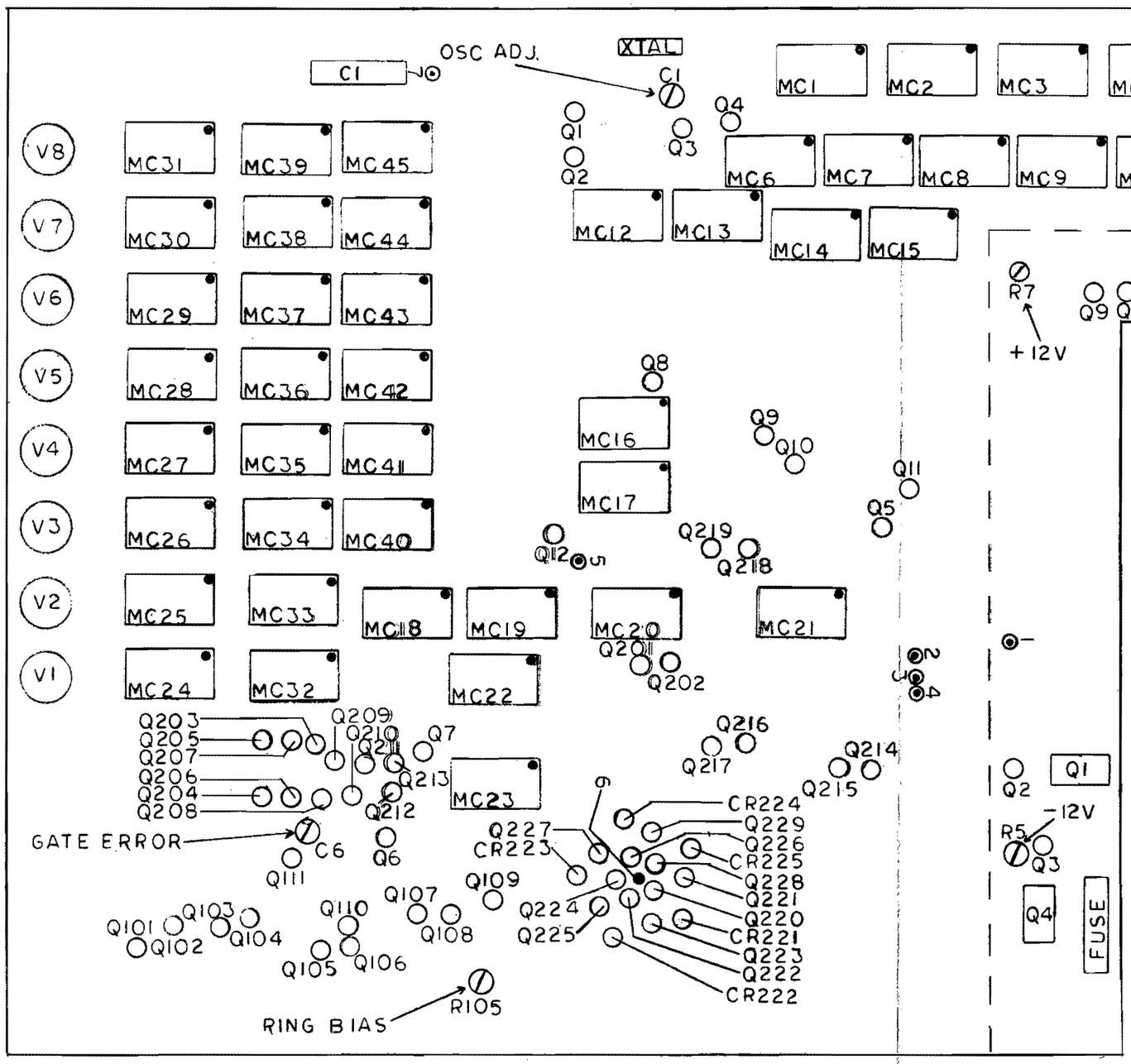
BASE CONNECTIONS

GATE	I	Z	$\bar{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\bar{Q}$

H = HIGH
L = LOW
Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED

TRUTH TABLE

Block Diagram and Pin Number Functions CμL 9959

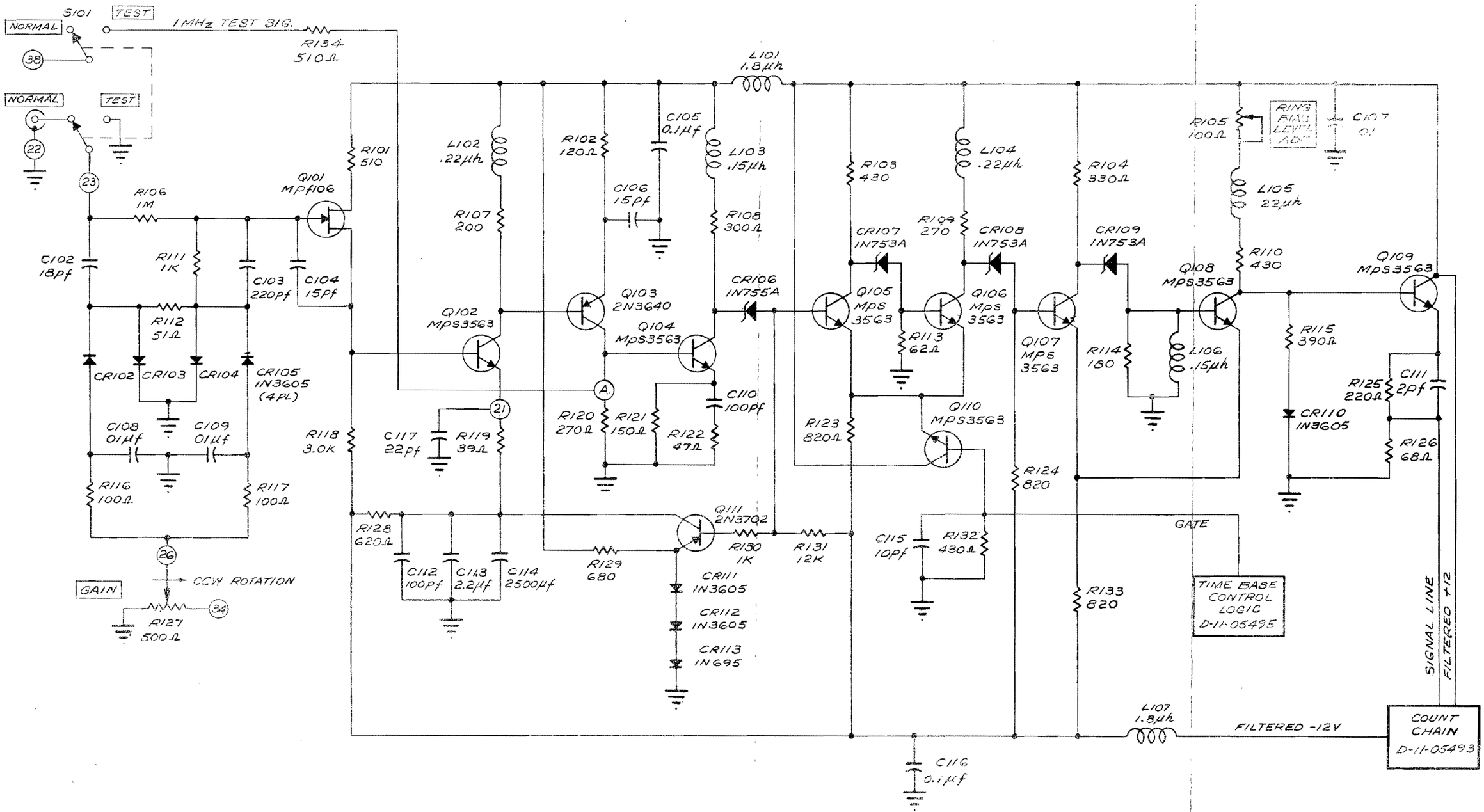


2
⊙=TEST POINTS

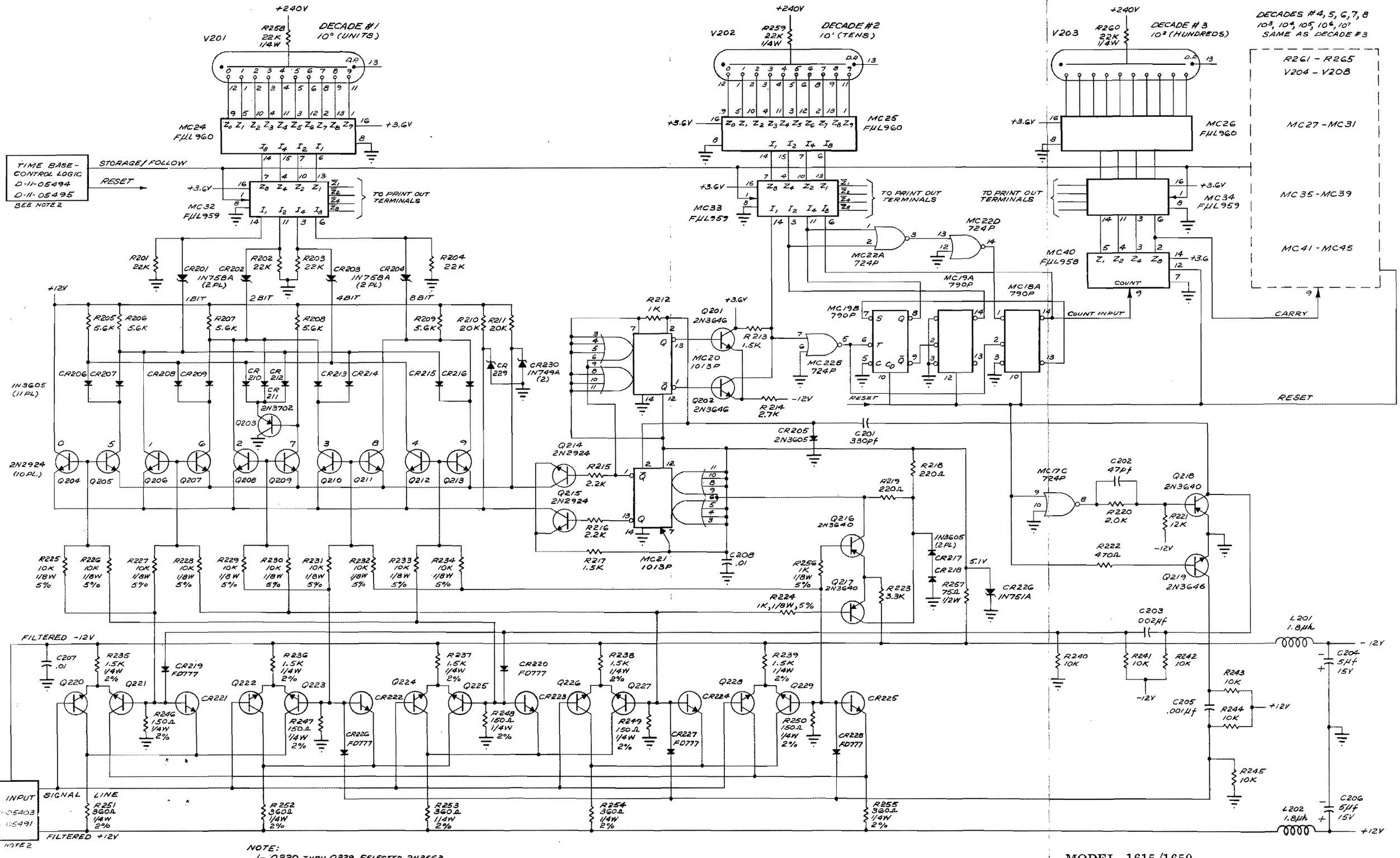
1=+3.6V
2=-12V
3=-5.2V
4=+12V
5=RESET
6=RING INPUT
7=+210V

INPUT CIRCUITS
Q101-Q111
COUNT CHAIN
& DISPLAY
Q201-Q229
CR221-CR225 =2N3646
MC17C, MC18-MC45
V201-V208
TIME BASE & CONTROL
OSC
Q1-Q4 & C1
TIME BASE
Q5-Q12
MC1-MC17, MC23
C6
POWER SUPPLY
Q1-Q7, Q9
R5, R7

MODEL 1615/1650
PCB COMPONENT LAYOUT



INPUT A SCHEMATIC
C-11-05491



NOTE:
1- Q220 THRU Q229 SELECTED 2N3563
CR221 THRU CR225 SELECTED 2N3646

2-C-11-05403 - MODEL 1650, C-11-05491 - MODEL 1615
D-11-05494 - MODEL 1650, D-11-05495 - MODEL 1615

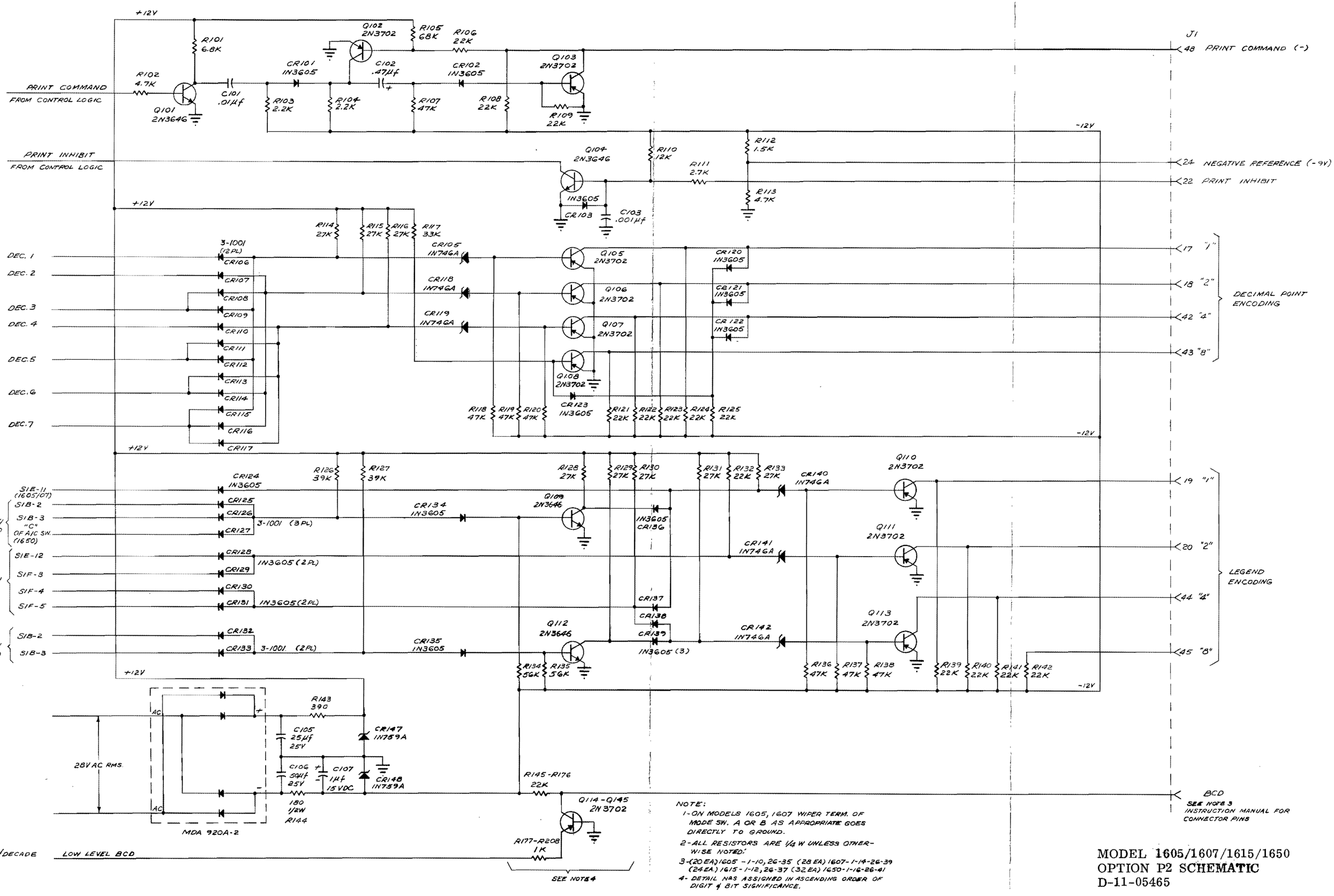
MODEL 1615/1650
COUNT CHAIN and DISPLAY SCHEMATIC
D-11-05493

MODEL 1615
CONTROL LOGIC and TIME BASE
SCHEMATIC D-11-05495

+12V
R101 6.8K
Q102 2N3702
R105 68K
R106 22K
CR101 IN3605
C102 47µf
CR102 IN3605
Q103 2N3702
PRINT COMMAND FROM CONTROL LOGIC
R102 4.7K
C101 01µf
R103 2.2K
R104 2.2K
R107 47K
R108 22K
R109 22K
Q101 2N3646
J101
48 PRINT COMMAND (-)
-12V
PRINT INHIBIT FROM CONTROL LOGIC
Q104 2N3646
R110 12K
R111 2.7K
R112 1.5K
R113 4.7K
1N3605 CR103
C103 .001µf
24 NEGATIVE REFERENCE (-9V)
22 PRINT INHIBIT
+12V
R114 27K
R115 27K
R116 27K
R117 33K
3-1001 (12PL)
DEC. 1
DEC. 2
DEC. 3
DEC. 4
DEC. 5
DEC. 6
DEC. 7
CR106
CR107
CR108
CR109
CR110
CR111
CR112
CR113
CR114
CR115
CR116
CR117
CR105 IN746A
CR118 IN746A
CR119 IN746A
Q105 2N3702
Q106 2N3702
Q107 2N3702
Q108 2N3702
CR120 IN3605
CR121 IN3605
CR122 IN3605
CR123 IN3605
R118 47K
R119 47K
R120 4.1K
R121 22K
R122 22K
R123 22K
R124 22K
R125 22K
17 "1"
18 "2"
42 "4"
43 "8"
DECIMAL POINT ENCODING
-12V
+12V
R126 39K
R127 39K
CR124 IN3605
CR125
CR126
CR127
3-1001 (3PL)
SIE-11 (1605/1607)
SIB-2
SIB-3
"C" OF A/C SW. (1650)
SIE-12
SIF-3
SIF-4
SIF-5
CR128
CR129
IN3605 (2PL)
CR130
CR131
IN3605 (2PL)
SIB-2
SIB-3
CR132
CR133
3-1001 (2PL)
CR134 IN3605
CR135 IN3605
Q109 2N3646
R128 27K
R129 27K
R130 27K
R131 27K
R132 22K
R133 27K
IN3605 CR136
CR137
CR138
CR139
IN3605 (3)
Q112 2N3646
R134 5GK
R135 5GK
CR140 IN746A
CR141 IN746A
CR142 IN746A
Q110 2N3702
Q111 2N3702
Q113 2N3702
R136 47K
R137 47K
R138 47K
R139 22K
R140 22K
R141 22K
R142 22K
19 "1"
20 "2"
44 "4"
45 "8"
LEGEND ENCODING
-12V
+12V
R143 390
28V AC RMS.
AC
C105 25µf 25V
C106 5µf 25V
C107 1µf 15VDC
CR147 IN759A
CR148 IN759A
180 1/2W R144
MDA 920A-2
R145-R176 100Ω
SEE NOTE 4
BCD
SEE NOTE 3 & FIG. 2.2 OF INSTRUCTION MANUAL FOR CONNECTOR PINS
1/DECADE
LOW LEVEL BCD

NOTE:
1- ON MODELS 1605, 1607 WIPER TERM. OF MODE SW. A OR B AS APPROPRIATE GOES DIRECTLY TO GROUND.
2- ALL RESISTORS ARE 1/4W UNLESS OTHERWISE NOTED.
3- (20 EA) 1605 - 1-10, 26-35 (28 EA) 1607 - 1-14-26-39 (24 EA.) 1615 - 1-12, 26-37 (32 EA) 1650 - 1-16-26-41
4- DETAIL NOS ASSIGNED IN ASCENDING ORDER OF DIGIT & BIT SIGNIFICANCE.

MODEL 1605/1607/1615/1650
OPTION P1 SCHEMATIC
D-11-05466



NOTE:

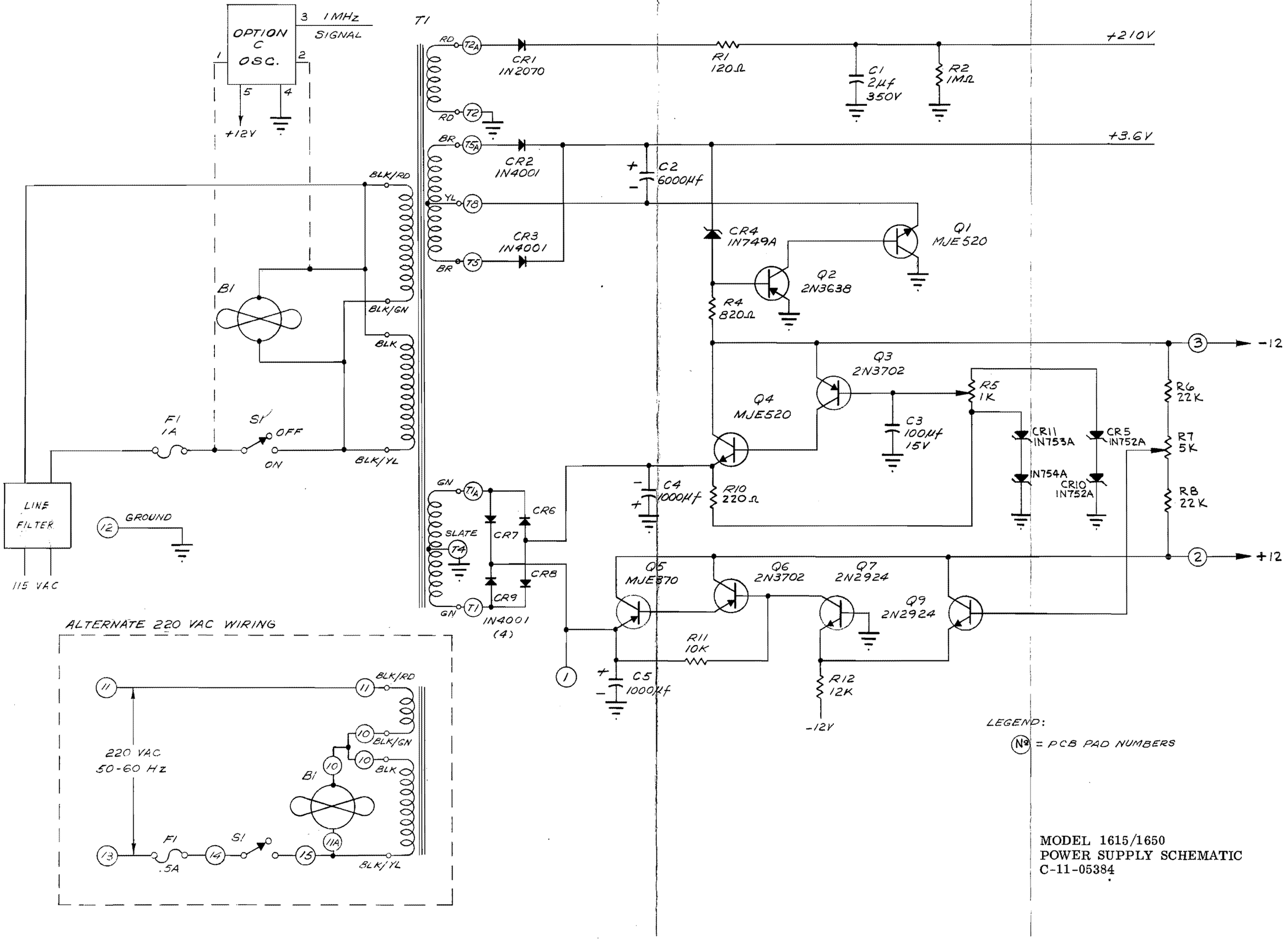
1- ON MODELS 1605, 1607 WIPER TERM. OF MODE SW. A OR B AS APPROPRIATE GOES DIRECTLY TO GROUND.

2- ALL RESISTORS ARE 1/4 W UNLESS OTHERWISE NOTED.

3- (20 EA) 1605 - 1-10, 26-35 (28 EA) 1607 - 1-14-26-39 (24 EA.) 1615 - 1-12, 26-37 (32 EA) 1650 - 1-16-26-41

4- DETAIL NOS ASSIGNED IN ASCENDING ORDER OF DIGIT & BIT SIGNIFICANCE.

MODEL 1605/1607/1615/1650 OPTION P2 SCHEMATIC D-11-05465



MODEL 1615/1650
POWER SUPPLY SCHEMATIC
C-11-05384