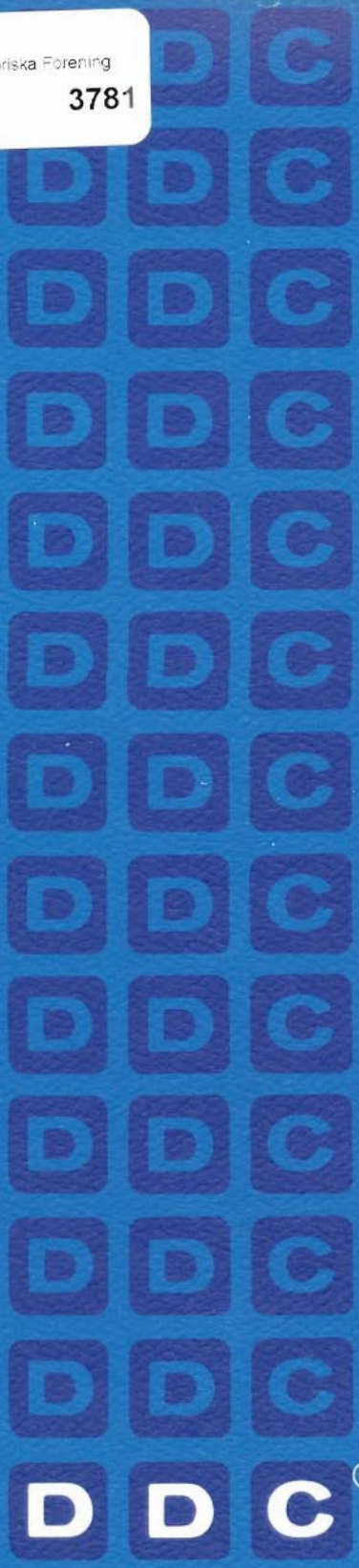


DDC®

ILC DATA DEVICE CORPORATION

105 Wilbur Place
Bohemia, New York 11716
516•567•5600, TWX 510•228•7324

Leader in Synchro Conversion • High-Speed, High-Accuracy D/A & A/D Conversion • Military Data Conversion Systems

INSTRUCTION MANUAL

FOR

DATA BUS ADAPTER

DBA-488-SR400

ILC DATA DEVICE CORPORATION

105 Wilbur Place, Bohemia, New York 11716
516•567•5600, TWX 510•228•7324

Leader in Synchro Conversion • High-Speed, High-Accuracy D/A & A/D Conversion • Military Data Conversion Systems

Rev. B. Effective 15 December 1981, with DBA-488 S/N 061

TABLE OF CONTENTS

SECTION 1. GENERAL DESCRIPTION

SECTION 2. FUNCTIONAL DESCRIPTION OF DBA-488

SECTION 3. DATA BUS ADAPTER DBA-488-SR400

TABLE OF CONTENTS (CONT'D.)

SECTION 3. DATA BUS ADAPTER DBA-488-SR400 (Cont'd.)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1

GENERAL DESCRIPTION

1.1 SCOPE OF MANUAL

Sections 1 and 2 of this instruction manual describe the DBA-488 Data Bus Adapter (figure 1-1) manufactured by ILC Data Device Corporation, Bohemia, N. Y. Section 3 covers the DBA-488-( ), the combination of the DBA-488 with one of DDC's synchro instruments (e.g., the DBA-488-SR103, DBA-488-SR400, DBA-488-SR202).

1.2 PURPOSE OF THE DBA-488 DATA BUS ADAPTER

The DBA-488 links DDC's synchro instruments to any programmable measurement instrument system, such as computer controlled automatic test equipment (ATE) or process control system, that operates from the IEEE-488-1975 General Purpose Interface Bus. Operation of the DBA-488 is also fully compatible with the Hewlett-Packard HP-IB bus without programming changes. Highlights of the IEEE-488-1975 bus are included for reference in later paragraphs.

Figure 1-1. DBA-488 Data Bus Adapter

1.3 PHYSICAL DESCRIPTION

The DBA-488 is configured as a fully enclosed flat rectangular assembly 8.1" X 6.1" X 1.7" (20.6 X 15.6 X 4.3 cm) that weighs less than 2-1/2 lbs (1.1 kg). Four holes in the lips of the cover facilitate mounting. Two interface connectors, one for the IEEE-488 General Purpose Interface Bus (GPIB) and the other for the associated instrument, are mounted on one side of the unit. Eight externally accessible miniature address select rocker switches are located between the two connectors.

1.4 THE IEEE-488 GPIB

The following abbreviated description of the IEEE-488 GPIB is included for reference. For complete bus details, consult IEEE Standard 488-1975 Digital Interface for Programmable Instrumentation. Copies of IEEE 488-1975 may be purchased from IEEE (Institute of Electrical and Electronics Engineers) or from the American National Standards Institute, both of which are located in New York, N. Y.

1.4.1 BASIC STRUCTURE AND CONSTRAINTS

The IEEE bus is a byte-serial bit-parallel interface system. It is structured with 16 lines consisting of the following:

a. Eight data bus lines for transmission of ASCII characters. Data is asynchronous and generally bidirectional.

b. Five bus management (control) signal lines.

c. Three data byte transfer control lines (handshake).

The system includes constraints on the number of devices, data rate, total transmission length, and is confined to exchange of digital data.

1.4.2 BASIC BUS TERMINOLOGY

a. Controller - A device that can address other devices to listen or to talk.

b. Listener - A device that can be addressed through the bus to receive messages from another device or the controller via the bus.

c. Talker - A device that can be addressed through the bus to transmit messages to another device or the controller via the bus.

NOTE

Controller, listener, and talker capabilities may occur individually and collectively in devices interconnected by the IEEE bus. (See fig. 1-2.)

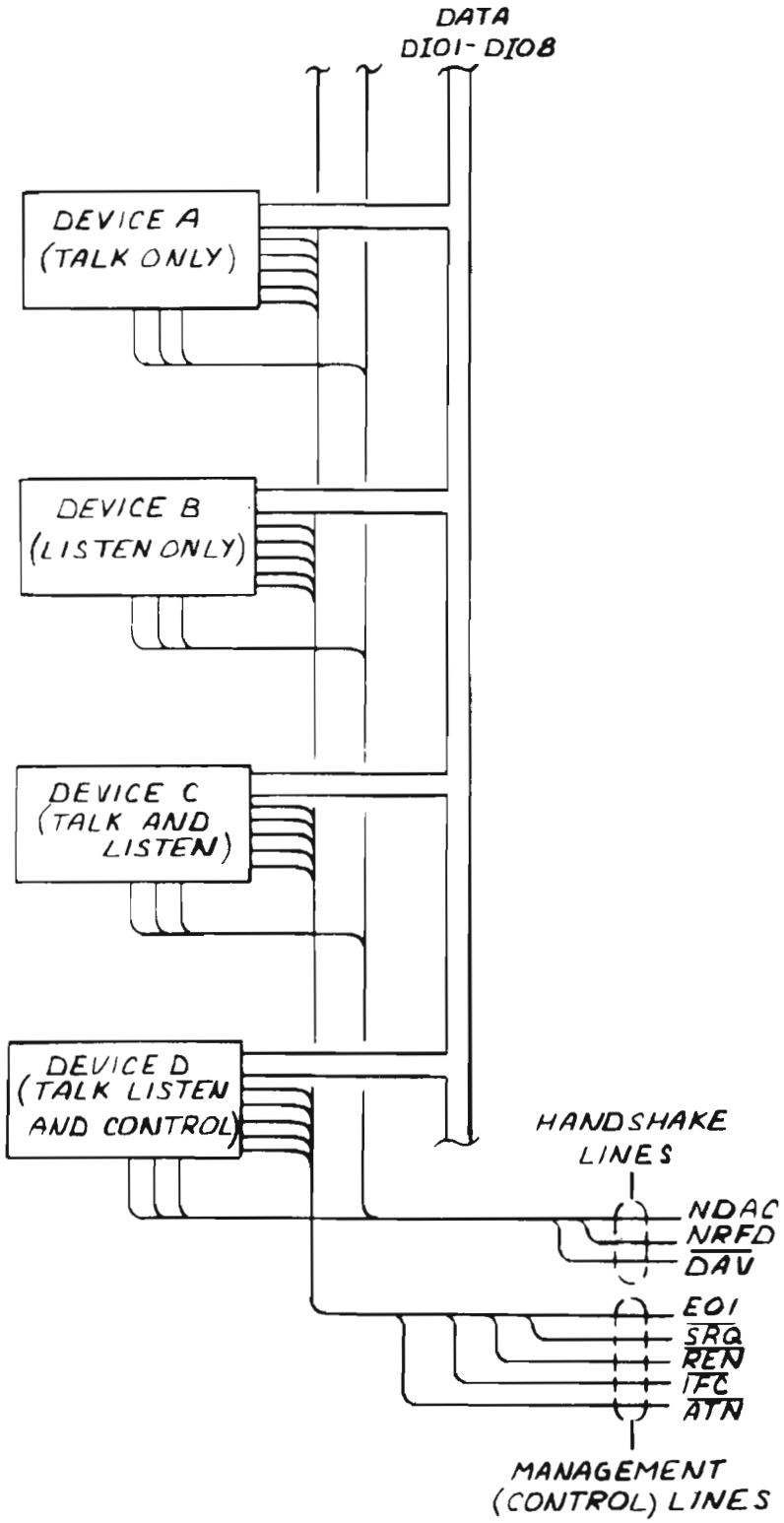


Figure 1-2. Interface Connections and Bus Structure

1.4.3 INTERFACE BUS SIGNALS

NOTE

The IEEE Standard 488-1975 is defined for a negative logic format:

Logic 0 = False = High ($\geq$2.0V)
Logic 1 = True = Low ($\leq$0.8V)

a. EOI (End or Identify). True level on this bus management (control) line indicates end of multiple byte transfer. When used with ATN, performs parallel polling sequence.

b. SRQ (Service Request). Device sets this control line true when it requires service from the interface controller.

c. REN (Remote Enable). This controller driven line is used with other messages to select source of device programming data (e.g., front panel or interface control).

d. IFC (Interface Clear). This controller driven line is set true to place all bus-connected devices in their idle states.

e. ATN (Attention). This control line specifies how data on the data lines are to be interpreted and which devices must respond to the data. When ATN is true, the DI01-DI08 lines carry addresses or commands. When ATN is set false, the data lines carry data.

f. NDAC (Not Data Accepted). When set false by a device, this handshake line indicates that data has been accepted.

g. NRFD (Not Ready for Data). When set false by a device, this handshake line indicates that the device is ready to accept data.

h. DAV (Data Valid). When set true, this handshake line indicates that information on the data lines is available and valid.

i. DI01-DI08 (Data Input-Output). These lines carry data in bit-parallel, byte-serial form. Information on the lines represents either address/commands or data, depending on the logic state of the ATN line.

j. Unlisten Command. This command is transmitted on the data lines in conjunction with ATN true to terminate the device listen function.

k. Untalk Command. This command is transmitted on the data lines in conjunction with ATN true to terminate the device talk function.

1.4.4 REMOTE MESSAGE CODING

Table 1-1 shows the coding of some of the control messages transmitted on the IEEE bus. The 1 and 0 designations refer to the logic states (negative logic convention). X = don't care. A1-A5 specify the five address bits set within the device by the address select switches.

TABLE 1-1. MESSAGE CODING

Message	I/O Data								Handshake			Control				
	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DAV	NRFD	NDAC	ATN	EOI	SRQ	IFC	REN
ATN (Attention)	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X
Data Byte	D8	D7	D6	D5	D4	D3	D2	D1	X	X	X	X	X	X	X	X
DAV (Data Available)	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X
NRFD (Not Ready for Data)	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X
NDAC (Not Data Accepted)	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X
DCL (Device Clear)	X	Ø	Ø	1	Ø	1	Ø	Ø	X	X	X	X	X	X	X	X
End	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X
Go to Local	X	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X
Identify	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X
IFC (Interface Clear)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
MLA (My Listen Address)	X	Ø	1	A5	A4	A3	A2	A1	X	X	X	X	X	X	X	X
MTA (My Talk Address)	X	1	Ø	A5	A4	A3	A2	A1	X	X	X	X	X	X	X	X
REN (Remote Enable)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
SRQ (Service Required)	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X
Unlisten	X	Ø	1	1	1	1	1	1	X	X	X	X	X	X	X	X
Untalk	X	1	Ø	1	1	1	1	1	X	X	X	X	X	X	X	X

1.4.5 3-WIRE HANDSHAKE PROCEDURE

The 3-wire handshake procedure, repeated for each byte transferred from a source to one or more acceptors, ensures that each listener is ready to accept data, that the information on the data lines is valid, and that the data has been accepted by all listeners. The DAV line is controlled by the source (talker); the NDAC and NRFD lines are controlled by the acceptors (listeners).

Figure 1-3 illustrates the handshake cycle for a source and several acceptors.

a. Both source and acceptors start in a known state. The source initializes DAV to high (false, data not valid) and the acceptors initialize NRFD to low (true, none are ready for data) and NDAC to low (true, none have accepted the data).

b. The source checks that both NRFD and NDAC are not high, then places the first data byte on the DIO lines. (If both lines are sensed high, the error condition ends the procedure.)

c. When all acceptors are ready to accept the first data byte, NRFD goes high.

d. After data is settled and valid and the source has sensed NRFD high, it sets DAV low (data is valid).

e. The first acceptor sets NRFD low then accepts the first byte. The other receptors follow suit at their own rates.

f. Each acceptor sets NDAC high to indicate that it has accepted.

g. When NDAC is sensed high by the source (after all acceptors have accepted the data byte), it sets DAV high (data on DIO lines no longer valid). At this point, one data byte transfer has been completed.

h. Upon sensing DAV high, the acceptors set NDAC low.

i. Source and acceptor initial conditions are now reestablished and the next handshake cycle may be initiated.

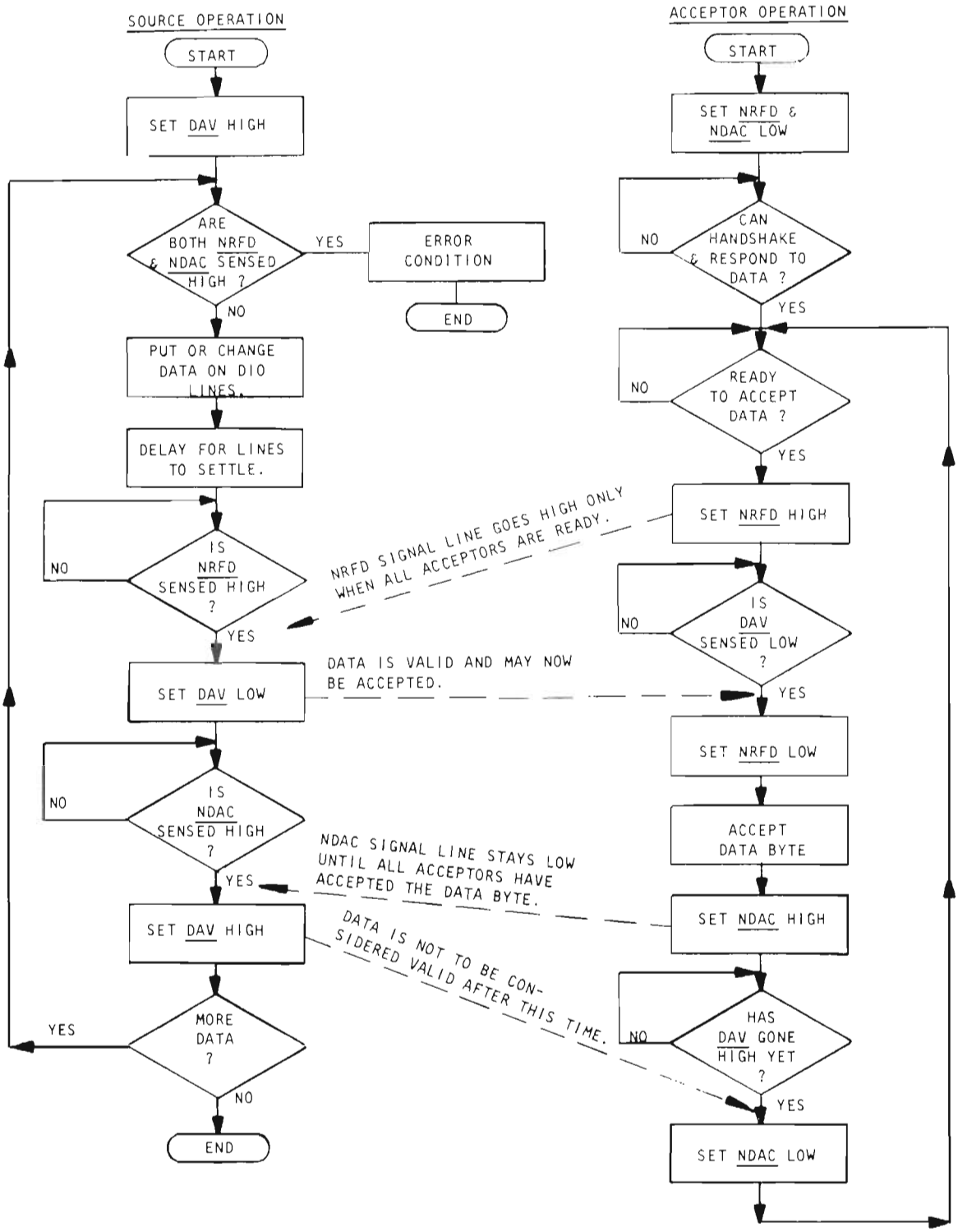


Figure 1-3. Handshake Timing Sequence

SECTION 2

FUNCTIONAL DESCRIPTION OF DBA-488

2.1 INTRODUCTION

This section provides a general functional description of the DBA-488, identifying the major input-output signals and covering basic signal flow. Detailed step-by-step operations within the DBA-488 are a function of the particular instrument and the stored program.

2.2 BLOCK DIAGRAM DESCRIPTION (See figure 2-1)

Operation of the DBA-488 is supervised by a self-contained microprocessor in accordance with a program stored in an erasable programmable ROM. Data transfer to and from the 16-line IEEE bus is mediated by the controller. The 32 input-output lines at the instrument interface are independently programmed, under microprocessor control, for input or output data transfer according to the requirements of the particular instrument connected to the DBA-488. The device address, preset manually by the user via the address select switches, is transferred to the controller memory at power turn-on.

2.3 FUNCTIONAL DESCRIPTION (See figure 2-2)

2.3.1 EQUIPMENT COMPLEMENT

The DBA-488 consists of four bus transceivers U1-U4, interface controller U5, microprocessor U6, tri-state buffers U7 and U8, ROM U9, and peripheral interface adapters (PIA's) U10 and U11. In addition, a low voltage power supply consisting of power transformer T1, bridge rectifier CRA1, and voltage regulator VR1 provides 5 volts DC for operating the unit.

2.3.2 TRANSCEIVERS U1 AND U2

Transceivers U1-U4 serve as the interface between the IEEE bus and the DBA-488 internal logic. Transceivers U1 and U2 are used for bus management and handshake signals; U3 and U4 accommodate the eight data lines. Logic levels applied to the four transmit-receive inputs of each quad transceiver from controller U5 determine which section behaves as a bus driver or receiver for the associated bus line. The T/$\overline{R}$ control for $\overline{SRQ}$ is always wired high (transmit) while those for $\overline{REN}$, $\overline{IFC}$, and $\overline{ATN}$ are wired low (receive). The remaining signals are controlled by U5. The bus transceiver outputs meet all requirements of IEEE Std. 488-1975.

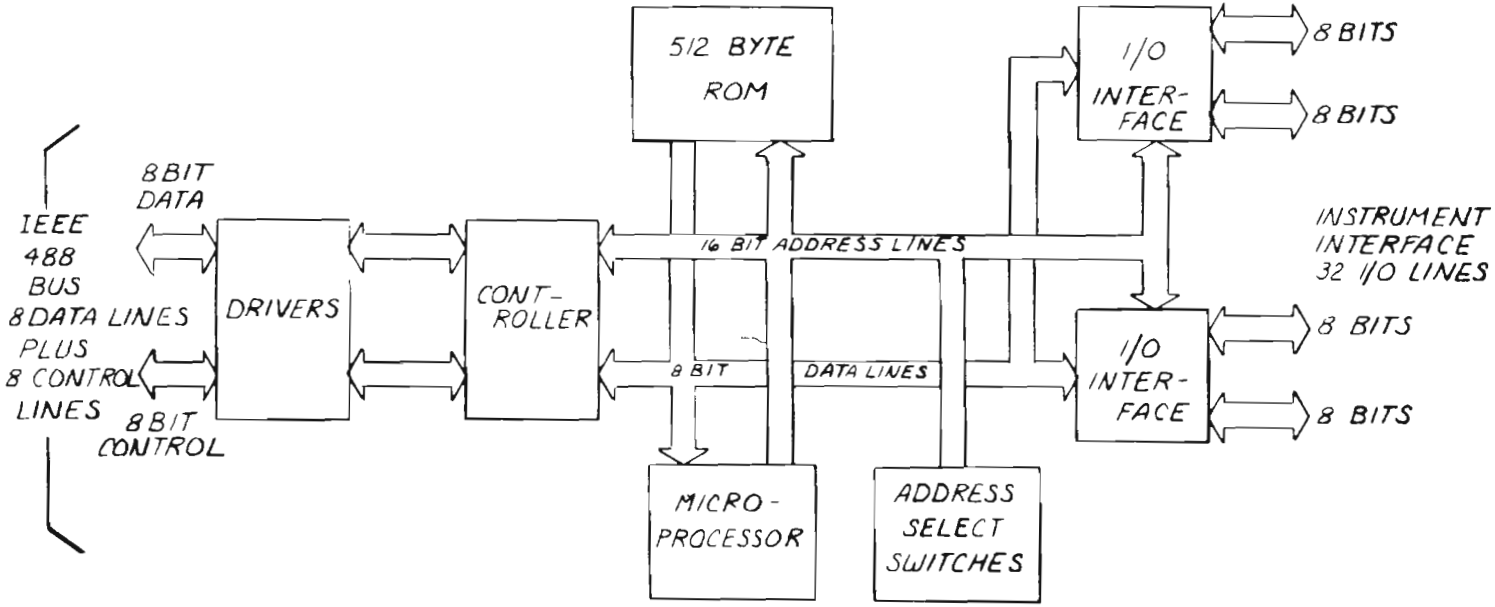


Figure 2-1. DBA-488, Block Diagram

2.3.3 INTERFACE CONTROLLER U5

Under the direction of microprocessor U6, interface controller U5 mediates the transfer of data between the DBA-488 and the IEEE bus. Controller U5 decodes messages from the IEEE bus, processes those directed to the DBA-488 and transfers messages to the internal data bus. It should be noted that, although the IEEE bus signals follow negative logic convention, positive logic is used within the DBA-488. (Thus, the signal NRFD from the IEEE bus is designated RFD at the input of U5.) The controller is equipped with internal registers that are selected by register select lines RS0, RS1, and RS2 and chip select $\overline{CS}$ (via microprocessor address bits A0, A1, and A2 and A14') in conjunction with the read/write (R/$\overline{W}$) signals and Ø2 clock from the microprocessor. The registers accommodate functions such as address, data in, data out, interrupt status, etc. Data transfer between U5 and U3/U4 is effected through the $\overline{IB}$Ø - $\overline{IB7}$ lines; the DBØ - DB7 lines carry data between U5 and the internal data bus. $\overline{CS}$ enables U5 and Ø2 is a timing signal provided by U6.

2.3.4 MICROPROCESSOR U6

The 8-bit microprocessor contains registers, accumulators, a 128 X 8 bit RAM and an internal clock. The 16-line address bus (AØ-A15) supervises the DBA-488 operations. The 8-line bidirectional data bus (DØ-D7) transfers data to and from memory and the peripheral devices. Clock pulses at pin E (Ø2) are used for timing. Upon receipt of an interrupt request ($\overline{IRQ}$) from controller U5 (upon U5's receipt of DCL on the data lines), U6 completes its current instruction then cycles through an interrupt sequence that resets the microprocessor. The read/write (R/$\overline{W}$) output of U6 controls the read/write status of controller U5 and PIA's U10 and U11.

2.3.5 ROM U9

Erasable programmable ROM U9 stores the DBA-488 program in its 512 X 8 bit memory. When enabled ($\overline{CS}$ input low) and strobed by a clock pulse from U6 (STR input), address bits AØ-A8 are decoded and data transfer is effected on the DOØ - DO7 lines.

2.3.6 PIA'S U10 AND U11

PIA's U10 and U11 interface the DBA-488 with the DDC instrument. Four 8-bit bidirectional data buses (PAØ - PA7 and PBØ - PB7) communicate with the instrument; an 8-bit bidirectional bus (DØ - D7) links the selected PIA's with the internal data bus. Each chip is selected by $\overline{CS2}$ low via a U6 address routed through tri-state buffer U8. Register select inputs (RSØ, RS1), controlled by microprocessor U6, accress registers within each PIA which provide functions such as data direction, control, peripheral interface, etc. PIA read/write operation is controlled by the R/$\overline{W}$ input from U6.

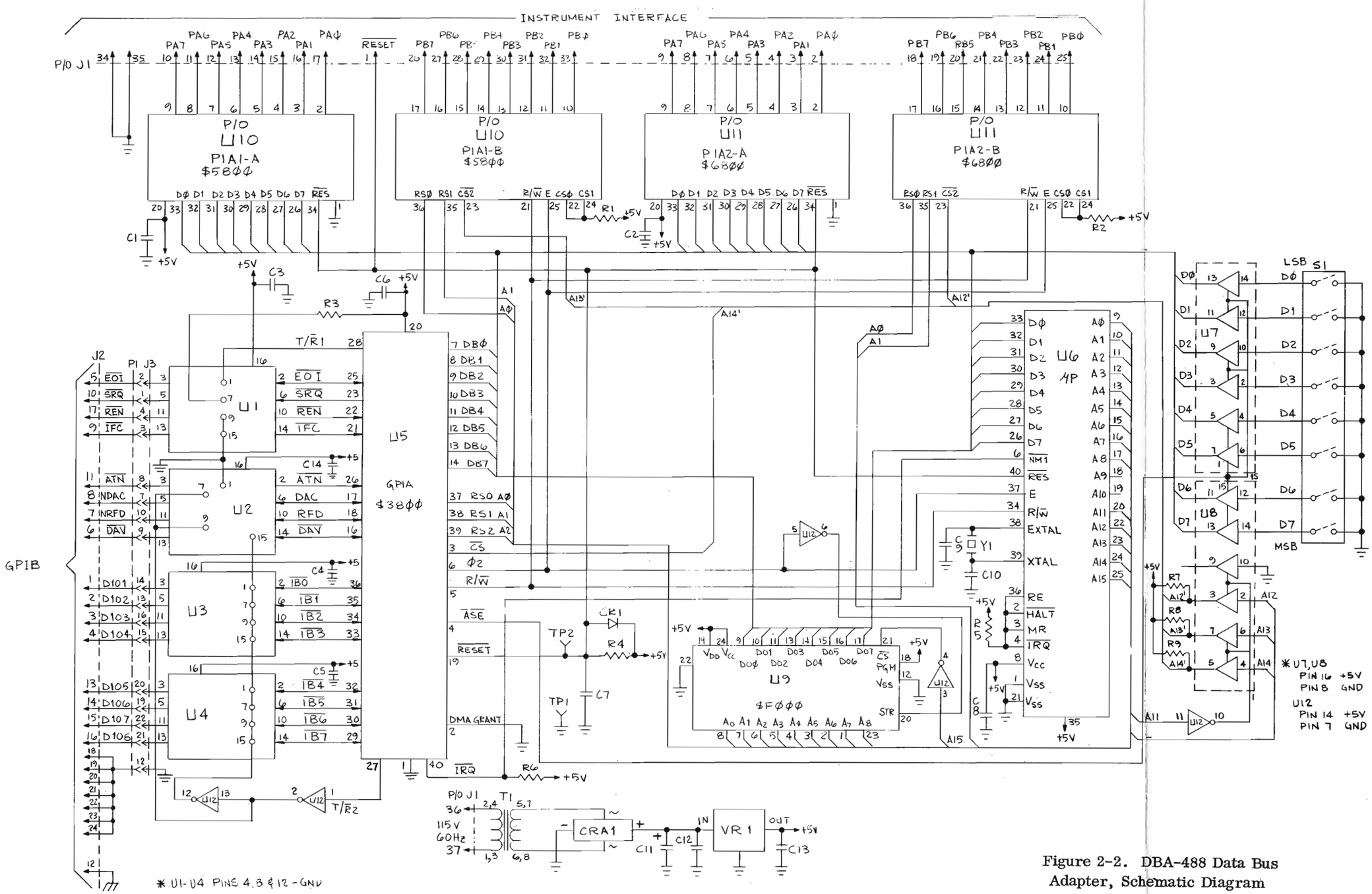


Figure 2-2. DBA-488 Data Bus Adapter, Schematic Diagram

2.3.7 POWER UP AND DEVICE ADDRESS

When power is applied to the DBA-488, the logic low level at test point TP2 (resulting from the uncharged state of C2) initializes U5, U10, U11 and U6. The $\overline{ASE}$ (address select) output of U5 drops, enabling the outputs of address switch S1. The five preset LSB's of S1, representing the primary device address, are then transferred into a register in controller U5, for subsequent use.

2.3.8 DATA TRANSFER

Controller U5 responds to the device address (applied via the data line inputs on the $\overline{IB}$ lines) when the IEEE bus sets ATN true. Notified by U5 via the DB data lines, U6 addresses ROM U9 which determines if talk or listen operation is required. If the talk mode is selected, U6 enables PIA's U10 and U11 and causes data from the instrument to be transferred through the PIA's to controller U5 which transfers the data through the $\overline{IB}$ lines to U3 and U4. These buffers, enabled by a T/$\overline{R}$2 level from U5, transfer the required data to the IEEE bus. Transmission of the individual data bytes is accomplished in proper sequence as a function of the handshake procedure. The bus management lines ($\overline{ATN}$, $\overline{IFC}$, $\overline{SRQ}$, $\overline{EOI}$ and $\overline{REN}$) insure that information flows through the interface lines in orderly fashion. When the last data bytes (ASCII carriage return/line feed) are transmitted, the DBA-488 sets $\overline{EOI}$ true to signal the end of the data transfer. This feature permits compatible operation of the DBA-488 with the HPIB system. The entire sequence is terminated by an Untalk command from the controller.

When the DBA-488 listen address is received, data applied to U3 and U4 is transferred to controller U5. The microprocessor then transfers the data from U5 to the PIA's which pass the information to the instrument. An $\overline{EOI}$ or carriage return/line feed is received to indicate the end of the data transfer and the listen sequence is terminated by an Unlisten command.

SECTION 3

DATA BUS ADAPTER DBA-488-SR400

3.1 EQUIPMENT SUPPLIED

3.1.1 DBA-488 ORDERED WITH SR-400

When the DBA-488 is ordered together with an SR-400 Synchro/Resolver Simulator, the DBA-488 is bracket mounted at the rear of the SR-400 and both units are electrically interconnected through a cable. (See figure 3-1.) AC power is applied to the DBA-488 when the SR-400 is turned on. The only component not supplied is the standard mating connector to the IEEE bus.

3.1.2 DBA-488 ORDERED SEPARATELY

When a DBA-488 is ordered separately (for retrofit to an SR-400), a mating connector for the instrument interface is supplied but is not wired. The standard mating connector for the IEEE bus is not supplied. Mounting hardware is included, as required.

The DBA-488 is not equipped with a power switch. Line voltage (115 volts at 60 Hz) is applied via the instrument interface connector. If the SR-400 front panel POWER switch is to control the DBA-488, this switch must be wired to pins on the instrument. This requires a modification to the SR-400, as shown in table 3-1.

NOTE

The DBA-488 may be ordered for operation from 220 volts, 50/60 Hz.

3.2 UNPACKING

Carefully remove the equipment from the packaging material and inspect for possible damage. Should any unit show signs of damage, notify the nearest ILC Data Device Corporation field representative immediately.

3.3 INTERCONNECTIONS

Table 3-1 shows the interconnections between the DBA-488 and SR-400 and indicates the function of each lead. For SR-400 units being retrofitted, switched AC line voltage (115 volts) may be wired to pins 39 and 40 of instrument connector J2. Connect pin 39 of J2 to the switched terminal of POWER switch S8 and pin 40 to pin L of instrument connector J1. The interconnecting cable must be wired as shown in table 3-1.

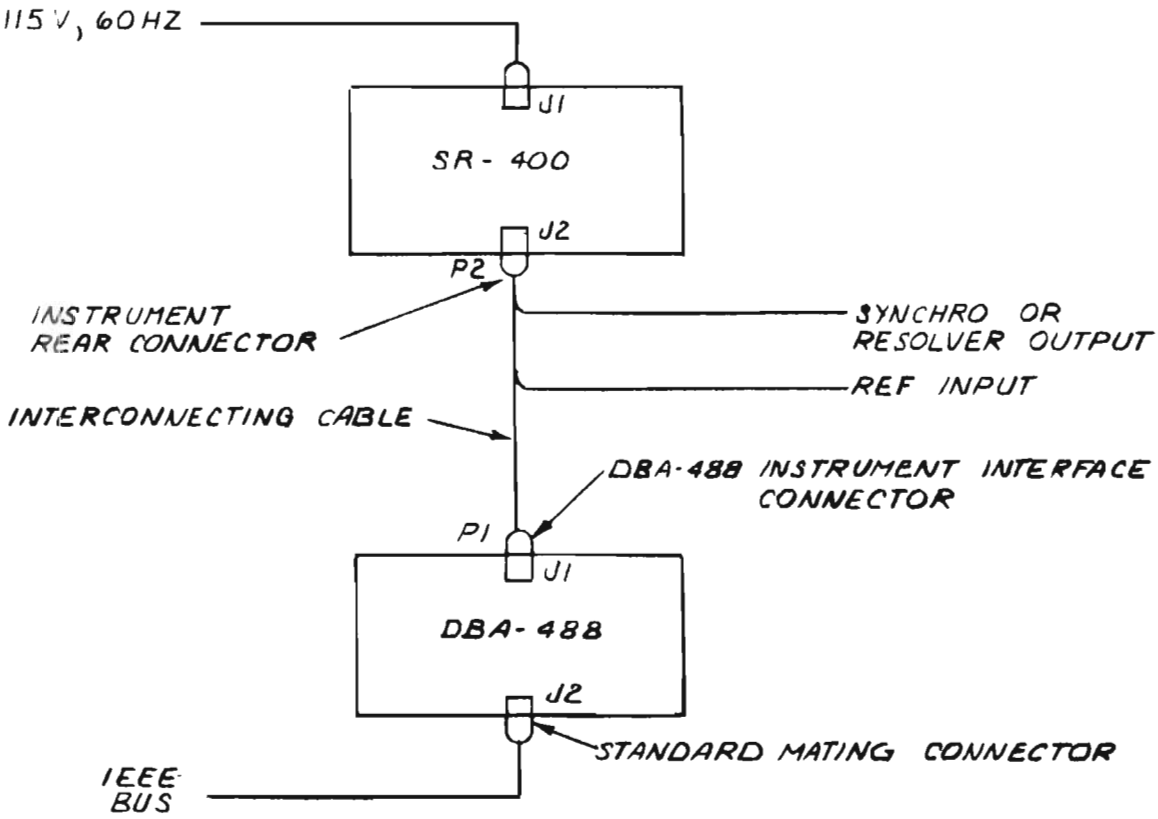


Figure 3-1. DBA-488-SR400 Connection Diagram

3.4 SETTING THE PRIMARY DEVICE ADDRESS

The five LSB's of the eight ADR SELECT switches on the DBA-488 determine the device address. Set these switches to the required bus address, LSB to MSB, as marked before applying power.

3.5 OPERATING PROCEDURE

Once the SR-400 is connected as shown in figure 3-1, it is only necessary to depress the REMOTE pushbutton and the POWER switch on the SR-400 front panel. The SR-400 resolver or synchro output should track the digital input angle applied from the IEEE bus via the DBA-488. The LED display will indicate the angular values. To turn off both the SR-400 and DBA-488, depress the POWER pushbutton on the SR-400.

3.6 COMMAND CODES

When operating from the IEEE bus, the SR-400 is controlled by bus commands applied via the DBA-488. Table 3-2 lists the codes applicable to the SR-400. Each command is ASCII encoded and applied to the DBA-488 via the bus data lines. When addressed to listen, the unit responds to the commands.

3.7 CONTROL WORD OR DATA COMMAND SEQUENCE (LISTEN)

Figure 3-2 depicts the operations that occur when the bus controller transmits control words or data to the DBA-488-SR400.

a. Controller sets ATN (Attention) line to true.

b. Controller transmits SR-400 listen address (MLA) on the data lines. When control words are to be transmitted, the LSB is set true; when data is to be transferred, the LSB is set false.

c. Controller returns ATN to false.

d. Controller (or device activated by controller) transmits ASCII encoded control words or data on the data lines.

e. Controller (or other device) signals end of transmission by transmitting an ASCII carriage return/line feed on the data lines or by setting EOI line to true with the last data byte.

f. Controller sets ATN line to true.

g. Controller transmits an Unlisten command on the data lines.

TABLE 3-1

DBA-488 TO SR-400 CONNECTIONS

DBA-488 INSTRUMENT INTERFACE CONNECTOR	FUNCTION	INSTRUMENT REAR CONNECTOR
1	$\overline{\text{Reset}}$	---
2	Internal Connection	---
3	Internal Connection	---
4	Internal Connection	---
5	Internal Connection	---
6	100°	33
7	200°	17
8	Internal Connection	---
9	Internal Connection	---
10	$.8^{\circ}$	30
11	$.4^{\circ}$	47
12	$.2^{\circ}$	13
13	$.1^{\circ}$	29
14	$.08^{\circ}$	46
15	$.04^{\circ}$	12
16	$.02^{\circ}$	28
17	$.01^{\circ}$	45
18	Internal Connection	---
19	Internal Connection	---
20	Synchro/Res Select	1
21	Strobe	6
22	Lamp Test	26
23	Internal Connection	---
24	Input Level Control 2	42

TABLE 3-1 (CONT'D.)

DBA-488 TO SR-400 CONNECTIONS

DBA-488 INSTRUMENT INTERFACE CONNECTOR	FUNCTION	INSTRUMENT REAR CONNECTOR
25	Input Level Control 1	41
26	80°	50
27	40°	16
28	20°	32
29	10°	49
30	8°	15
31	4°	31
32	2°	48
33	1°	14
34	Gnd	9
35	Gnd	9
36	Power Hi	39*
37	Power Lo	40*
38-50	Spare	---

*Switched AC line voltage may be wired to these pins from the power switch on the instrument front panel.

3.8 MAINTENANCE

Maintenance of the SR-400 is described in the associated DDC instruction manual. Maintenance of the DBA-488 in the field is limited since its operations occur under control of the IEEE bus controller and the internal stored program. Check that the self contained power supply (T1, CR1A, VR1, and C11 through C13) is delivering +5 volts.

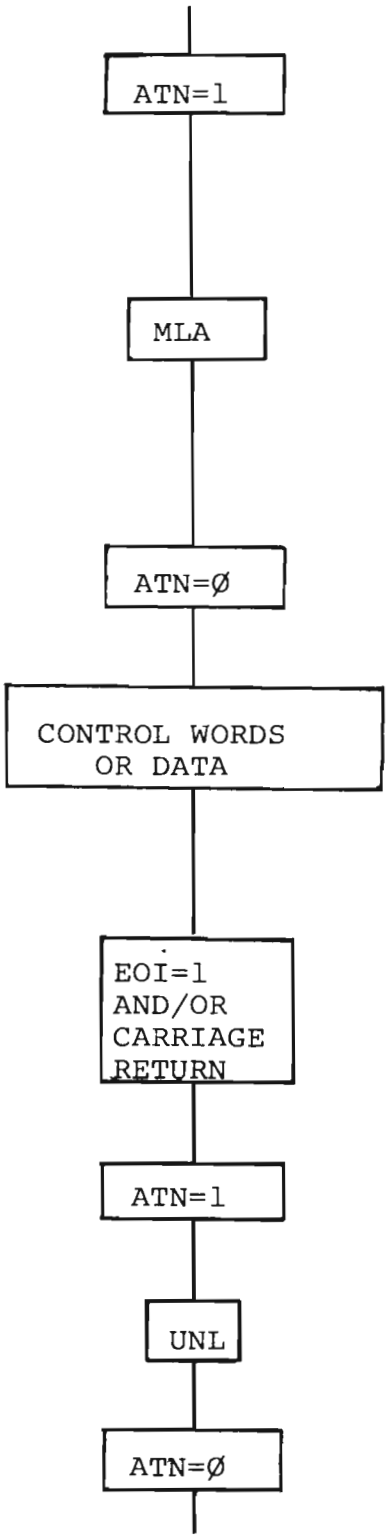
3.9 DBA-488 PARTS LIST

All DBA-488 parts are listed in table 3-3. Each part is identified by reference designation, part number, description and manufacturer. Location of parts on the printed circuit board is shown in figure 3-3.

TABLE 3-2

COMMAND CODE FUNCTIONS

Command Code	Function
P	Preset SR-400 output to 26V L-L.
1	Set output to 11.8V L-L.
2	Set output to 26V L-L.
9	Set output to 90V L-L.
S	Select synchro output.
R	Select resolver output.
I	Inhibit converter tracking.
F	Enable converter tracking of data input.
T	Test lamps.
D	Set display to read data.



Controller sets ATN (Attention) line to true.

Controller transmits device listen address on the data lines. For the SR-400 (SR-460) the LSB is set either to true to indicate that control words will be sent or to false to indicate that a data word will be sent.

Controller returns ATN line to false.

Controller (or another device activated by the controller) transmits ACCII encoded control words or data on the data lines.

Controller or other device signals end of transmission by setting EOI (End or Identify) line to true during the last word or command, or by transmitting a Carriage Return after the last word command.

Controller sets ATN line to true.

Controller transmits a UNL (unlisten) command on the data lines.

Controller returns ATN line to false.

Figure 3-2 "Listen" Command Sequence Flow Chart

ADDRESS SWITCH SETTING: S8 S7 S6 S5 S4 S2 S1

	DON'T CARE'S			LISTEN ADDRESS		WILL LISTEN REGARDLESS OF POSITION

TO SEND COMMANDS: EXAMPLE (SYNCHRO, 11.8V)

S = SYNCHRO, R = RESOLVER
1 = 11.8V, 2 = 26V, 9 = 90V LINE TO LINE
P = PRESET (SYNCHRO, 26V LINE TO LINE)

ASSERTED CONTROL LINES	DATA BUS INFORMATION							
	DI/08	DI/07	DI/06	DI/05	DI/04	DI/03	DI/02	DI/01
"ATN" (MY LISTEN ADDRESS)	0	0	1	S5	S4	S3	S2	0
(SENDING ASCII-S=SYNCHRO)	0	1	0	1	0	0	1	1
"EOI" (SENDING ASCII-1= 11.8V AND TERMINATING)	0	0	1	1	0	0	0	1
"ATN" (UNLISTEN)	0	0	1	1	1	1	1	1
OR CR (CARRIAGE RETURN)	0	0	0	0	1	1	0	1
LF (LINE FEED)	0	0	0	0	1	0	1	0

EXAMPLE: SENDING ANGLE 342.15 DEGREES

	DI/08	DI/07	DI/06	DI/05	DI/04	DI/03	DI/02	DI/01
"ATN" (M.L.A.)	0	0	1	S5	S4	S3	S2	0
(SEND DATA) MSB FIRST, ETC.								
3 (100)	0	0	1	1	0	0	1	1
4 (10)	0	0	1	1	0	1	0	0
2 (1)	0	0	1	1	0	0	1	0
1 (0.1)	0	0	1	1	0	0	0	1
5 (0.01)	0	0	1	1	0	1	0	1
"CR"	0	0	0	0	1	1	0	1
"LF"	0	0	0	0	1	0	1	0
"ATN" (UNLISTEN)	0	0	1	1	1	1	1	1

NOTE: LSB POSITION IS: "0" TO SEND DATA
"1" TO SEND COMMANDS

TABLE 3-3

DBA-488 PARTS LIST

Ref. Desig.	Part No.	Description	Manufacturer
C1-C6, C14	VK33	Capacitor, .01 uf, 20%	
C7	VK33	Capacitor, 0.47 uf, 10%	
C8, C12, C13	VK33	Capacitor, 0.1 uf, 20%	
C9, C10	VK23	Capacitor, 27 pf, 10%	
C11	39D	Capacitor, 8000 uf @ 15V	Sprague
CRA1	VH-148	Rectifier, bridge	Varo
CR1	1N4148	Diode	
J1	205869-1	Connector	Amp
R1-R3, R7-R9	RCR07	Resistor, 2.2K, 1/4W, 5%	
R4	RCR07	Resistor, 110K, 1/4W, 5%	
R5, R6	RCR07	Resistor, 5.1K, 1/4W, 5%	
S1	76PB08	Switch, Dip	Grayhill
T1	LP16-700	Transformer	Signal
U1-U4	MC3448AP	Bus Transceiver	Motorola
U5	MC68488P	Interface Controller	Motorola
U6	MC6802P	Microprocessor	Motorola
U7, U8	70L97N	Tri-State Buffer	National
U9	IM6604IJG	Read Only Memory	Intersil
U10, U11	MC6821P	Peripheral Interface Adapter	Motorola
U12	7404	Inverter Driver	Texas Instrument
VR1	UA7805	Voltage Regulator	Fairchild
Y1	SCM-18(4MHz)	Crystal	Sentry
	C22933	Printed Circuit Board	DDC
	C22934*	Printed Circuit Board Assy	DDC

* Specify " C22934 for SR-400 " or SR-460

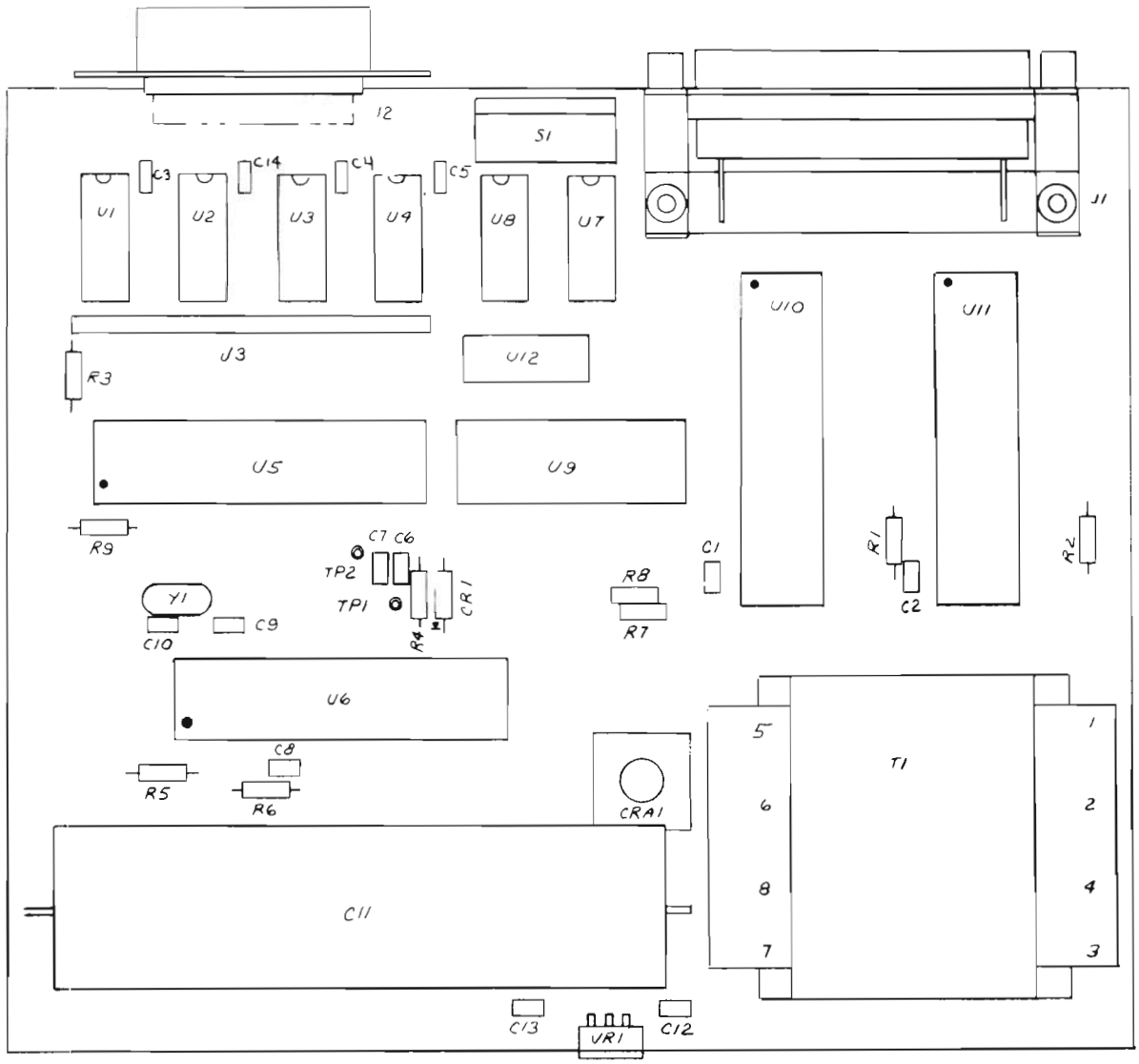


Figure 3-3. DBA-488, Location of Parts