ELLIOTT

PROCESS COMPUTING DIVISION

Issued by:—

MINILOG DIVISION

Elliott Brothers (London) Limited, Elstree Way, Borehamwood, Herts.

Telephone: Elstree 2040

MINILOG DESIGN BULLETINS

INDEX

(ISSUE 5)

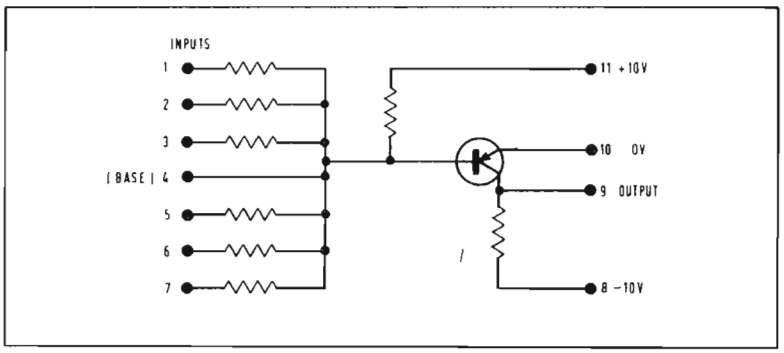
ELEMENT TYPE 1 (Mk11)

This unit performs a 6 way "inverted and" function on up to 6 inputs.

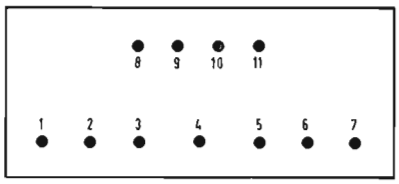
OUTPUT: The output will drive up to 5 logic loads.

INPUT: Each input imposes a load of 1 logic load.

CIRCUIT:



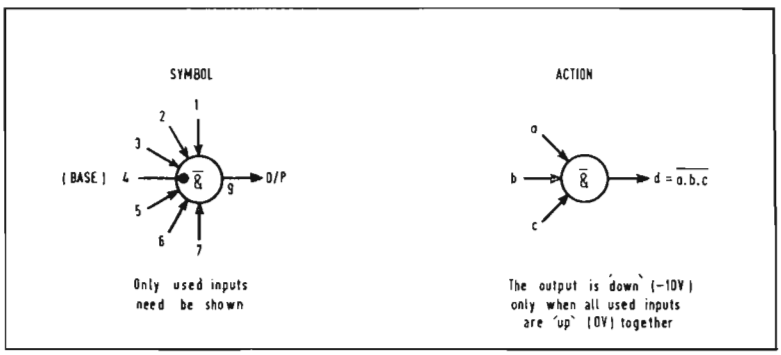
CONNECTIONS: (View looking at leads)



POWER REQUIREMENTS: +10V: 0.1 mA. Voltage Tolerance ±10%. Max. ripple: 100mV p-p.
−10V: 6.7 mA. Voltage Tolerance ±10%. Max. ripple: 10mV p-p.

TEMPERATURE RANGE: 5°C to 45°C.

LOGIC:



DIMENSIONS: 2″ x 0.85″ x 0.625″ deep.

LEADS: 11 off 0.032″ dia. tinned copper wire ⅜″ long.

THE ELEMENT IS FULLY ENCAPSULATED.

(ISSUE 5)

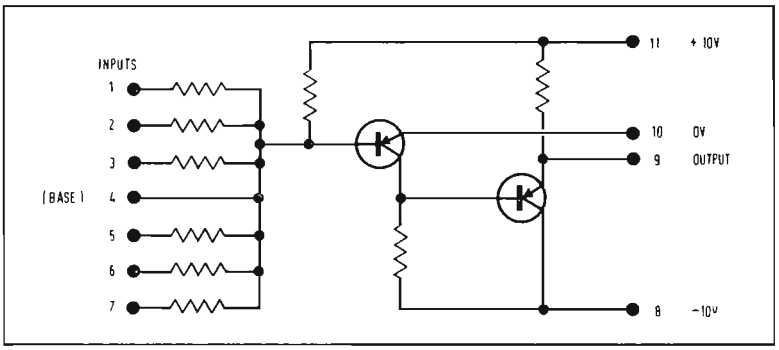
ELEMENT TYPE 2 (MkII)

This unit performs a 6 way "inverted and" function on up to 6 inputs.

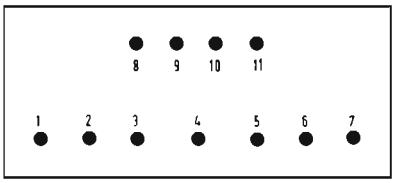
OUTPUT: The output will drive up to 25 logic loads.

INPUT: Each input imposes a load of 1 logic load.

CIRCUIT:



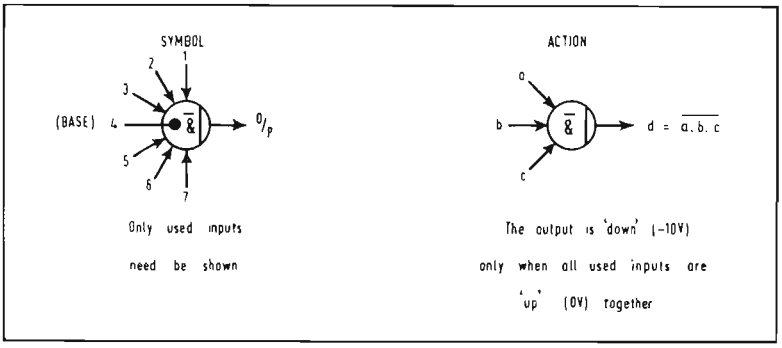
CONNECTIONS: (View looking at leads)



POWER REQUIREMENTS: +10V: 3.1 mA. Voltage Tolerance ± 10%. Max. ripple: 100mV p-p.
−10V: 2.1 mA. Voltage Tolerance ± 10%. Max. ripple: 10mV p-p.

TEMPERATURE RANGE: 5°C to 45°C.

LOGIC:



DIMENSIONS: 2″ x 0.85″ x 0.625″ deep.

LEADS: 11 off 0.032″ dia. tinned copper wire ⅜″ long.

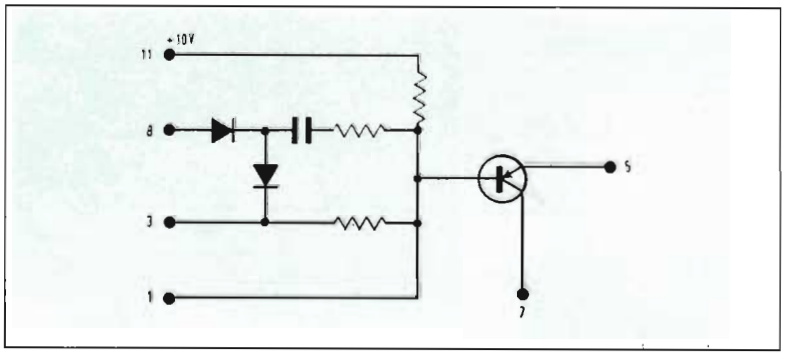
THE ELEMENT IS FULLY ENCAPSULATED.

(ISSUE 5)

ELEMENT TYPE 3 (MkII)

This element is a power drive for solenoids, relays etc. and may be used to drive loads individually or in conjunction with other elements in a matrix.

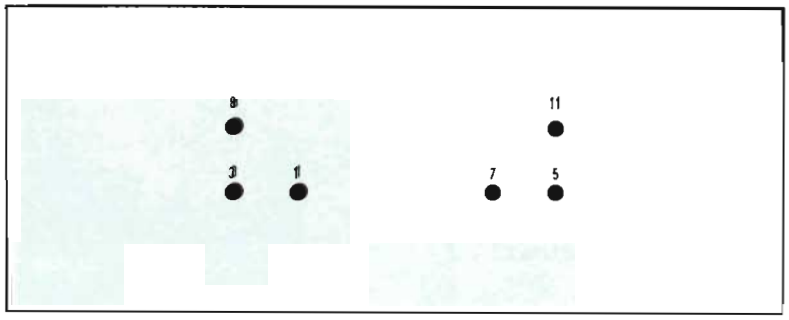
CIRCUIT:



POWER REQUIREMENTS: +10V: 12mA.
Temperature Range 5° to 45°C.

ACTION: Minilog type 3 simulates an on/off switch with one terminal permanently earthed. It may be used to switch a maximum current of 1A at a voltage up to BUT NOT EXCEEDING —50V.

CONNECTIONS:



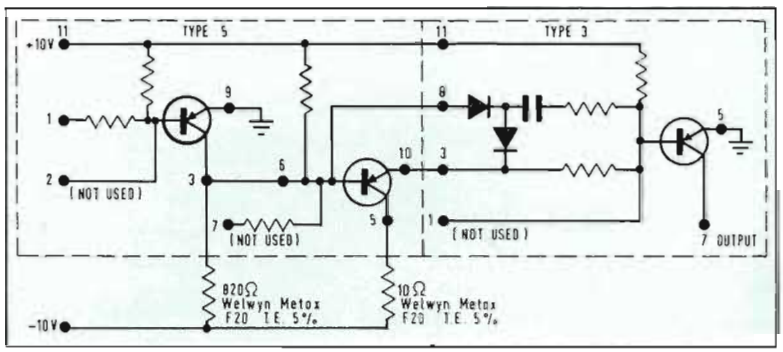
(View looking at leads) Actual size $4\frac{3}{4}'' \times 1\frac{7}{8}''$

P.T.O.

DIMENSIONS: $1\frac{7}{8}$ in. $\times 4\frac{3}{4}$ in. $\times \frac{13}{32}$ in. approximately.
(4.75cm $\times$ 12.21cm $\times$ 1.03cm) approximately.

APPLICATION: To drive any load rated at up to 1A the type 3 Minilog MUST be driven by a Minilog type 5 element.

CIRCUIT:

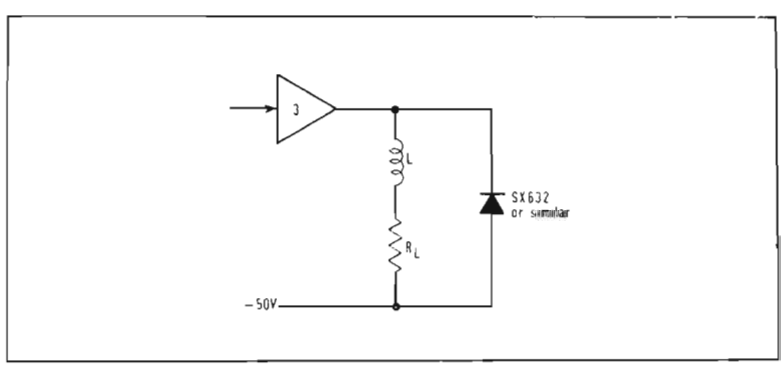


Full details of Minilog type 5 are given in Design Bulletin No. 16.

ACTION: The output transistor is switched off when the input to pin 1 is down (−10V).

NOTE: Precautions must be taken to ensure that the emitter-collector voltage does not exceed 50V. Transient voltage peaks must be eliminated by connecting a diode across the inductive load as shown. For 24V coils it is possible to de-energise in less time than the natural time-constant. An additional circuit is needed for this and will be given on request.

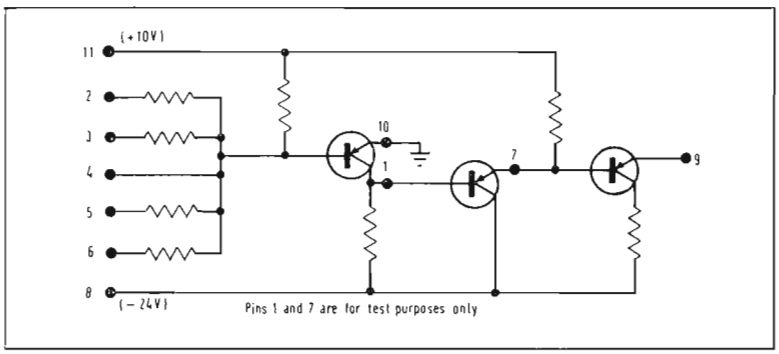
CIRCUIT:



ELEMENT TYPE 4 (Mk I I)

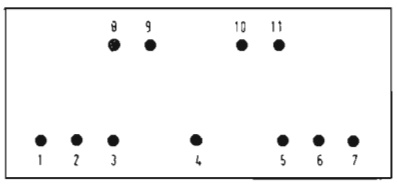
This element acts as a relay driver by switching a negative supply to one side of the relay (or inductive load).

CIRCUIT:



The load is connected between pin 9 and earth.

CONNECTIONS: (View looking at base)



P.T.O.

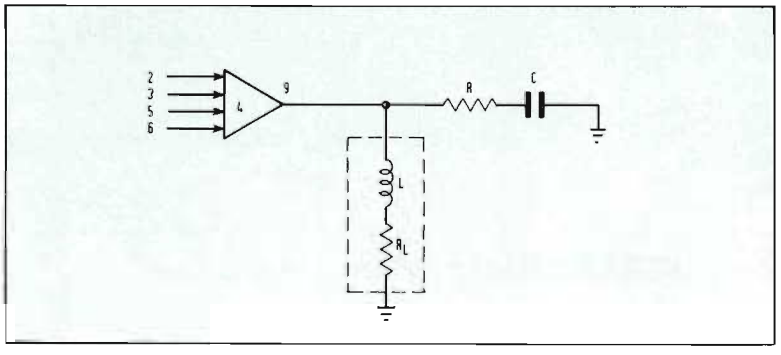
OUTPUT: The output will drive loads rated at up to 24V at 50mA.

POWER REQUIREMENTS: +10V; 6 mA.
−24V; 4 mA (excluding current taken by the relay)
Temperature range 5° to 45°C

ACTION: The load will be switched when ALL the inputs 2, 3, 5 and 6 are up (i.e. at 0V).

NOTE: It is important to employ resistance-capacitance protection. Values of R and C are given in Design Bulletin No. 17.

CIRCUIT:



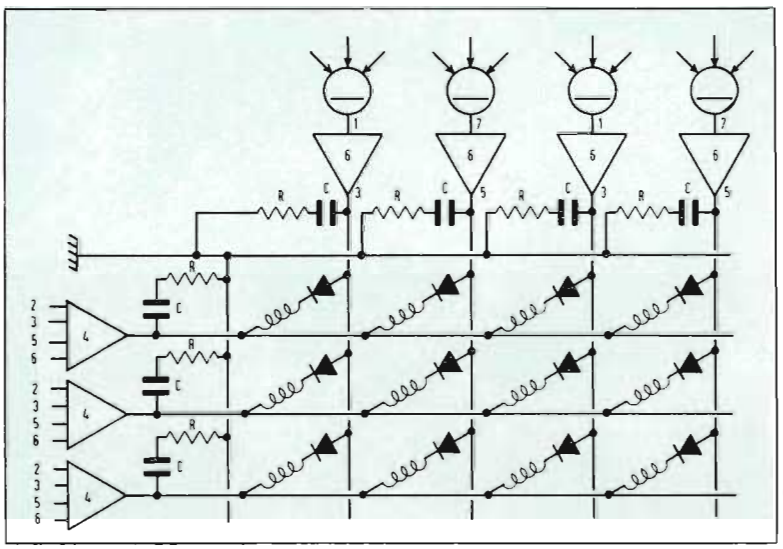
For use in a matrix drive see Design Bulletin No. 5.

(ISSUE 5)

MATRIX DRIVE

Minilog type 4 and Minilog type 6 can be used to drive a matrix.

CIRCUIT:



Recommended diode SX632.
Values of R and C are given on Design Bulletin No. 17.

OUTPUT: The output will drive loads rated at up to 24V and up to 50mA.

NOTE: A matrix composed of loads rated at 300mA can be driven by a similar circuit using type 3, type 4 and type 6. Details are available on request.

ELLIOTT BROTHERS (LONDON) LTD · Elstree Way · Borehamwood · Herts · Telephone · ELStree 2040

D.C. LOADING RULES

The following rules apply for resistive loading within the range 5°C to 45°C.

1 — Up to 5 logic loads may normally be driven from a type 1 or type 7 MINILOG.

2 — A type 1 or type 7 MINILOG may only drive up to 4 logic loads where one or more of the elements which it drives is also driven by a type 2 MINILOG.

3 — The outputs of up to 15 type 1 or type 7 MINILOGS may be connected together in which case the common point is treated as the output from a single type 1 MINILOG.

N.B.—In this case the negative supply must only be connected to one element in the group.

4 — The outputs of type 1 and type 2 or type 7 and type 2 MINILOGS must not be connected together, but the outputs of type 1 and type 7 MINILOGS may be.

5 — Up to 25 logic loads may be driven from a type 2 MINILOG.

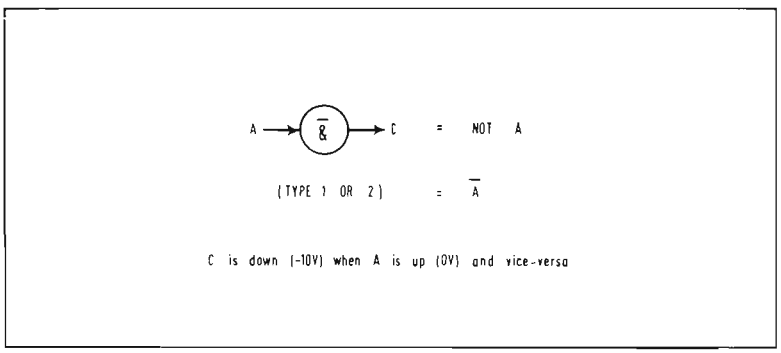
6 — The outputs of up to 10 type 2 MINILOGS may be directly connected together to drive a common rail. Such a rail may drive up to 17 logic loads when driven by two type 2 elements, reducing by two logic loads for each additional type 2 element driving the common rail.

Note — 1 — These rules apply for wiring voltage drops not exceeding 0.25 volts between any elements in a logical system.

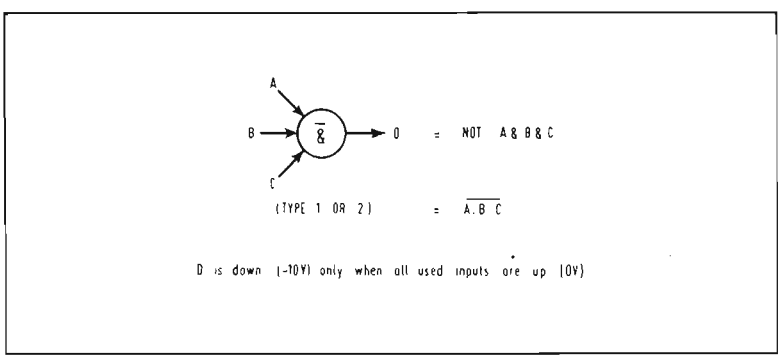
2 — A logic load is that load imposed by connecting one input, i.e. pins 1, 2, 3, 5, 6 or 7 of a type 1 or type 2 or pins 2, 3, 6 & 7 of a type 7 MINILOG.

FUNDAMENTAL LOGIC UNIT

'NOT' unit (Inverter): A MINILOG using one input performs an inversion function:



'AND' unit (Gate): One MINILOG can be used to obtain the 'NOT AND' (inverted AND) function. If an 'AND' function is required, this unit is followed by an inverter.

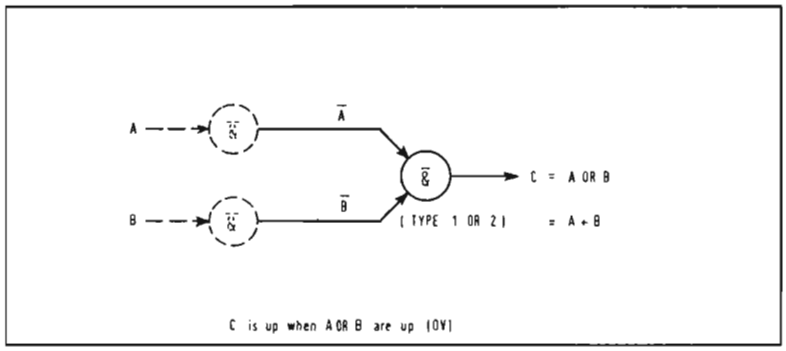


Where more than 6 inputs are required, the 'AND' unit can be extended as described in DESIGN BULLETIN 8.

(ISSUE 5)

FUNDAMENTAL LOGIC UNIT

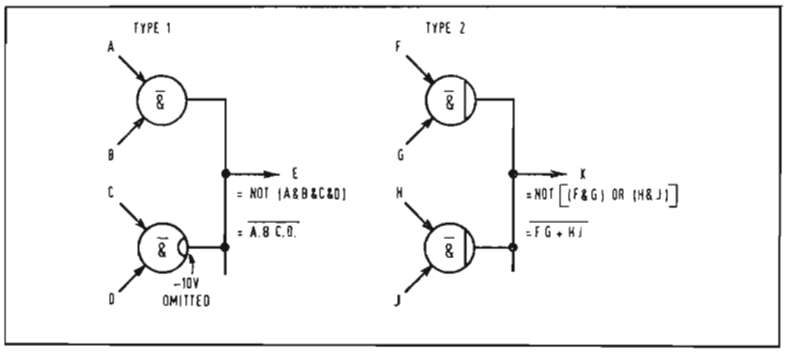
'OR' unit (Mix): The 'OR' function is accomplished using one MINILOG and applying inverted inputs. Three MINILOGS are required should the inverted waveforms not be available already.



COMMON OUTPUTS: Logical functions may be obtained by directly connecting the outputs of two or more MINILOGS.

In the case of type 1 elements, the connection acts as a means of extending the & function to more than 6 inputs, i.e. E is down ONLY when all used inputs *on all elements* are up.

In the case of type 2 elements, the connection acts in a different way. K is down when all the used inputs *on any one element* are up.

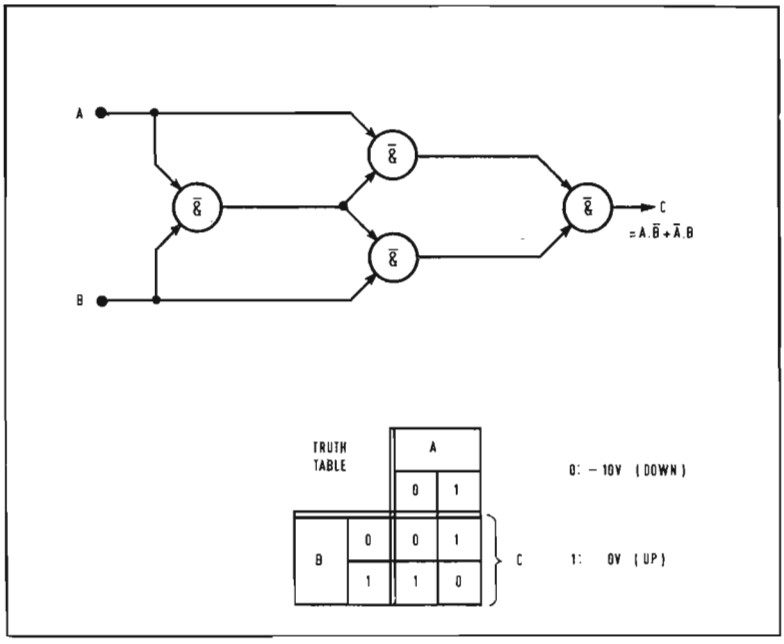


The loading rules applying to these connections are given in DESIGN BULLETIN 6.

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

ANTICOINCIDENCE (Exclusive 'OR'): The instantaneous state of two inputs may be compared in this unit, the output of which is down whenever the two inputs are up or down *together*.

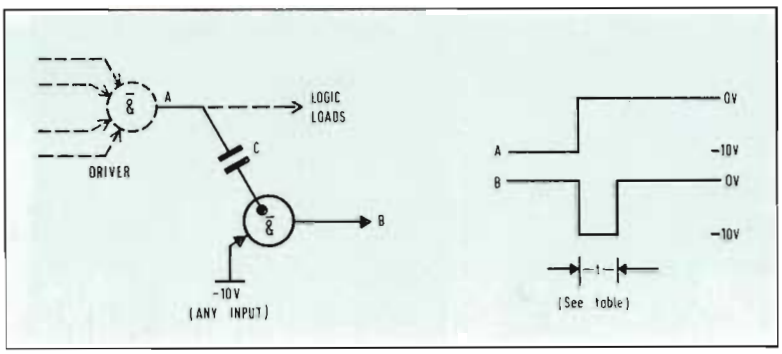


C is down when A and B are 1 or A and B are 0. The action of this unit can be followed through with reference to DESIGN BULLETINS Nos. 7 and 8.

(ISSUE 5)

FUNDAMENTAL MINILOG FUNCTIONS

DIFFERENTIATION: In order to differentiate the positive going edge of an output from a type 1 MINILOG, the following connection is used.



NOTE: (1) The driver stage must be a type 1 or type 7 element.

(2) Four inputs only may be used on the driver stage.

(3) The inputs to the driver must be from type 1/type 7 OR type 2.

(4) The output of the driver may also drive 5 logic loads.

(5) Recommended values of C.

Minimum 0.001 μF
Maximum 10,000 μF (with no logic loads at A).
,, 5 μF when one or more logic loads are connected at A.

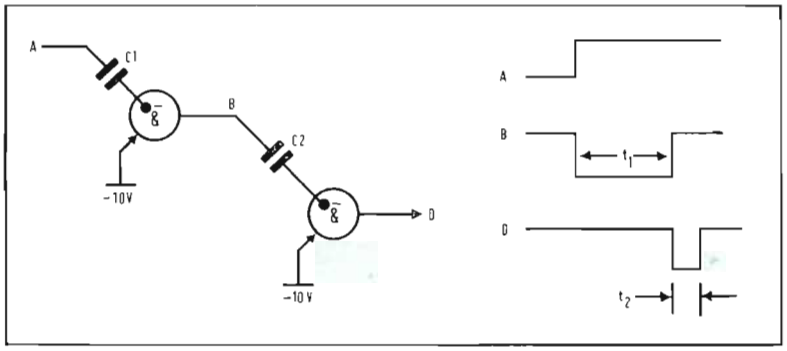
(6) The value of t depends upon the number of logic loads imposed on point A.

NUMBER OF LOGIC LOADS AT POINT A	VALUE OF t (m sec.)
0	8C
1	7·5C
2	6·5C
3	6·0C
4	5·7C
5	5·4C
	Where C is in μf

(7) If the inputs to the driver come from type 2 elements the output A may drive 5 logic loads *and* 4 differentiator stages. Recommended value of the TOTAL capacitance as in note 5 above.

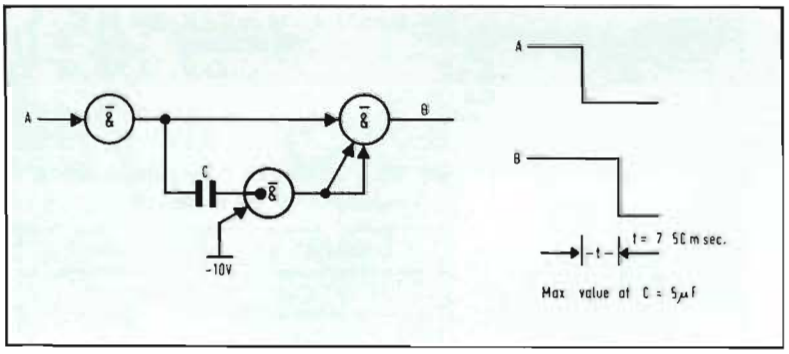
P.T.O.

DELAY AND DIFFERENTIATION: A differentiated pulse may be obtained, delayed from the positive going output edge from a type 1 MINILOG as shown:



Note. C_1 is not greater than $15C_2$ and C_1 is not less than C_2 for value of t_1 and t_2 see table above.

DELAY:

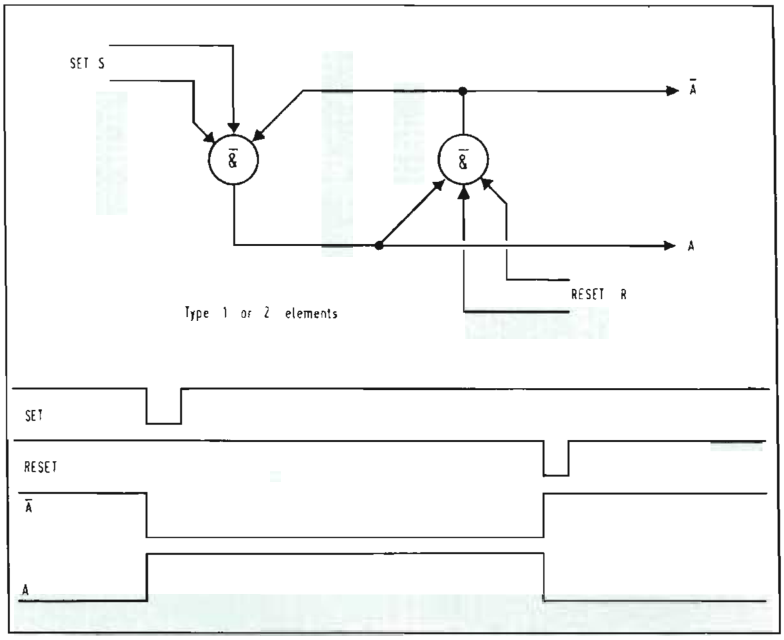


A step waveform can be delayed by the connections shown.

(ISSUE 5)

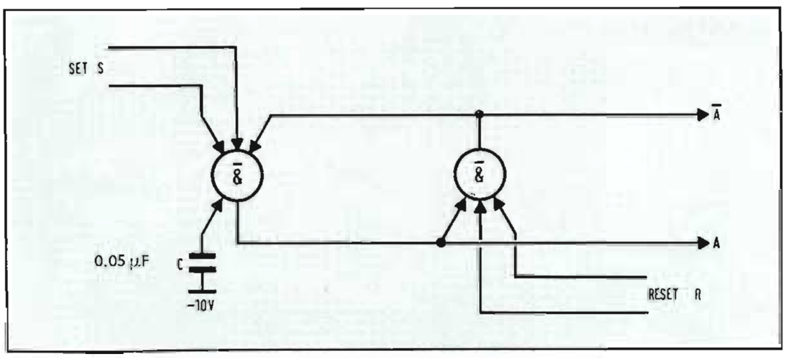
FUNDAMENTAL LOGICAL FUNCTIONS

SINGLE BIT MEMORY UNIT (BISTABLE): The output of this unit is set to one state and remains in that state until reset to the opposite state. The inverse (complementary) output is also available.



One method of ensuring that the bistable element is always "set up" in a particular way is to connect a capacitor to a normal input with the other end taken to —10V. In the example shown A will go to OV when the power supplies are switched on.

Alternatively, initial reset can be achieved as shown in Design Bulletin No. 21.

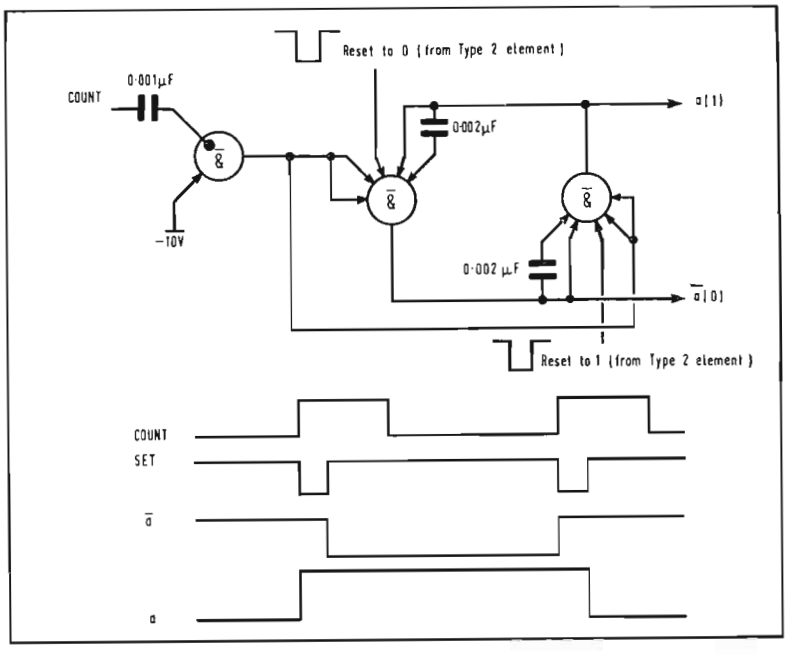


(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

COUNTER STAGE: A single stage of a binary counter can be constructed from 3 MINILOGS as shown.

The outputs change state after each positive going edge of the count waveform.



The switching rise time of MINILOG elements is <2μs and the switching fall time is <4μs.

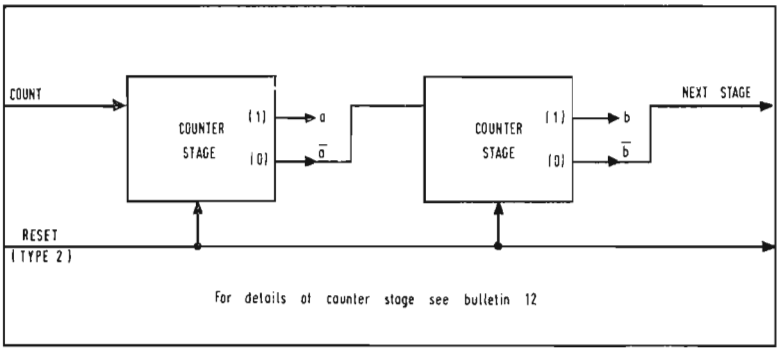
The connection of counter stages to form a full binary counter is shown in DESIGN BULLETINS No. 13 & 14.

If it is desired to reset the counter to a known state on switching on, initial reset should be applied to one side of the counter (see Design Bulletin 21).

(ISSUE 5)

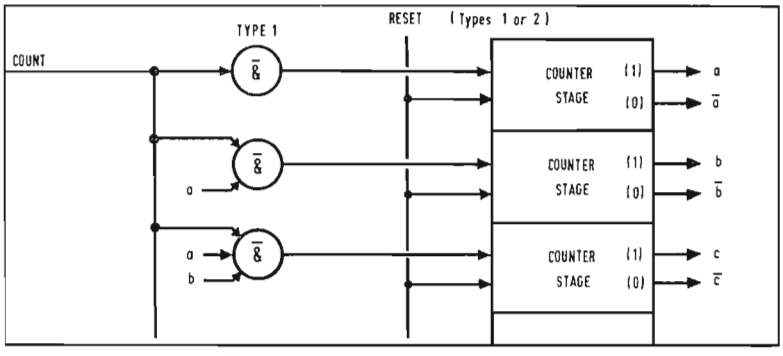
FUNDAMENTAL LOGICAL FUNCTIONS

SERIAL BINARY COUNTER: The output of each counter stage is fed to the input of the next. The connection shown will 'count up' on the COUNT waveform. If the waveforms a, b, etc. are connected, it will count down. Type 1 MINILOGS must be used.



Carry propagation: 2 μs per stage.

PARALLEL BINARY COUNTER: This counter requires one more MINILOG per stage than the SERIAL counter and counts on the negative going edges of the COUNT waveform. The connection shown counts up, but if the gates are fed from the 'bar' waveforms, it will count down.



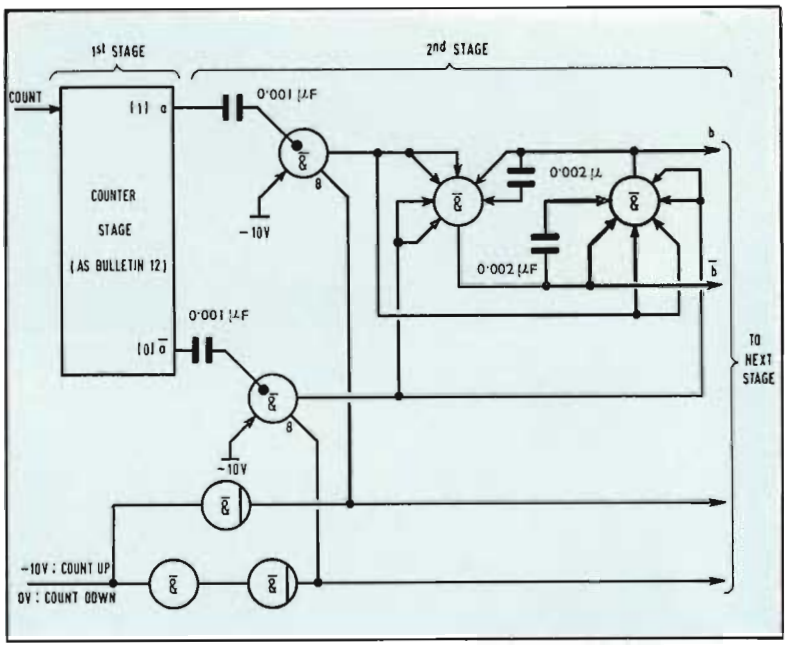
Each stage is fed from a type 1 MINILOG the inputs to which are "COUNT" and the outputs of all the less significant stages. All stages are set to the next value simultaneously, hence no time need be allowed for carry propagation. Maximum counting frequency: 40 Kc/s.

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

REVERSIBLE COUNTER: The binary counters described in DESIGN BULLETIN 13 are capable of counting one way only (i.e. count up *or* down). To build a reversible counter (i.e. one which counts up *and* down), the first stage (a normal counter stage) is followed by counter stages each of which is made up of 4 MINILOGS. One type 1 MINILOG and two type 2 MINILOGS are also required per 3 stages.

For driving many stages it is more economical to use type 5 elements with external resistors connected as shown in Design Bulletin 19.



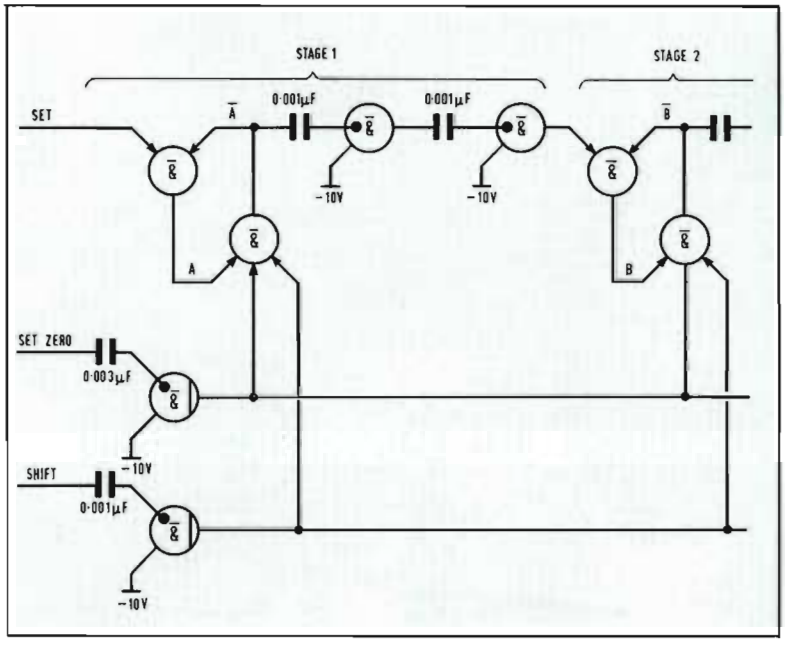
Each stage is operated respectively by the output or the inverse output of the previous stage depending on whether counting down or counting up is required.

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

SHIFT REGISTER: A shifting register can be built using only 4 MINILOGS per stage plus 2 MINILOGS per 25 stages.

Type 1 MINILOGS are used throughout for up to 5 stages after which the SET ZERO and SHIFT pulses must be generated by Type 2 MINILOGS.



RATE OF SHIFT: Up to 40 Kc/s.

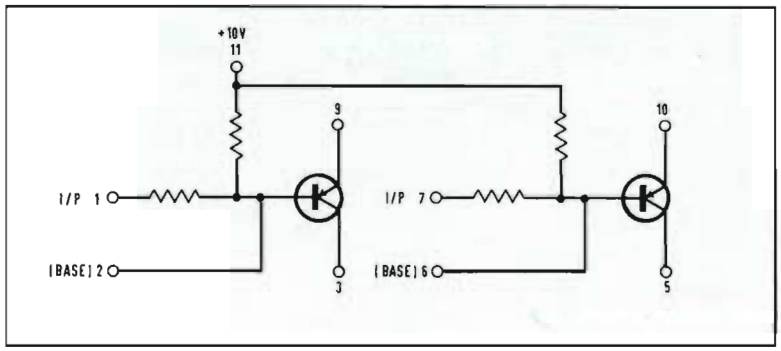
OPERATION: The application of the SHIFT pulse causes the state of each bistable to be transferred into the next bistable along the register.

SET ZERO sets all the bistables to 0, i.e. A, B, C, etc. all down, $\overline{A}$, $\overline{B}$, $\overline{C}$, etc. all up.

(ISSUE 5)

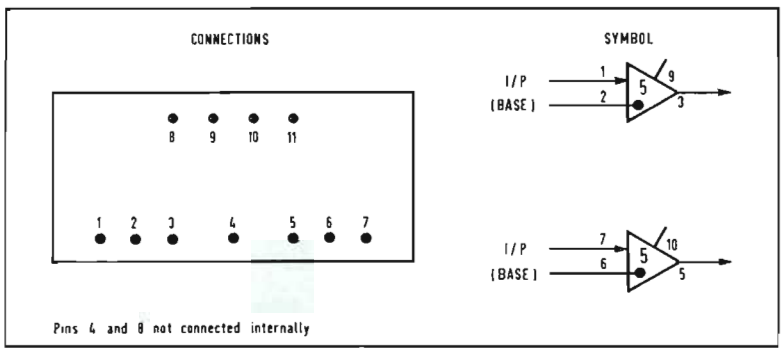
ELEMENT TYPE 5 (MkII)

This element is intended as a lamp drive and MUST NOT BE USED WITH INDUCTIVE LOADS. (The MINILOG ELEMENT TYPE 6 is for this purpose).



LOADING: Each input imposes a load of 2 logic loads.

OUTPUT: 50 mA max. up to 12V when each half independent.
300 mA max. up to 12V with both halves cascaded.
(For load connections see over).



DIMENSIONS: 2″ x 0.85″ x 0.625″ deep.

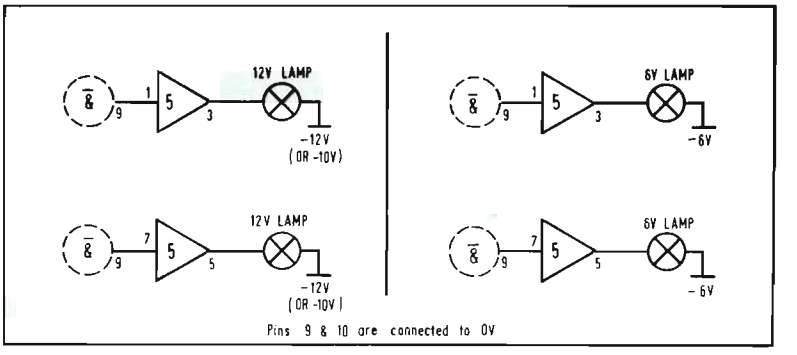
LEADS: 11 off 0.032″ dia. tinned copper wire ⅜″ long.

THE ELEMENT IS FULLY ENCAPSULATED.

P.T.O.

ELEMENT TYPE 5 (Mk11)

LOAD CONNECTIONS INDEPENDENT OUTPUTS: Each half of a type 5 element may be used to drive separate loads.

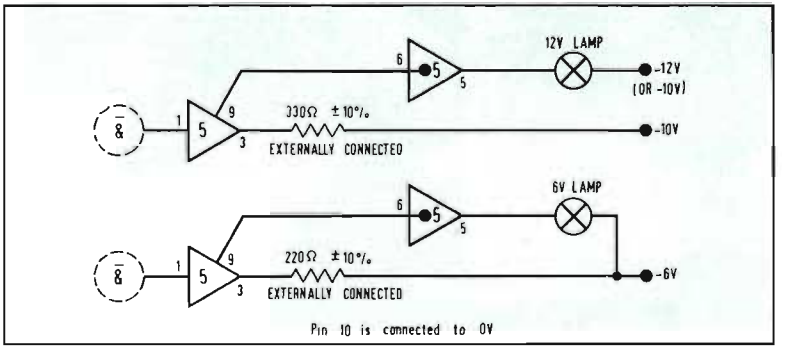


The lamp is lit when the input to the type 5 element (pin 1 or pin 7) is down (−10V).

OUTPUT CURRENT: 50 mA max.

POWER REQUIREMENTS: +10V at 0.5 mA.

CASCADED CONNECTION: One half of a type 5 element may be used to drive the other half in cascade Alternatively. one element may be used as two "first halves" or two "second halves".



The lamp is lit when the input to the type 5 element (pin 1) is down (−10V).

OUTPUT CURRENT: 300 mA max.

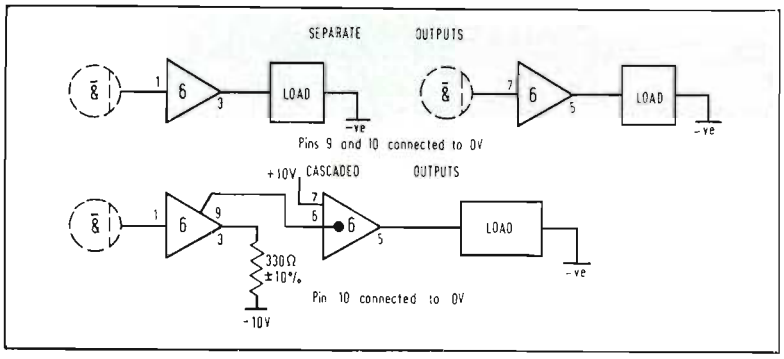
POWER REQUIREMENTS: +10V at 3 mA.

(ISSUE 5)

ELEMENT TYPE 6 (MkII)

This element is intended to be used as a power drive for relays etc. The circuit, pin layout and physical dimensions are the same as those of a type 5 element.

NON-INDUCTIVE LOADS:



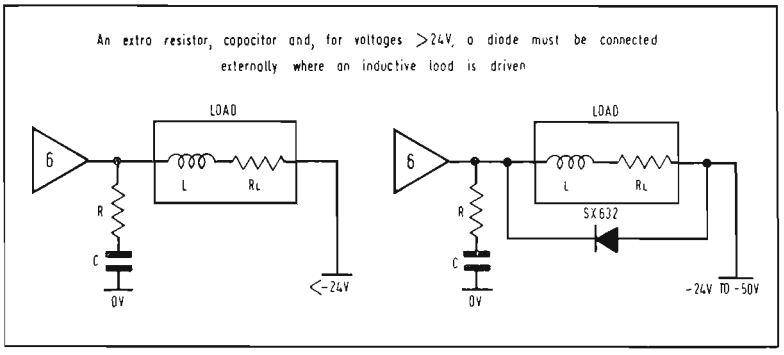
CASCADED CONNECTION: A type 6 element may be used as two "first halves" or two "second halves" of a cascaded connection.

With no loss in output current, the first stage of the cascaded connection may be a type 5 element (can be driven from a type 1 MINILOG).

LOADING: Each input imposes a load of 6 logic loads (it must therefore be driven from a type 2 MINILOG or a type 5 MINILOG).

OUTPUT CURRENT: 50 mA max. (separate outputs) up to 30V. } Without RC
300 mA max. (cascaded output) up to 30V. } connections.

INDUCTIVE LOADS:



The values of R and C for various loads are given overleaf.

POWER REQUIREMENTS: +10V : 2 mA (separate outputs) 8 mA (cascaded output).

OUTPUT CURRENT: 50 mA max. (separate outputs) up to 50V.
300 mA max. (cascaded output) up to 50V.

P.T.O.

ELEMENT TYPE 6 (Mk II)

SOME RECOMMENDED VALUES OF EXTERNAL COMPONENTS

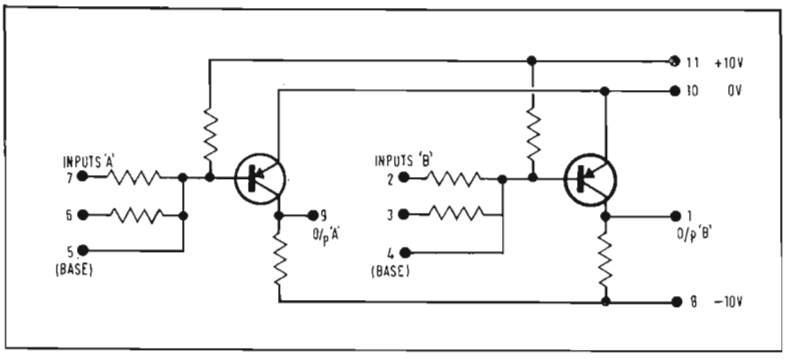
Relay	*Voltage*	*R(Ω) ±10%*	*C(μF)*	*Diode*
Siemens Halske — Trls 162b	24	330	1.0	—
Arrow Electric Contactor	24	100	4.0	—
C.P. Clare Mercury Wetted Contact HG.4A1016	24	220	2.0	—
S.T.C. 700/4190 H.D.	24	330	1.0	—
Elliott Dry Reed E.2R.A.1000	50	470	0.5	SX632
Elliott Mercury Wetted Contact	50	120	2.0	SX632
I.B.M. O/P Writer Relays	48	68	2.0	SX632
P.O. Relays — 1000 Ω	48	330	0.5	SX632
P.O. Relays — 2000 Ω	48	560	0.5	SX632
S.T.C. Sealed Relays — 2500 Ω	48	680	0.25	SX632
Creed Trip Relay R_L = 200 Ω	24	100	0.25	—
Creed Character Relay R_L = 97 Ω	24	47	4.0	—

N.B.—Capacitor values must not fall below 75% of the nominal figure.

ELEMENT TYPE 7 (MkII)

This is a double logic element, each half having one base and two logic inputs. The pin positions, dimensions, temperature range and logical action are the same as for ELEMENT TYPE 1 (see Design Bulletin 1).

CIRCUIT:

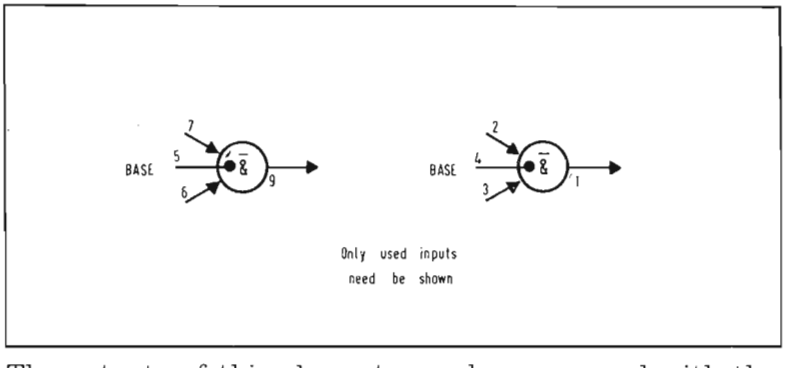


EXTRA INPUTS: It is permissible to add one further logic input to each half by connecting an externally mounted 11k 5% T.E. Welwyn F20 resistor to the base input.

LOADING RULES: As for ELEMENT TYPE 1.

POWER REQUIREMENTS: +10V: 0.2mA Voltage tolerance ±10% Max. ripple: 100mV p-p.
—10V: 13.2mA Voltage tolerance ±10% Max. ripple: 10mV p-p.

LOGIC:

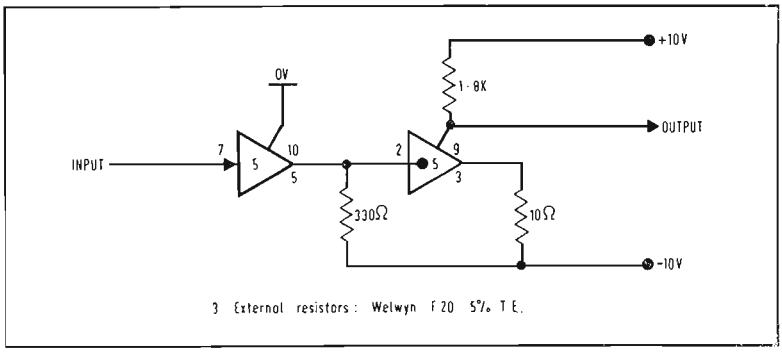


COMMON OUTPUTS: The outputs of this element may be commoned with the outputs of TYPE 1 ELEMENTS as described in bulletins 6 and 8. In this case, the —10V connections should be removed from the TYPE 1 ELEMENT, since the —10V is common to both halves of the TYPE 7.

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

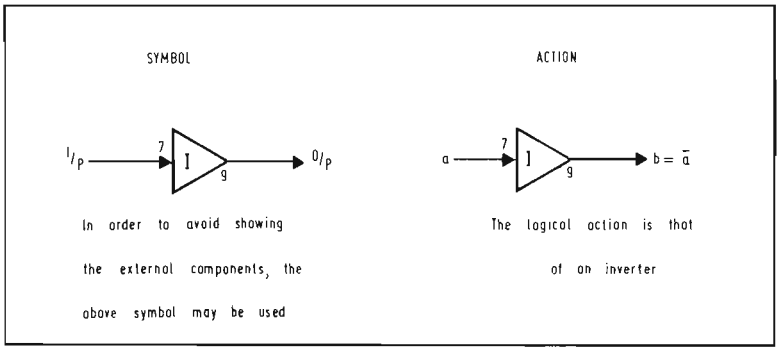
LOGIC ELEMENT DRIVE: One ELEMENT TYPE 5, connected as shown may be used to drive up to 200 logic loads.



LOADING: The input imposes a load of 2 logic loads

POWER REQUIREMENTS: +10V: 10mA (max.)
—10V: 200mA (max.)

LOGIC:

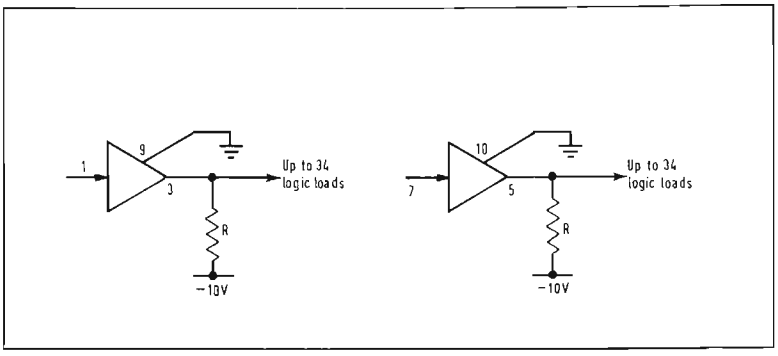


NOTE: Pin 11 is connected to +10V.

P.T.O.

MEDIUM LOADS: Each half of the type 5 element can be used to drive up to 34 logic loads.

CIRCUIT:



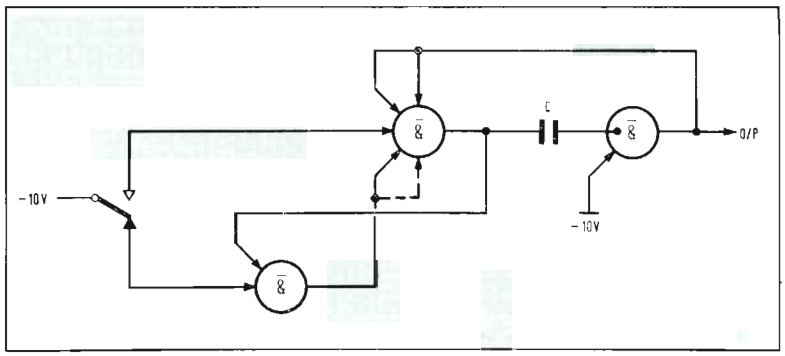
Recommended value of R 220Ω Welwyn Metox F22 ±7% T.E.
or 220Ω Electrosil N22 ±5% T.E.

Switching time. The rise and fall times are each better than 12μ sec.

(ISSUE 5)

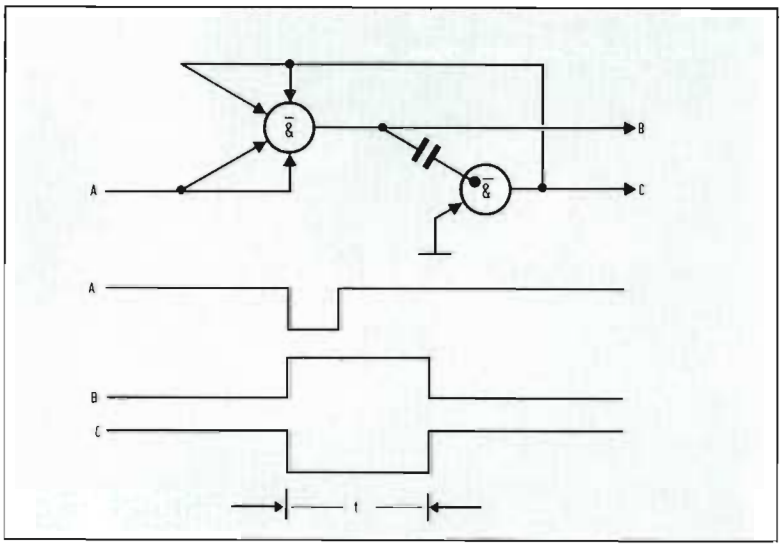
FUNDAMENTAL LOGICAL FUNCTIONS

SINGLE SHOT:



It is permissible to use a TYPE 2 element in the output stage. If this is done the additional connection shown dotted should be made.

MONOSTABLE: A monostable unit is shown below. This can be used to alter the length of a pulse (A). If the width of pulse A is less than 't', the waveforms B and C are as shown. If, however, the width of A is greater than t, B is the inverse of A and the width of pulse C remains unchanged.

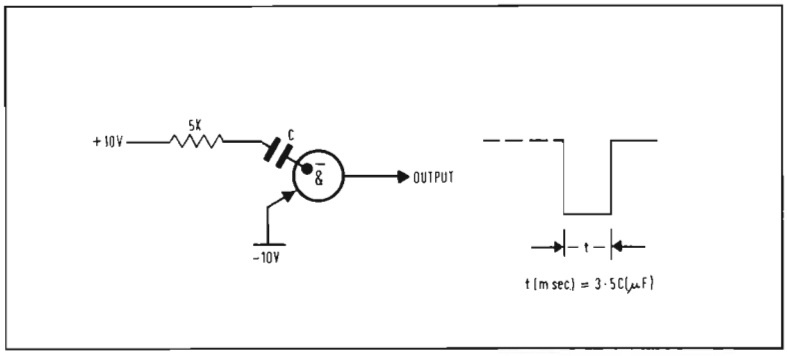


The rules for connecting logic load and other differentiators to point B, and value of t, are given in Design Bulletin 10.

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

INITIAL RESET:



In order initially to set counter stages or bistable elements to a desired state, the above circuit can be used. One pulse only will appear at the output when the power supplies are switched on.

NOTE: (1) Output may drive 5 logic loads and 4 differentiators.

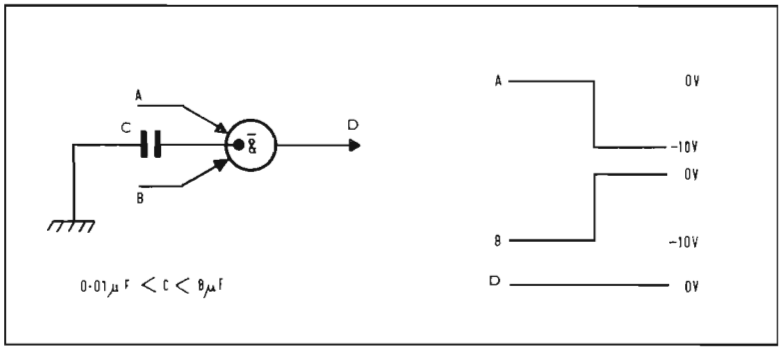
(2) If differentiators are used:

(*a*) Maximum total value of differentiator capacitances is C/2

(*b*) Minimum total value of differentiator capacitances is C/10

(3) Suggested minimum value of C = 0.02μF.

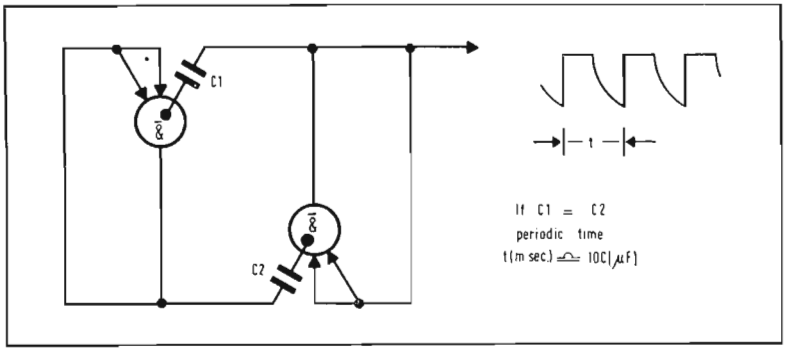
BASE DECOUPLE:



The above connections can be used to prevent output spikes when the two inputs A and B change state together.

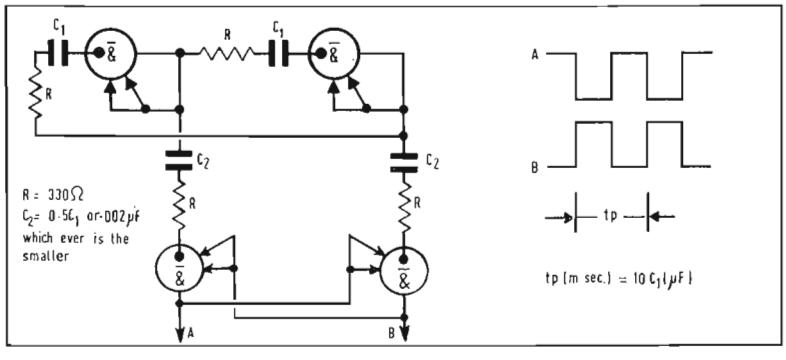
FUNDAMENTAL LOGICAL FUNCTIONS

OSCILLATOR: An oscillator giving an output wave form as shown can be constructed from two type 1 MINILOGS.



If C_1 and C_2 are of unequal values, an unequal mark/space ratio of up to 3:1 may be achieved. For mark/space ratios greater than this, the oscillator should be followed by a differentiator stage to produce the desired pulse width. 3 logic loads may be driven from either side.

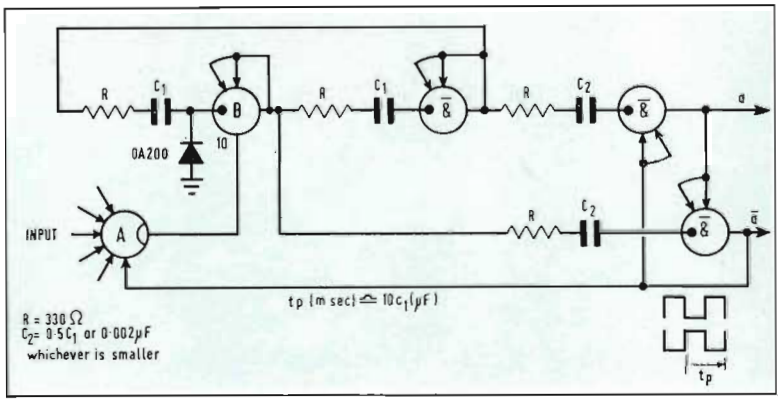
An improved output waveform can be obtained from the oscillator shown below.



3 logic loads may be driven from each side of the oscillator.

GATED MINILOG OSCILLATOR

CIRCUIT:

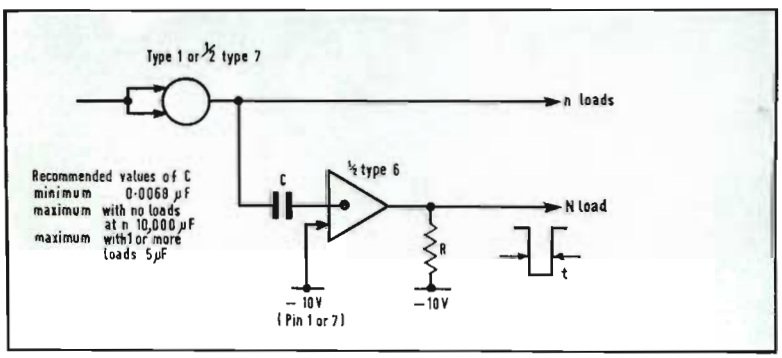


The oscillator will start with "a" rising and "$\bar{a}$" falling when one input goes down (−10V).
The oscillator will stop with "a" down and "$\bar{a}$" up when ALL inputs are up.

NOTE: The −10V supply is NOT connected to the collector of the Minilog marked A (pin 8) and the output of A is taken to pin 10 of the Minilog marked B. Pin 10 of Minilog B is NOT connected to earth.

DIFFERENTIATOR TO DRIVE MANY LOADS

CIRCUIT:



The value of t depends upon C and the number of logic loads n.
The value of R depends upon the value of N.

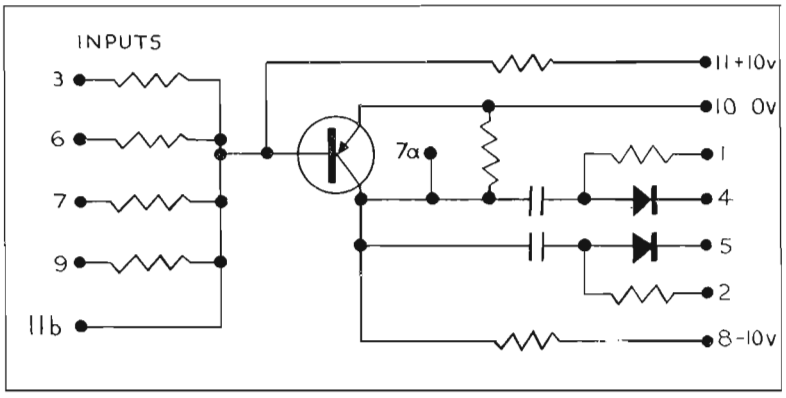
n	t
0	1·3C
1	1·23C
2	1·06C
3	0·98C
4	0·94C
5	0·89C

N	R ohms	
UP TO 29	180	Welwyn F22 7% T.E. or Electrosil N25 5%
" " 35	150	
" " 40	120	
" " 52	100	
" " 64	82	Welwyn F23 7% T.E. or Electrosil N30 5%
" " 85	68	

ELEMENT TYPE 8 (MkII)

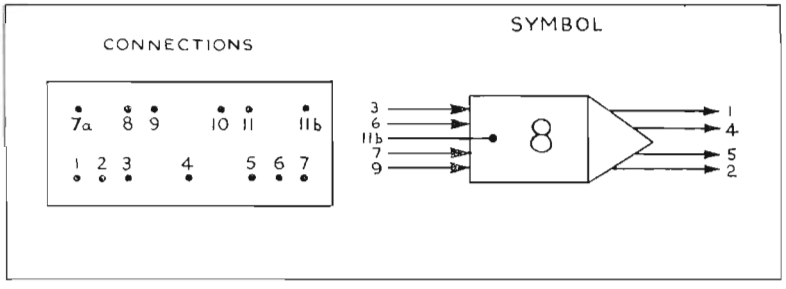
This is a pulse steering unit which may be used, in conjunction with a bistable, as a binary counter stage.

CIRCUIT:



LOADING: Each input imposes a load of one logic load.

POWER REQUIREMENTS: +10V: 0.1mA. Voltage tolerance ±10%. Max. ripple 100mV p-p.
—10V: 6.7mA. Voltage tolerance ±10%. Max. ripple 10mV p-p.



DIMENSIONS: 2″ × 0.85″ × 0.625″ deep.

LEADS: 11 off 0.032″ dia. tinned copper wire ⅜″ long.

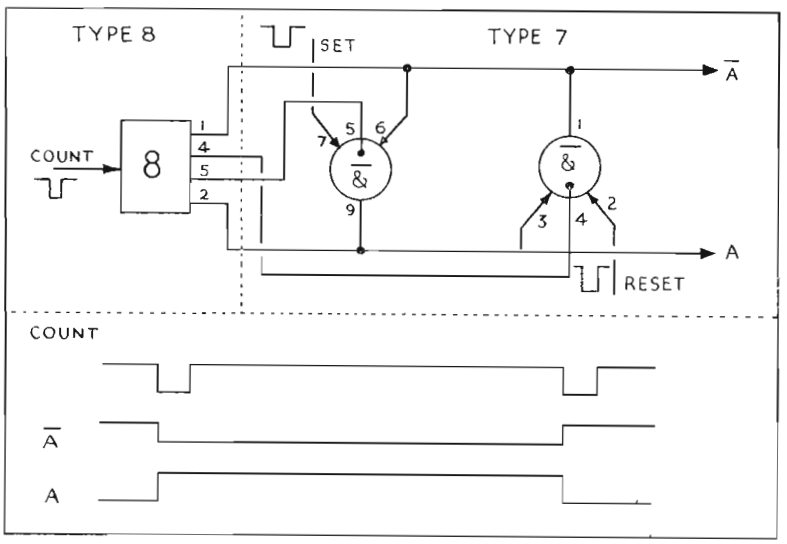
The functioning of this unit when used with a bistable is described in Design Bulletin No. 28.

THE ELEMENT IS FULLY ENCAPSULATED.

FUNDAMENTAL LOGICAL FUNCTIONS

COUNTER STAGE: Minilog Type 8 and Minilog Type 7 (connected as a bistable), may be used as a single stage of a binary counter.

The outputs change state after each negative going edge of the count waveform.



This combination is more economical than the alternative given on Minilog Design Bulletin No. 12, since only two elements are required.

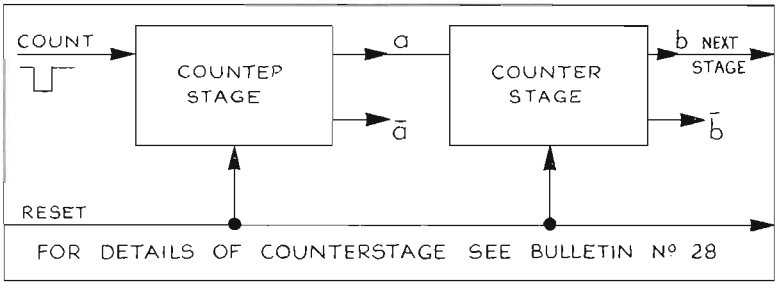
If it is desired to set the counter to a known state upon switching on, an initial set or reset should be applied to one side of the counter (see Design Bulletin No. 21).

(ISSUE 5)

FUNDAMENTAL LOGICAL FUNCTIONS

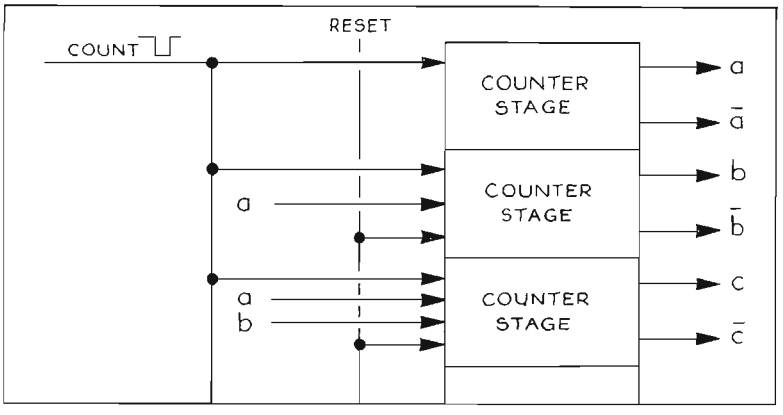
SERIAL BINARY COUNTER: Using the counter described in Bulletin No. 28.

The output of each counter stage is fed to the input of the next. The connection shown will 'count up' on the COUNT waveform. If the waveforms $\bar{a}$, $\bar{b}$, etc., are connected, it will count down.



Carry propagation $<2\mu S$ per stage

PARALLEL BINARY COUNTER: The counter stages as described in Bulletin No. 28 may be connected to form a parallel binary counter as shown in the figure. The circuit shown will count up on negative-going edges of the count waveform, but if the gates are fed from the 'bar' waveforms it will count down.



The inputs to each stage are 'COUNT' and the outputs of all the less significant stages. All stages change to the next value simultaneously ($<2\mu S$) because there is no carry propagation as in the serial counter.

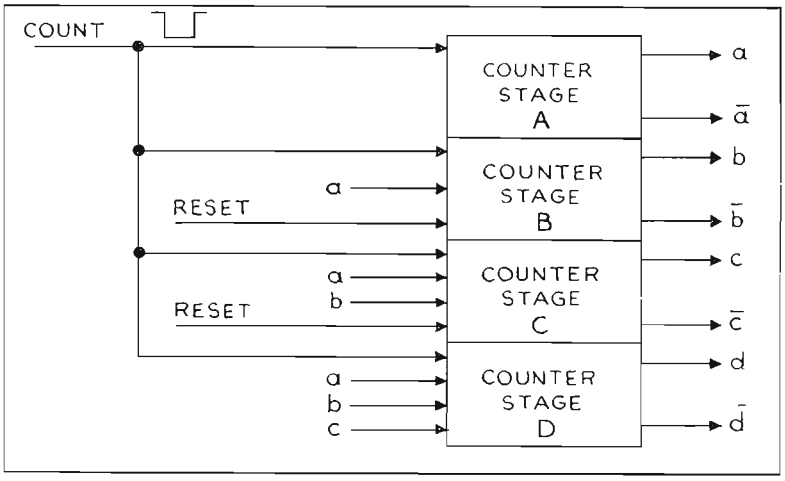
For more than 4 stages extra Minilog elements are required according to the usual loading rules. Alternatively, serial propagation ($<2\mu S$) may be used between each group of 4 stages.

P.T.O.

FOUR STAGE BINARY COUNTER FOR COUNTS OF 10, 12 OR 16:

Using the counter stage described in Bulletin No. 28.

This circuit is similar to the PARALLEL BINARY COUNTER described overleaf, but incorporates an automatic 'reset to zero' on the 10th, 12th or 16th count.



As shown above the counter will reset to zero at 16. With output $\bar{d}$ connected to the reset input of Stage C the counter will count up to 12 as shown in table (2). With output $\bar{d}$ connected to the reset inputs of Stages B and C the counter will count up to 10 as shown in table (3). This circuit obviates the need for a reset decoder and decode gate.

MODIFIED OUTPUT CODES:

	(1) 16 *Counter*				(2) 12 *Counter*				(3) 10 *Counter*			
	d	c	b	a	d	c	b	a	d	c	b	a
1	0	0	0	1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1	0	1	1	1
8	1	0	0	0	1	1	0	0	1	1	1	0
9	1	0	0	1	1	1	0	1	1	1	1	1
10	1	0	1	0	1	1	1	0	0	0	0	0
11	1	0	1	1	1	1	1	1				
12	1	1	0	0	0	0	0	0				
13	1	1	0	1								
14	1	1	1	0								
15	1	1	1	1								
16	0	0	0	0								