A Data Error Analyzer for Tracking Down Problems in Data Communications

A combined data generator and self-synchronizing receiver, this new instrument makes six different measurements simultaneously, helping to pinpoint sources of trouble in data communications systems.

by Jeffrey R. Duerr

WITH THE GROWING USE of voice-communication channels for the transmission of digital data, maintaining transmission reliability becomes of increasing concern.

Reliability can be enhanced by repeating messages or by transmitting at slower rates, which means less efficient use of facilities, or it can be enhanced by the use of error-correcting codes, which implies more complex equipment. On the other hand, increased reliability results from consistently maintaining optimum system performance.

Making sure that optimum performance is maintained at all times has not been as simple and straightforward as one might surmise. The transmission of digital data over any distance often involves sophisticated equipment designed and manufactured by several different firms. The data may originate in a keyboard/display terminal or a computer made by one firm, be coupled to someone else's telephone system by a modem made by still another firm, be transmitted over the telephone system to another modem, and finally reach the receiving terminal or computer. The system is usually a combination of the efforts of a terminal manufacturer, a separate modem manufacturer, a representative of the telephone company, and an in-house technician, none of whom are liable to be involved in a comprehensive view of the whole system.

Diagnostic programs that can show whether or not a system is operating satisfactorily have been written, but interpreting results when the system does not operate properly is often hard to do, especially since those who understand the diagnostics may not have a good understanding of the various parts of the system.

For these reasons a new instrument was conceived, an instrument sufficiently complex to fully exercise a sophisticated data link yet simple enough to be operated without detailed knowledge of the various parts of the system under test. Information presented by the instrument is unambiguous and easily interpreted to help track down the system component at fault.

This instrument, Model 1645A Data Error Analyzer (Fig. 1), is designed primarily to survey data communications systems that use voice-grade phone lines. It derives the information necessary to approach solutions to network problems by generating

Fig. 1. *Model 1645A Data Error Analyzer generates digital test patterns in its transmitter section, transmits the patterns through a communications channel, and analyzes the received patterns in its receiver section by comparing them to locally-generated patterns. It analyzes the patterns six ways simultaneously.*

and interpreting digital patterns. It operates at 12 standard bit rates from 75 to 9600 bits/s but it can analyze synchronous systems* at any bit rate up to 5 Mbits/s.

Multiple Tests

The Analyzer generates pseudorandom bit sequences for the data input. At the receiving end, it compares the received sequence to a locally generated sequence identical to the transmitted sequence. For end-to-end measurements, two instruments are used, but because the instrument contains both transmitting and receiving circuits, only one is needed for loop-around tests.

The instrument makes several tests as it compares the received and locally generated sequences. Besides measuring bit-error rate, which gives a measure of how well a digital transmission system is performing, it measures several other parameters to help localize problems. The tests it performs are:

- **Bit error rate** (BER), the ratio of number of incorrect bits to number of bits received. It is fast becoming the preferred indicator of digital transmission quality.
- **Block error rate** (BKER), the ratio of the number of data blocks that have errors to the number of blocks received. In the 1645A, each block has 1000 bits. When compared to bit-error rate, this indicates the distribution of error, that is, whether they are evenly distributed or whether they occur in bursts.
- **Skew**, a comparison of the number of times that a "1" data bit is in error to the number of times that a "0" is in error. As measured by the new Data Error Analyzer, skew is the percentage of time that "1's" are in error with respect to total errors. If the reading is not consistently near 50%, it indicates that the errors may be pattern sensitive or that a decision threshold somewhere in the system is improperly set.
- **Jitter**, which is peak-to-peak timing variations in the received bits expressed as percent of nominal bit period. This can be the result of power line pickup or other interference with the timing of the system.
- **Total peak distortion**, which is jitter plus bias, bias being a condition where marks, or "1" data bits, are consistently of a different length from the spaces, or "0" data bits, expressed as a percent of nominal bit period. It usually results from an improperly set threshold level and often results in skew.
- **Clock slip**, the number of times that data jumped one bit period or more during the selected measurement interval. It usually results from phase hits caused by path switching in the transmission link or it could be caused by slippage of the bit synchronizer in a synchronous modem.
- **Carrier loss**, expressed as the number of times that input data faded during the measurement period. An output is provided so the number of bits lost can be totaled by an external counter to derive a measure of total lost time.

* A synchronous system is defined as one where system timing is synchronized to a master clock in the transmitting modem. A clock-recovery circuit in the receiving modem reconstitutes the master clock for the terminal. In an asynchronous system, timing is controlled by the terminal, e.g. a teletypewriter.

Organizing Test Results

Errors are accumulated for a time interval equivalent to the number of bits selected by a front-panel switch, which gives a choice of 10^2 to 10^9 bits in decade steps. Tests may also be conducted in an AUTO mode that terminates a test on the next decade number of bits received after 98 errors have been counted. This assures valid (non-overranged) readings when the instrument must be left unattended. Tests may also be started and stopped manually.

Single tests can be made, each in response to a front-panel switch, or tests may be repeated automatically.

Regardless of the test selected for display during the measurement interval, front-panel indicators flash to show occurrence of each of four types of errors (BER, BKER, clock slip, carrier loss). During the test, the display presents a continuously updated indication of number of errors. Results of all tests are stored internally and at the conclusion of the measurement interval, are made available for readout individually, as selected by a front-panel switch. This permits comparison of all values obtained on the same data, an aid in diagnosing problems. The results of any four tests are also printed sequentially if an external printer is used, permitting long-term, repetitive tests to be conducted unattended.

The instrument outputs a pulse once per received digital sequence, enabling oscilloscope viewing of the received sequence. It also outputs a pulse whenever an error is detected. One of the uses for this output is to trigger an oscilloscope or logic analyzer when an error occurs, so the 16 bits that precede the error can be displayed. A 16-bit delay makes the last 16 bits available at a front-panel connector. This is useful in determining whether certain bit patterns cause the errors.

The time lapse between a data edge and an internal clock reference is available at a front-panel connector as an analog signal. This allows oscilloscope study of the cyclic nature of any jitter, often helping by providing clues as to the cause of the jitter, e.g., powerline pickup.

Where It Goes

In evaluating a system, the Data Error Analyzer usually connects to the modem in place of the terminal. Accordingly, it generates and responds to the "handshake" signals used by modems. The display includes the necessary indicators (DATA SET READY,

CLEAR TO SEND) and a front-panel switch selects the control status (DATA TERMINAL READY, REQUEST TO SEND). The switch also has a BACKWARD CHANNEL position to allow tests involving the modem's supervisory channel.

Interface is by way of a plug-in circuit card and connector (Fig. 2) that can be changed to meet the requirements of different interface standards. Normally, the instrument is supplied with a card that meets the logic-level and pin numbering requirements of EIA specification RS232C (CCITT V 24).

TTL-compatible inputs and outputs through BNC connectors on the front and rear panels facilitate use of the instrument in the lab and in other special situations.

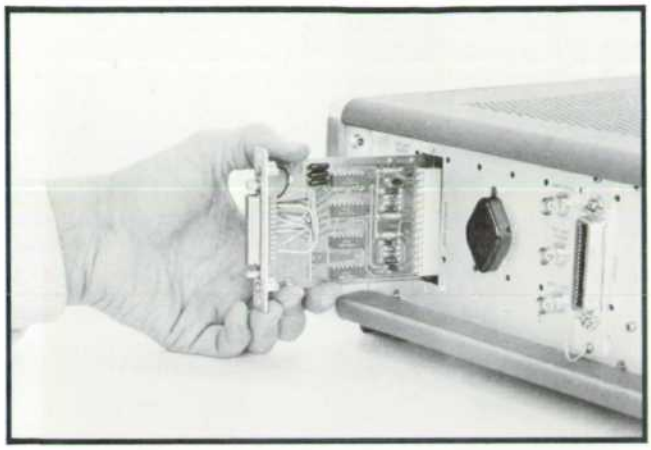

Fig. 2. *Plug-in modules interface the Data Error Analyzer to the system to be tested. The circuit card converts the instrument's logic levels to those required by the system. An appropriate connector is included.*

Test Patterns

A front-panel switch selects one of seven digital sequences in NRZ (non-return to zero) format for transmission and at the same time it sets the receiver circuits to the identical pattern. Four pseudorandom bit sequences (PRBS) are available (63, 511, 1047, and 1 048 575 bits) and there are three mark:space patterns, a single mark (or "1") preceded by 1, 3, or 7 spaces ("0"), a greater range of test sequences than CCITT requirements. A DATA/DATA switch allows the complement of the selected pattern to be used, e.g., a

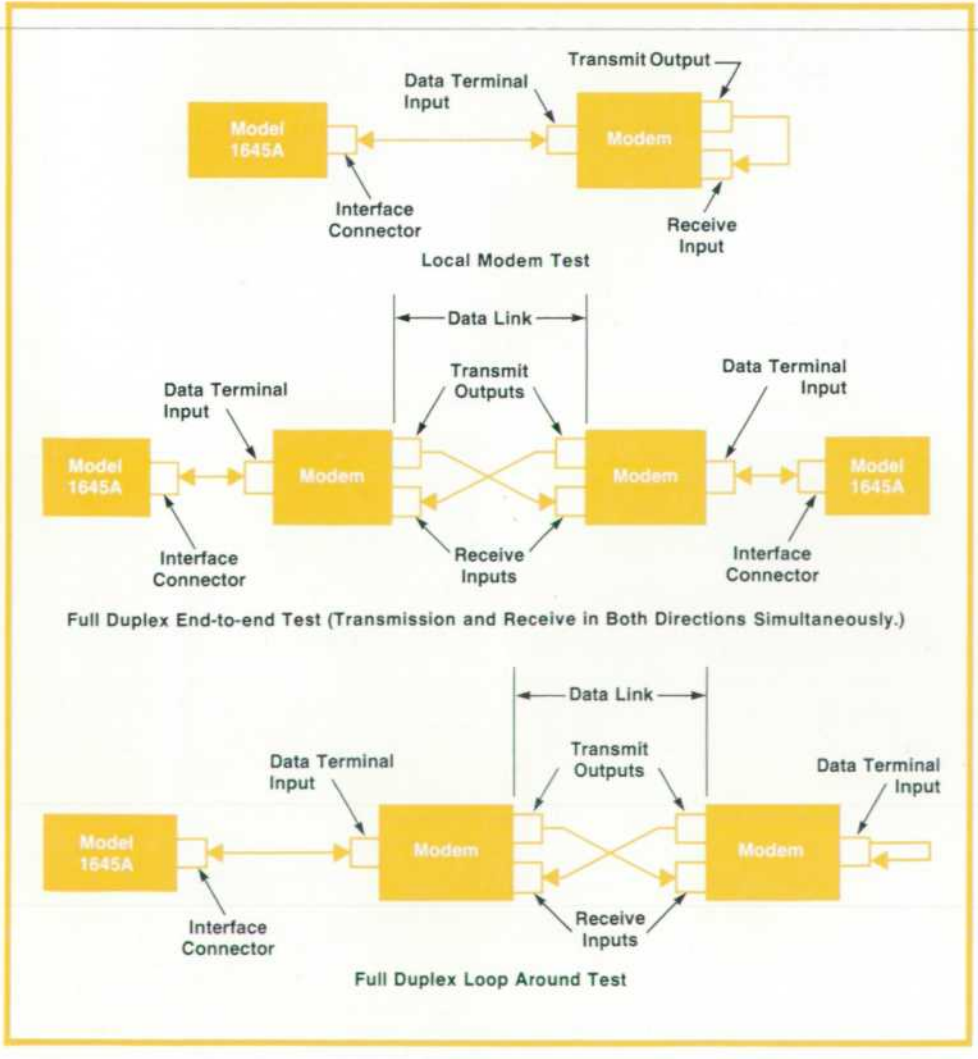

Fig. 3. *Some of the ways by which the Data Error Analyzer is connected to a system for tests.*

single space preceded by seven marks.

The pattern selector switch also has a MARK position that simply places a dc level on the output.

In end-to-end measurements, as long as the receiving instrument is set to the same pattern and bit rate as the transmitting instrument, the receiver circuits automatically synchronize to the transmitted bit rate and automatically align the locally-generated bit sequence to that transmitted. The receiving circuits also sense whether or not the polarity of the transmitted bit sequence may have been inverted during transmission and perform a re-inversion if necessary. Furthermore, the display circuits are autoranging. Thus, in routine tests the operator need concern himself only with setting the pattern and bit-rate switches and selecting the time duration of the test.

The instrument also has a LOOP mode that internally couples the transmitting circuits directly to the receiving circuits to verify that the instrument is operating correctly. One bit in each PRBS sequence can be made a deliberate error so the operation of the error-detecting circuits can be confirmed.

Some of the ways that the Data Error Analyzer may be connected to a system for tests is shown in Fig. 3. The manner in which it used to track down a problem is shown by the troubleshooting diagram of Fig. 4.

Instrument Operation

A block diagram of the Data Error Analyzer is shown in Fig. 5. The pseudorandom digital sequences are generated in a shift register that has feedback through exclusive-OR gates to its input from selected stages within the register. The mark:space sequences are generated by a counter that resets after a selected number of counts.

The clock frequency is divided down from a 5.76 MHz crystal oscillator to one of the standard modem clock frequencies, or it can be supplied by an external source.

The selected sequence is supplied to the front panel through a TTL-level buffer and to the interface module that converts the sequence to levels suitable for the system to be tested. These are the only circuits concerned with the transmit function. All the others belong to the receiver.

The test sequence, after transmission through the unit or system under test, is brought into the instrument either through a front-panel connector (not shown) or through the interface module. It is then distributed to the various circuits.

Receiver timing is controlled by the bit synchronizer. This has a stable 5.76 MHz oscillator that is phase-locked to the incoming data stream. The output of the oscillator is divided down to derive the selected clock frequency. It is not used, however, if an external clock is supplied.

Checking for Errors

The incoming data is compared bit by bit to the output of a closed-loop shift register that is configured the same as the transmitting shift register. Whenever the two bit sequences differ, an error is counted.

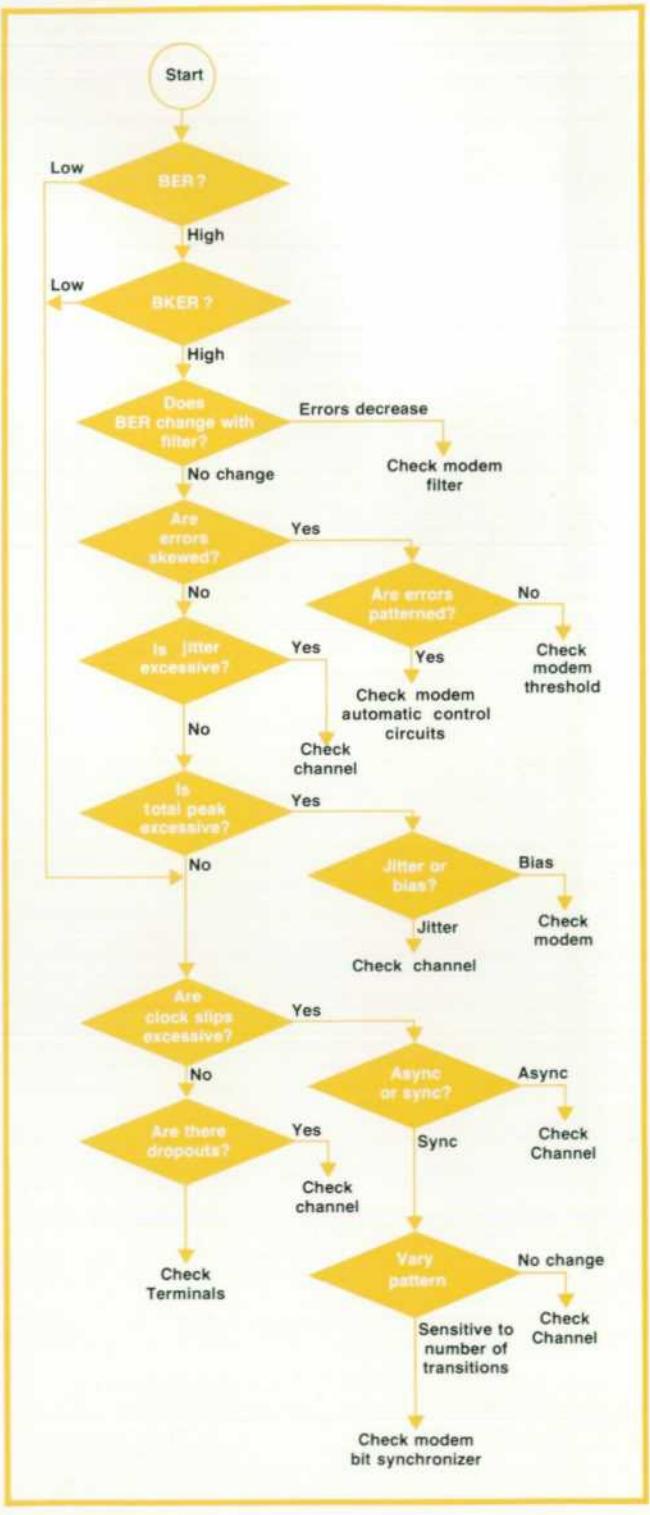

Fig. 4. *Troubleshooting diagram shows how various test results are used to track down problems in a data communications system.*

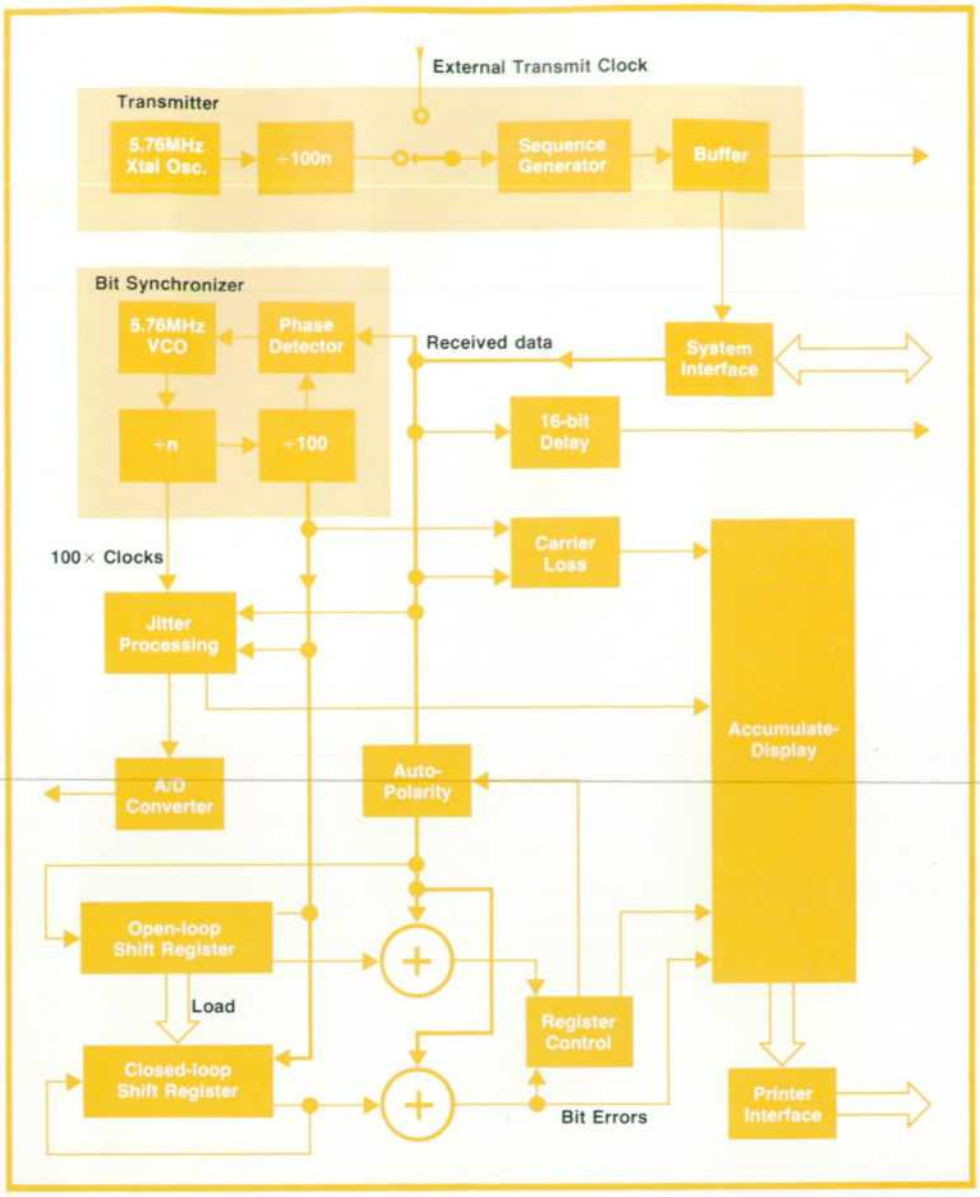

Fig. 5. *Block diagram of Model 1645A Data Error Analyzer.*

From this, measurements of bit-error rate are derived.

The incoming data is also compared to the output of an open-loop shift register that uses the same exclusive-OR gate configuration as the transmit register but which has no feedback connection. This register is used for synchronizing the closed-loop shift register, for detecting clock slip, and for detecting the need for inverting the polarity of the incoming data stream, as will be described subsequently.

Block-error rate is measured by incrementing a counter every 1000 bits only if one or more errors had occurred during the 1000-bit block. Skew is measured by totaling all errors in one counter and only the 1's errors in a second counter. When the all-error counter overflows on a count of 100 (actually 98 because of internal logic), the contents of the 1's-only counter is latched out as the measure of skew.

The jitter/bias circuit compares the timing of the data edges to clock pulses derived from the phase-locked oscillator. From this comparison, values for jitter and total peak distortion are derived.

Carrier loss is detected by a counter that totals clock pulses between data transitions in the incoming data stream. If more than 16 clock periods elapse without a data transition, it is assumed that a dropout occurred. For the long pseudorandom sequence, which has up to 20 bits without a transition, the decision threshold is set to 32. The error measuring circuits are inhibited when carrier loss is detected so as not to count false errors beyond those counted during the detection period. The error count resumes, however, after the carrier returns so measurements are not aborted by a carrier loss.

The incoming data is also applied to a 16-bit shift register that serves for temporary storage. This

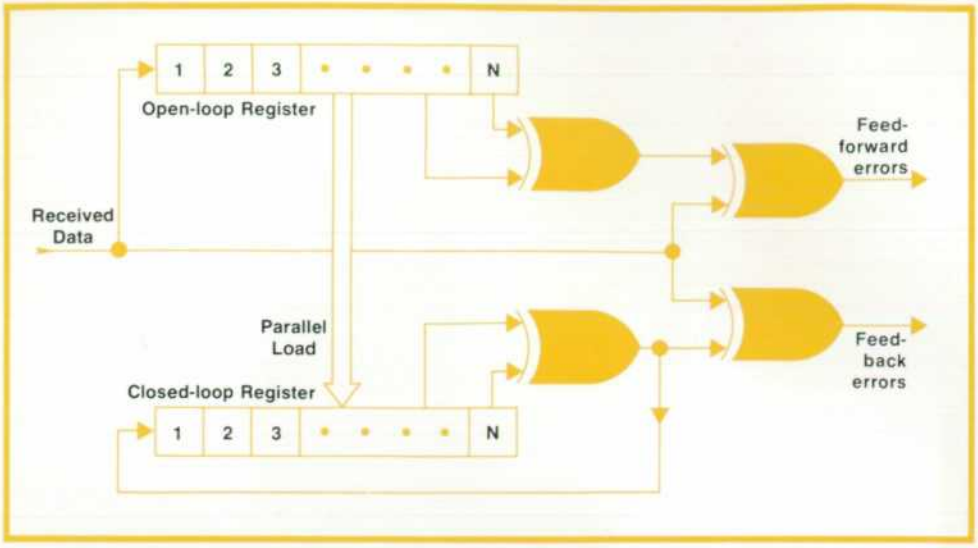

Fig. 6. *Simplified diagram illustrates concept behind closed-loop (feedback) and open-loop (feedforward) registers and how the two configurations are used in the Data Error Analyzer.*

makes the 16 bits that precede an error available for examination.

Automatic Sync

For the error detection circuits to work, the closed-loop shift register in the receiver must operate in synchronism with the shift register in the transmitter. Frame sync, as it is called, is accomplished with the help of the open-loop shift register.

By way of explanation, the two shift register configurations are shown in Fig. 6. The output of the closed-loop or feedback register is passed through an exclusive-OR gate and fed back into the input. There is an output from the exclusive-OR gate only when its inputs differ, so the output of the feedback register may or may not be fed back unaltered depending on the state of the other input to the gate. With proper choice of feedback taps (and precautions to assure that the shift register is never in the all-zero state), the shift register generates all possible combinations of N ones and zeros, except all zeros, where N is the number of states in the register.

If the same PRBS sequence generated by the feedback register were fed into the open-loop or feedforward register, the output of the feedforward register would be identical to its input, just as though it were supplying its own input. If, however, an error were injected into the input stream, it would cause *two* errors at the output (once in each stage connected to the exclusive-OR gate). Open-loop shift registers therefore are not accurate indicators of bit-error rate, not only adding errors but also cancelling errors when there is more than one error in the register. However, frame sync with the data stream is automatically achieved as soon as the data loads N bits into the register.

These properties are used to advantage in the new Data Error Analyzer. As shown in Fig. 6, the incoming bit stream is fed only to the feedforward register but it is compared to the outputs of both registers. The instrument, however, counts only the errors from the feedback register when measuring bit-error rate.

The comparison of the errors detected by the two registers determines the course of action within the instrument. At startup or following a clock slip, both registers will be out of frame sync, but within N bits the feedforward register will be loaded by the incoming data and will stop generating errors. The feedback register, on the other hand, continues to generate errors.

Errors from the feedback register are totaled in a counter that is reset by errors from the feedforward register. If the counter overflows, indicating a great excess of feedback errors over feedforward errors, the overflow turns on a front-panel OUT OF LOCK indicator and it initiates the transfer of the contents of the feedforward register, which now has valid data, into the feedback register. This is how the instrument achieves frame sync automatically.

Following start up, frame sync is required only when there has been a clock slip or when there has been a carrier loss. Each time frame sync is triggered, the clock slip totalizer is incremented one count.

This system is also used to detect the polarity of the data stream. If the data stream is inverted by the system under test, the output of the feedforward register will nevertheless have the proper polarity because both inputs to the exclusive-OR gate are inverted. The feedforward error detector would thus detect errors 100% of the time. If errors are counted 100% of the time, the control circuits switch an inverter into the data path.

The autopolarity system is locked up during a test interval to prevent bursts of errors from triggering polarity inversion.

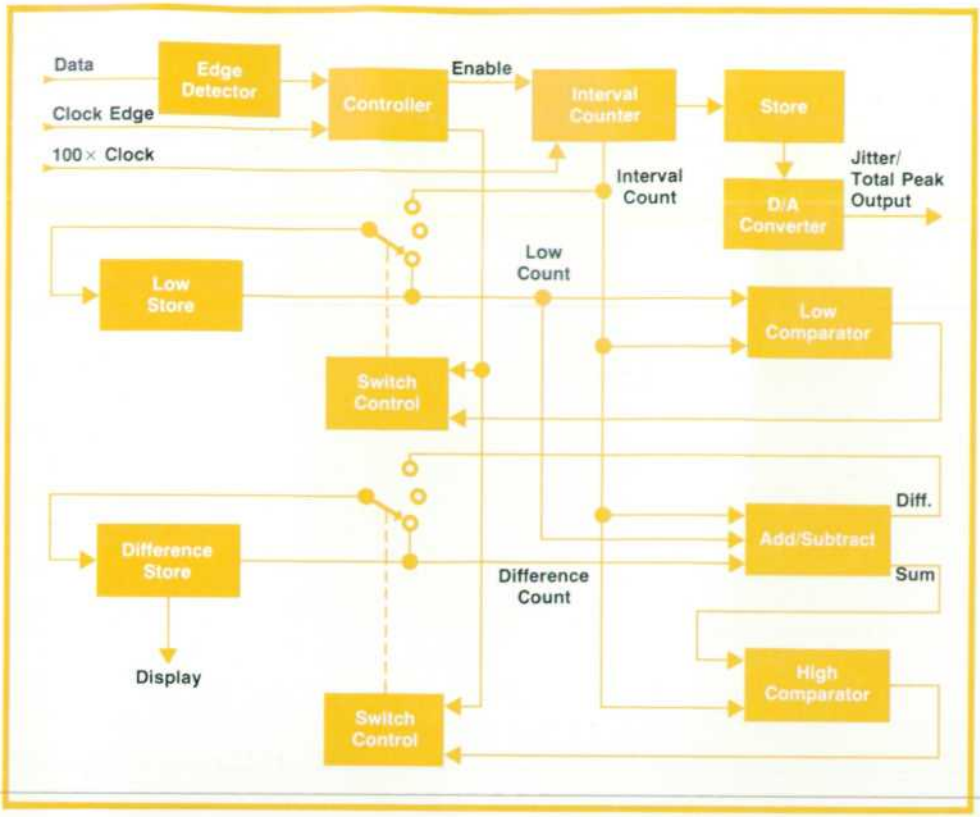

Fig. 7. *Block diagram of jitter measurement circuit.*

Jitter/Total Peak Measurement

Jitter is measured by counting 100× clock pulses (100× faster than the clock rate) from a data edge to the clock edge, which normally occurs half way through the data bit period. The difference between the lowest and highest values counted during the test interval is a measure of jitter.

This is carried out by the system diagrammed in Fig. 7. Upon sensing a positive-going data edge, the edge detector generates a start pulse for the controller which in turn enables the interval counter to start totalizing 100× clock pulses. The next clock edge stops the count, the exact count depending upon the position of the data edge with respect to the clock edge.

The count thus obtained is compared to the count in the low store register. If the count in the interval counter is the lesser of the two, it is loaded into the low store register in place of the count already there (the register was loaded with the first interval count at the beginning of a test).

The count in the interval counter is also compared to the sum of the counts in the low store and difference store registers. If the new count is greater than this sum, which represents the maximum count that has been received, the number in the low store register is subtracted from the new count and the result is loaded into the difference store register.

The difference register now contains a number that corresponds to jitter directly in terms of percent of clock period (100 counts equals 100%). The contents of this register are displayed to give readings of jitter.

Total peak distortion (jitter plus bias) is measured by switching the edge detector to respond to both positive- and negative-going data edges. The number in the difference store thus reflects both the edge variations (jitter) and the relative positional difference between positive and negative edges (bias).

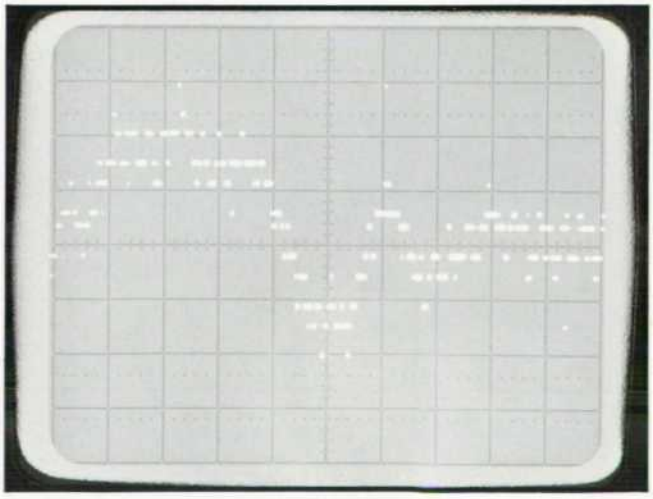

Fig. 8. *Oscillogram of analog waveform available at JITTER/ TOTAL PEAK output. The nature of the waveform helps determine the cause of the jitter (the waveform appears quantized because it is made up of discrete samples).*

An additional feature of the system is that the interval counter contains continuously up-dated information about the position of data edges with respect to the clock. When the data-edge-to-clock count is complete, this information is converted to an analog voltage and presented at a front-panel connector, generating a waveform that corresponds to the movement of data edges with respect to the clock. The resulting waveform can be viewed on an oscilloscope, as shown in Fig. 8, as an aid in determining the source of the jitter. This output (JITTER/TOTAL PEAK) is calibrated so 1 volt out represents 10% distortion.

When the Analyzer is measuring total peak distortion, the oscilloscope's vertical deflection switches back and forth from the voltage corresponding to the positive-edge-to-clock interval to the voltage corresponding to the negative-edge-to-clock interval, tracing out two waveforms. The separation between waveforms is proportional to bias.

When the Analyzer is used with an external clock, the jitter measurement circuits are disabled since no 100× clock would then be available. Jitter in synchronous systems, where an external clock most likely would be used, is usually less than 1% and is not a problem at the modem output. Jitter is primarily of concern with asynchronous systems where it may be as much as 20%.

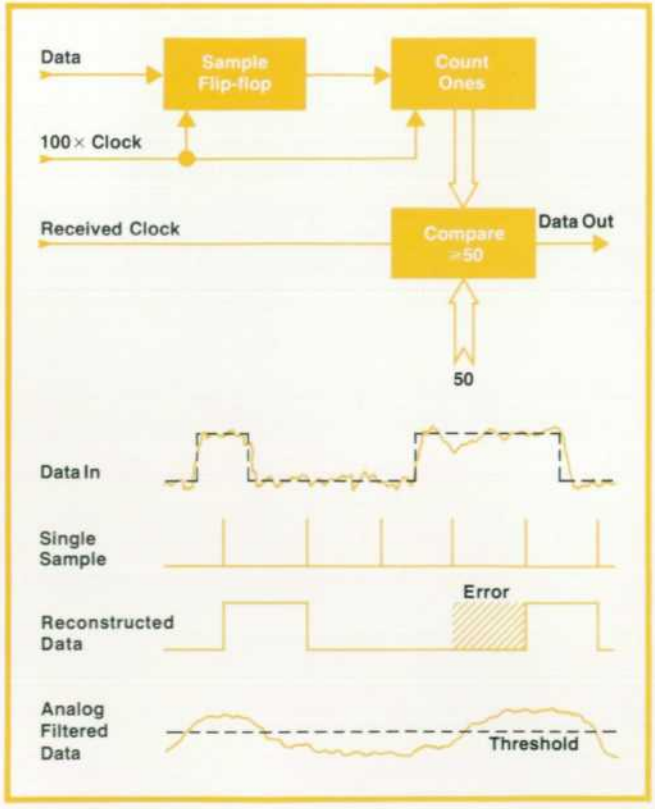

Fig. 9. *Statistical filter reduces effects of noise.*

Statistical Filter

A switchable filter is included in the incoming data path. Usually, the filter in the modem cleans up a noisy signal. Whether or not it is performing satisfactorily can be determined by comparing bit-error-rate measurements with the Analyzer's filter switched out to those made with the filter in.

The filter has to accommodate asynchronous bit frequencies from 75 to 9600 bps. As shown by the waveform in Fig. 9, analog filtering does not obtain reliable results so the filter used is a digital type that uses majority logic to decide whether a particular bit is a one or a zero. Each bit is sampled 100 times. Each time the sample is above the median threshold, it increments a counter. At the end of the bit, the comparator checks to see if 50 or more counts have accumulated. If so, that data bit is classed as a one. Otherwise it is a zero.

When the filter is disabled, the incoming data is sampled once in the center of each bit to determine whether it is a one or a zero.

Stable Clock

As mentioned previously, stable clock pulses are derived in the bit synchronizer. The heart of the bit synchronizer is a voltage-controlled 5.76 MHz LC oscillator that can be electrically tuned over a ±0.5% range. As in the case of the transmitter, dividers derive the various clock rates.

As shown in Fig. 10, the oscillator frequency is controlled by a phase detector, an RS flip-flop that is triggered on by a data edge and off by the next clock edge. This not only ensures that the instrument locks to the incoming bit rate, but it also places the clock edge midway in a bit period.

The output of the phase detector is averaged by a low-pass filter that is a compromise between stability (long time constant) and acquisition speed. Loop bandwidth is 3 Hz, which is well below the rate of change of jitter and other parameters to be measured with reference to the clock, but which permits fast acquisition from the operator's point of view.

The filter's time constant, however, would allow the oscillator to drift off frequency during the long pseudorandom sequence, which has long strings of bits in a row where no data edges occur. These would cause the phase detector to remain in either one of its two stable states, pulling the oscillator off frequency. Lengthening the filter's time constant to prevent drift from this source would seriously hamper acquisition speed.

This problem was solved by using a switch that disconnects the phase detector output, allowing the filter capacitor to retain its present voltage until the switch closes again. The switch is controlled by a comparator circuit that monitors the internal states of the input feedback shift register and turns off the

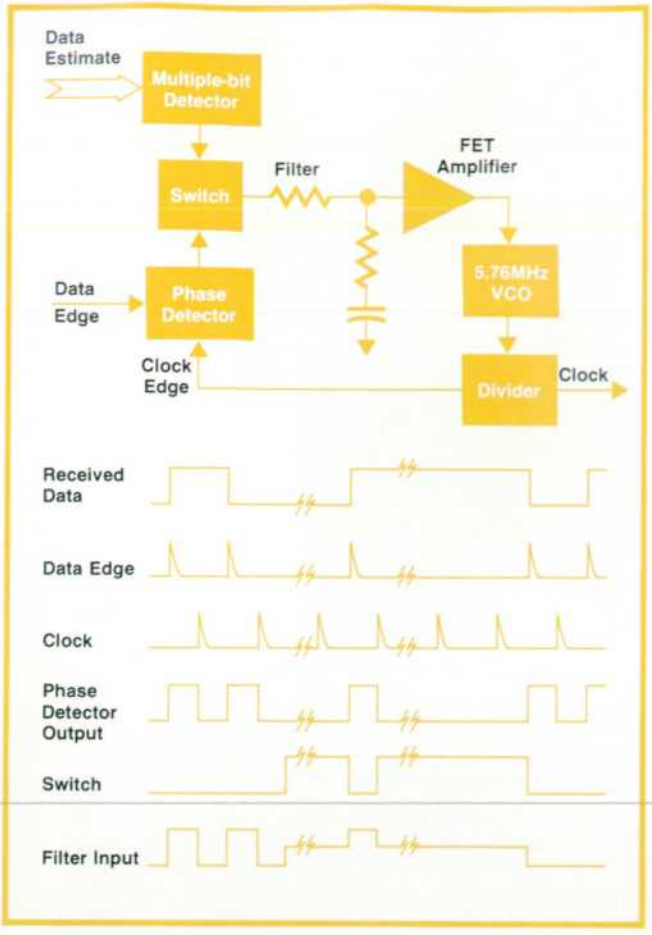

Fig. 10. *VCO control loop.*

switch whenever it detects that the register is about to output a long string of ones or zeros.

This arrangement reduces jitter during the long pseudorandom sequence from 15% or so to less than 1%. Another indication of the effectiveness of this circuit is that if the data input is removed, the oscillator remains in the correct phase for more than 5 seconds, equivalent to more than 375 bits at the slowest rate.

Autorange Control

The traditional way of displaying bit-error rate is as a number times 10 raised to some negative power ($A \times 10^{-x}$). This method is used in the Data Error Analyzer. It was also desired to display the count in progress which would indicate how much of the test interval had elapsed. This is accomplished by using the exponent in the display to indicate the number of data bits received in decade steps. At the conclusion of the test, the display then shows the overall bit-error rate properly ranged.

The autoranging system is shown in Fig. 11. Clock pulses are totalized in nine decade counters connected in tandem. The output of each of these counters goes to a selector. Initially, the output of the first decade is selected. As the clock count goes through 10, the first decade's output passes through the selector to increment the exponent counter. The exponent counter then shifts the selector to the next decade. This procedure repeats for each decade.

The count in the exponent counter is displayed continuously as the exponent. It is also compared to the number selected by the front-panel EXPONENT RANGE switch and when they become equal, the comparator stops the measurement.

In the automatic mode, the exponent counter receives a signal from the bit-error counter when 98 errors have been counted. It then stops the measurement when it receives the increment signal from the clock counter at the next decade change.

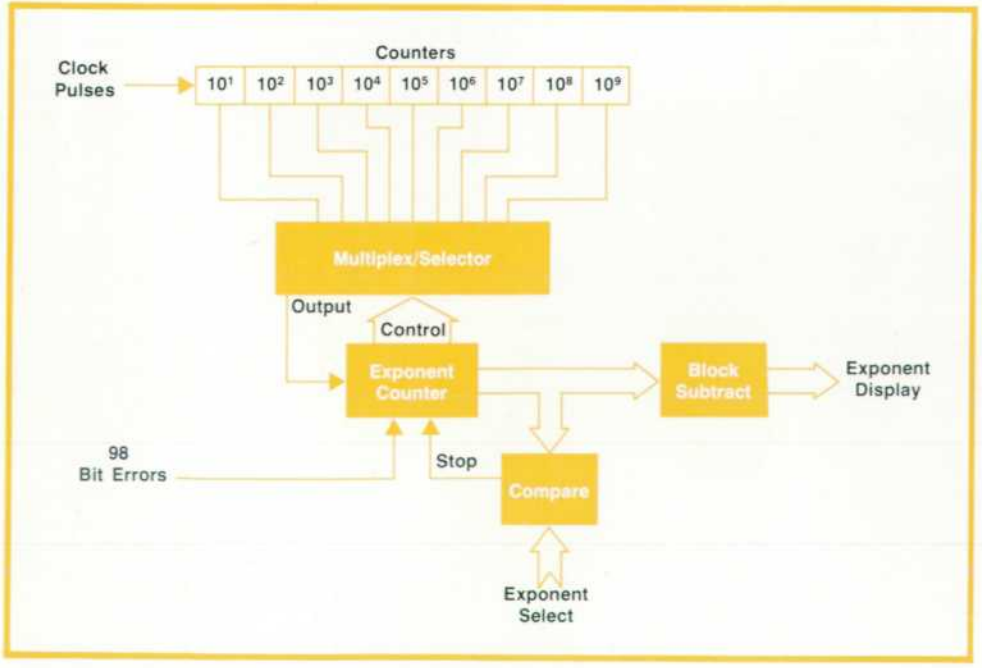

Fig. 11. *Autorange circuit selects appropriate exponent to terminate test interval automatically.*

The exponent counter's output passes through the block subtract circuit before display. This circuit subtracts 3 from the exponent count when the instrument is displaying block error rate, giving block error rate directly.

Acknowledgments

Appreciation is expressed to Al Knack for the innovative mechanical design, to Rick Vestal for many hours of patiently taking data on and with the Model 1645A, to Maxine Cheyney whose talents were essential to modularizing a complicated system, and to Eddie Donn whose creativeness was responsible for many of the basic ideas.

SPECIFICATIONS

HP Model 1645A Data Error Analyzer

Bit Rate

INTERNAL TRANSMITTER

BITS PER SECOND: selectable 75, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600.

CRYSTAL FREQUENCY: 5.76 MHz ±0.03%; <0.01% jitter.

INTERNAL RECEIVER (with bit synchronizer)

RATE: dc to 9.6 kbps.

TIME TO LOOP LOCK: 2 s max at <0.01 error rate.

EXTERNAL TRANSMITTER and RECEIVER FREQUENCY: dc to 5 MHz.

Data Outputs/Inputs

REAR PANEL

INPUTS: backward channel data, external transmitter clock, and external receiver clock require TTL level; maximum input 5.5V.

OUTPUTS: bits lost and transmitter sync provide TTL levels; internal transmitter clock provides >2V into 50 ohms.

MULTIPIN CONNECTORS: RS 232C connector and interface levels for interfacing with standard communications systems. Printer output provides TTL level outputs in BCD 8421 code.

FRONT PANEL

INPUT: data input requires TTL levels; maximum input, 5.5V.

OUTPUTS: receiver sync, 16 bits before error, and event provide TTL levels; data output provides >2V into 50 ohms. Jitter/total peak analog output provides 1V p-p for 10% of p-p distortion from waveform causing jitter.

General

DIMENSIONS: 5.25 in H, 16.75 in W, 11.25 in D (133 × 416 × 286 mm).

WEIGHT: 22 lb (10 kg).

POWER: 115 or 230 Vac, 48 to 440 Hz, 150 VA max.

OPERATING ENVIRONMENT

TEMPERATURE: 0°C to +55°C.

HUMIDITY: to 95% relative humidity at 40°C.

ALTITUDE: to 15,000 ft. (4600 m).

VIBRATION: vibrated in three planes for 15 minutes each with 0.010 in (0.25 mm) excursion, 10 to 55 Hz.

PRICE IN U.S.A.: 1645A, $2150.

MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
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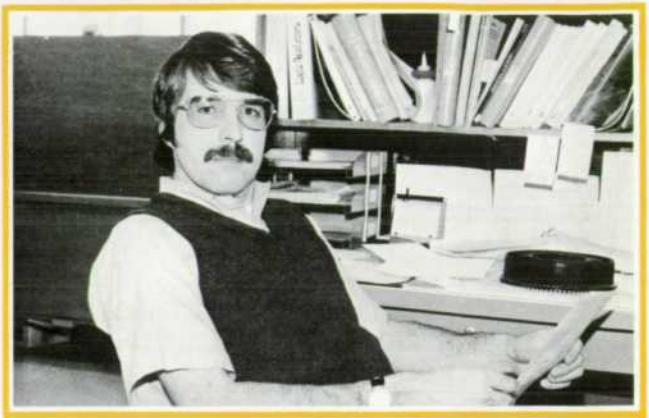

Jeffrey R. Duerr

Joining HP in 1970 after two years in aerospace communications, Jeff Duerr initially worked on the 6940A/1900A programmable pulse generator system. Then, as project leader on the 1645A Data Error Analyzer, he combined engineering with the marketing research needed for developing an international product. He is now a sales engineer in the Colorado Springs Division. A native of Cleveland, Jeff earned a BSEE degree at the University of Rochester and an MSEE degree in communications from the State University of New York at Buffalo (1967). Jeff likes to spend weekends backpacking in summer and skiing in winter and he enjoys photography and blue-grass banjo picking all year around.

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