DIGITAL STORAGE OSCILLOSCOPE OS4020

Instruction Manual

GOULD

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Introduction

Section 1

The Gould OS4020 providing a combination of Digital Storage and Realtime, caters for measurements from D.C. to 10MHz with a flicker-free display of a full cycle down to 0.005Hz.

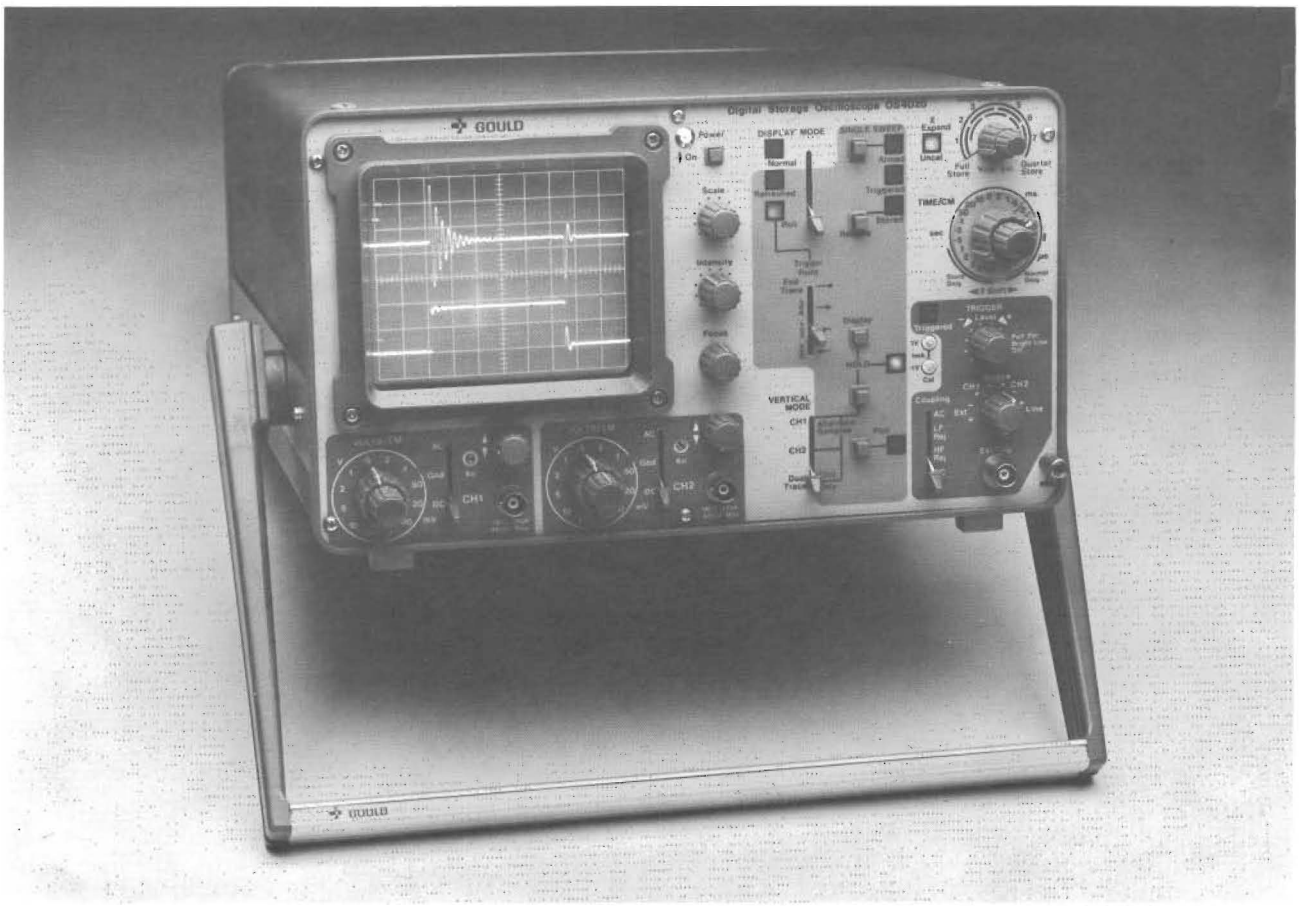
The digital method of storage offers many advantages, notably the facility of pre-trigger viewing, simultaneous display of a stored and realtime signal, absence of deterioration of the stored display with time.

The primary modes 'Normal', 'Refreshed' and 'Roll' give an optimum choice when observing repetitive waveforms in realtime, low frequencies, transients, pre-trigger information or long term phenomena.

The 4K length store is sufficient to retain all stored traces in detail and allows up to 40 times post storage X expansion to view the detail of any part of the trace.

Careful attention to the ergonomic design allows the OS4020 to be operated with ease similar to a conventional oscilloscope with the storage functions clearly segregated. The additional facilities of having the internal clock available or to provide an external clock, permits more than one OS4020 from operating in parallel or in series. An external clock can be used to define the timebase characteristic. The optional 4022 unit provides an analogue output suitable for X-Y or T-Y chart recorders and a digital interface to input or output data and control majority of the oscilloscope functions externally.

The OS4020 is ideally suited for viewing transient waveforms, e.g. in medical, dynamic testing, vibration and pulse testing applications. Comparing realtime or stored waveforms with ones previously obtained.



Specification

Section 2

2.1 DIGITAL STORAGE OSCILLOSCOPE OS4020

DISPLAY

8 x 10cm rectangular. CRT operating at 4kV. Illuminated graticule.

VERTICAL DEFLECTION

Two identical input channels.

Bandwidth: DC–10MHz in NORMAL mode.

Sensitivity: 5mV/cm to 20V/cm in 12 ranges. Uncalibrated fine gain control gives continuous adjustment between ranges.

Accuracy: ±3% in calibrated positions.

Input Impedance: 1MΩ/28pF.

Input Coupling: AC–GND–DC

Maximum Input: 400V DC or pk AC

TIMEBASE

Normal Mode

Range: 1μs/cm to 20 sec/cm in 23 ranges.

Accuracy: ±3%

X Expansion: Continuously variable from x1 to x10

Refreshed and Roll Modes

Range: 0.2ms/cm to 20 sec/cm in 16 ranges (Uncal LED flashes to indicate unavailable range selected).

Accuracy: ±3%

X EXPANSION

Calibrated Quadrant Expansion

Display of any one of 7 overlapping quadrants of full store. Calibration (x4 or x5) equal to two steps faster on timebase range, indicated by additional cursor line.

Uncalibrated: As NORMAL mode.

TRIGGER

Source (slope): CH1 (±), CH2 (±), Ext (±) or line (±)

Coupling: AC, LF Rej., HF Rej., DC

Sensitivity: Internal 2mm approx., DC–2MHz (1cm @ 10MHz)
External 1V approx., DC–2MHz (5V @ 10MHz).

Bright Line (Normal)/Auto Trigger (Refreshed) Mode, switchable.

DIGITAL FUNCTION (Refreshed and Roll modes)

Sample Rate: 2MHz (0.5μs/sample) at 0.2ms/cm (5μs/cm expanded), reducing proportionately with timebase range.

Store Size: 4096 x 8 bits

Vertical Resolution: Approx. 30 steps/cm.

Horizontal Resolution: Approx. 400 samples/cm unexpanded.
Approx. 100 samples/cm on 5 sec/cm quadrant expanded and all decade multiples.
Approx. 80 samples/cm on 2 & 1 sec/cm quadrant expanded and all decade multiples.
X10 expansion via variable control reduces resolution by factor of 10 on all ranges.

Dual Trace or Lock

Alt. Samples: The resolution of each trace is half the figure quoted above.

Dot Joining: Linear interpolation between samples.

Capture Modes

Refreshed: Stored data and display normally updated by triggered sweep.

Roll: Stored data and display normally updated continually.

Single Shot: Freezes store at end of triggered sweep.

Hold: Freezes store immediately.

Hold Alt. Samples (CH2): Freezes alternate samples of stored data to:
(i) Retain CH2 in dual channel mode only.
(ii) Produce one frozen trace and one current trace in single channel mode.

Pre-trigger Storage: Available in ROLL mode only, switchable for ¼, ½, ¾ & FULL STORE pretrigger.

ADDITIONAL FACILITIES

Calibrator: Positive going square waves of 0.1V and 1V ±2% at approximately 2KHz. Shorting between the CAL pins produces a 1mA ±2% current in the shorting link.

External Control (TTL compatible)

External Clock Input: Edge sensitive input, replaces the internal write clock. A negative edge causes one sample to be written into store followed by an increment of the Write Address Counter. Useful frequency range DC to <1MHz.

Ready: An output which forms a simple two wire handshake with external clock input if required. HI level to indicate the instrument is ready to accept a new clock edge.

Clock Out: An output at the write rate of the instrument, negative edge when a write is being initiated. May be used to synchronise a second oscilloscope.

Gate: An output signal which is LO during a write sweep of the instrument. May be used to trigger a second instrument for four trace operation.

INT/EXT. CK: Input, LO to select external clock.

SUPPLIES 115, 220, 240V ±10% by switch.
100V ±10% by tap change.

Specification

Section 2

SIZE 17.8 x 31.2 x 41.7 (7" x 12" x 16½").

WEIGHT Approx. 11kg (24¼lb).

TEMPERATURE RANGE

Operating: 0 to 50°C.

Full Specification: 15 to 35°C.

ACCESSORIES SUPPLIED

Handbook PN 43692
2 x Lead PL44 BNC - Croc. Clip.
2 x Lead PL43 BNC - BNC.

OPTIONAL ACCESSORIES

2.2 OPTION 4022

ANALOGUE OUTPUTS - via BNC connectors

Channels 1 and 2

Amplitude 100mV per cm of screen height
Bipolar with Ov corresponding to centre of screen

Accuracy Output voltage per cm of display ±3%
Output to input voltage (cal.) ±3%.

X Ramp

Amplitude 100mV per cm of screen width
Positive ramp resetting to Ov

Accuracy Output voltage/cm of display ±3%
Output voltage/unit time recorded ±3%

Time output accuracy of Y Channel outputs ±1% (record to replay ratio)

Output Impedance CH1, CH2 and X ramp approx 100Ω/0.1uF
Continuous short circuit protected.

Readout

Range Internal clock 100s/cm - 1ms/cm in 1-2-5 steps. External clock (Displayed sample rate) 0 to 1MHz continuously variable. Rephased by internal 2MHz clock. (Equiv. - to 0.4ms/cm).

Bandwidth DC - 16kHz (−3dB)

Controls

Plot Mode Manual (or Remote) start, autostart or continuous read-out.

Start-up Delay Delay from start command to initiation of read-out cycle. Range 100ms to 1sec.

Inputs External plot Rate clock, TTL, positive edge active.
External clock select, TTL, low level active.
Remote start, TTL, negative edge active.

Outputs

Contacts Isolated single pole contact which closes from start command to end of read-out cycle.

Rating 100V DC 250mA DC, 10W DC

Isolation 400V Max.

Plot Marker TTL High commencing at the end of the delay, for the duration of the read-out cycle.

Ready TTL signal for use in conjunction with external clock. Goes LOW on reception of clock edge, returns HIGH when ready to accept another clock edge.

DIGITAL I/O SIGNALS

On board storage/buffering for external read and/or control of the following oscilloscope signals.

Oscilloscope Mode (Normal/Refresh/Roll)
Timebase Range
Stored Trigger Point
Channel Selection
Full Store Data
Arm
Stored (read only)

Connection via 25 way D type connector.

3.1 SUPPLIES

The instrument is normally despatched from the factory with the supply range switch on the rear panel set to the 240V (±10%) range. Check that this is set correctly before connecting to the supply. Note that the correct fuse for the two high voltage ranges, 220V and 240V, is 500mA Slo-Blo (20mm) Advance Part No. 33685. If the 115V range is selected the fuse should be changed to a 1A Slo-Blo Advance Part No. 34790.

NOTE: DO NOT CHANGE THE SUPPLY RANGE SWITCH WITH THE INSTRUMENT CONNECTED TO THE SUPPLY.

SAFETY

THE INSTRUMENT IS DESIGNED TO BE USED WITH THE FRAME EARTHED AND IT IS IMPORTANT THAT THE APPROPRIATE (GREEN/YELLOW) CONDUCTOR OF THE SUPPLY LEAD PL98 IS CONNECTED TO A SUITABLE EARTH.

While the instrument does not rely on forced air circulation, it should not be operated at elevated temperatures if the natural convection cooling is restricted, particularly at the rear of the instrument.

The instrument is switched on by pressing the POWER button when the associated L.E.D. indicator should light. The button is self-locking and the instrument is switched off by pressing the button again.

3.2 C.R.T. CONTROLS

These controls are grouped to the right of the c.r.t. display.

Intensity This is used to set optimum trace intensity depending on ambient lighting conditions.

Focus Used to obtain finest possible trace width.

Scale The un-illuminated graticule is easily visible under normal lighting conditions. Graticule illumination is usually only required under low ambient light conditions or when photographically recording the display. The intensity will depend on the film speed, aperture and exposure time being used. The graticule has 0, 10, 90, 100% lines marked to assist in rise time measurement.

3.3 Y CHANNEL CONTROLS

These controls are grouped beneath the c.r.t. display. The input signal is applied to the CH1 or CH2 BNC input socket.

3.3.1 COUPLING

For direct connection of the input signal, set the associated AC–Ground–DC input lever switch to DC.

For capacitive coupling of the input signal through an internal 0.1μF 400V capacitor, set the lever switch to AC.

NOTE: When examining low amplitude a.c. signals superimposed on a high d.c. level, the lever switch should be set to AC and the sensitivity of the Y amplifier increased.

To locate the baseline, set the lever switch to the 'ground' setting. At this setting, the input signal is open circuit and the input of the amplifier is switched to ground.

3.3.2 SENSITIVITY

Set the VOLTS/CM switch to a suitable setting. To minimise pick up at sensitive settings, it is essential to ensure that the ground lead connection is near to the signal point.

If necessary, adjust the concentric VARIABLE control.

NOTE: The range of the VARIABLE control is approximately 3:1 so that its full adjustment overlaps the adjacent lower sensitivity range. Except at the CAL setting, the VARIABLE control is uncalibrated.

3.3.3 SHIFT

For vertical shift of the trace, adjust the Y shift controls (identified with vertical arrows).

Bal.

The preset balance minimises vertical movement of the CH1 or CH2 traces when the inputs are grounded and the attenuator switch is moved between the 0.5V/cm and the 0.2V/cm position and requires infrequent adjustment (see section 5.3.4).

3.3.4 Y MODE

The three position switch allows single channel display of the selected channel CH1 or CH2, or dual channel display when Dual Trace is selected.

3.4 TIMEBASE AND TRIGGER

All controls associated with the Timebase and Trigger facilities are grouped together on the right hand side of the panel.

3.4.1 TIME/CM, EXPAND AND SHIFT

The timebase sweep speed (i.e. the time scale of the horizontal axis) is determined by the brown cursor of the TIME/CM switch. (see Display also Expansion). Changing timebase range while capturing important data in REFRESHED or ROLL modes may select an indeterminate range between positions causing loss of data.

3.4.2 VARIABLE X EXPAND (SEE ALSO QUADRANT EXPANSION)

The time scale can be adjusted to any intermediate setting by use of the concentric X expand control. This provides a calibrated sensitivity at the X1 detent position at the end of travel with a fully variable uncalibrated range to X10. The Uncal L.E.D. indicates when this control is switched away from the X1 position.

3.4.3 X SHIFT

The X shift control, identified with horizontal arrows is used to centre the display or locate any part of the trace in the expanded condition. This is a dual action control, providing fine adjustment over a small angle of rotation and coarse adjustment over the full rotation.

3.4.4 TRIGGER

The TRIGGER SOURCE switch selects one of the four signals, Internal CH1, Internal CH2, External or Line. The TRIG. COUPLING selects wideband DC or AC coupling. The AC coupling cuts off at approx. 1.5Hz.

The L.F. Reject position limits the trigger sensitivity below approx. 15kHz while the HF Reject is AC coupled but limits sensitivity above approx. 34kHz. The source switch also selects the slope, positive or negative going, to cause trigger when the signal passes through the level set by the TRIGGER LEVEL control. The associated L.E.D. indicates when trigger signals are present. This will flash at low repetition rates and remain on at faster rates. However, it may not indicate trigger signals above 5MHz.

In the Normal mode of operation, the timebase will free run automatically in the absence of trigger signals. This provides a 'bright line' display to assist in trace location. With this facility operating, false triggering may occur if the trigger frequency is less than approx. 40Hz. In the Refresh and Roll modes of operation, an auto-trigger facility is provided which will operate if the instrument has waited more that ¼ sec for trigger. This assists in trace location but may cause false triggering on signals less than 10Hz.

Bright line and auto trigger are disabled by pulling the TRIGGER LEVEL knob.

3.5 STORE CONTROL

All controls associated with the storage facility are grouped together and distinguished with blue coding. The DISPLAY MODE lever switch selects the three modes of operation NORMAL, REFRESHED, or ROLL, the associated L.E.D. indicating the operating mode.

3.5.1 NORMAL MODE

In this mode the instrument operates as a conventional oscilloscope and the store controls do not influence the display. This mode of operation is available for all medium and fast sweep rates, 0.5s/cm to 1μs/cm, but if slower sweep rates are selected, the instrument automatically selects the Refreshed mode.

3.5.2 REFRESHED MODE

If the instrument is displaying a trace in the Normal mode and the mode switch is moved to REFRESH, the display essentially will be unchanged. However, in this mode and in ROLL, the display is generated via the digital signal path and a small amount of step structure may be detected on the trace.

The display is triggered as in the Normal mode but in the absence of trigger (with auto-trigger not selected) the previously stored trace is displayed continuously. This has the advantage of providing a flicker-free display of signals with low repetition or trigger rates even if a fast timebase range is selected. The display is updated (refreshed) by each trigger signal which occurs while the instrument is not engaged in updating the store. A further advantage over Normal operation is the availability of very slow sweep rates with continuous flicker-free display of the sweep as it is written or re-written.

The Refreshed mode can be used over the range 20 sec/cm to 0.2μs/cm (full store display). The UNCAL, L.E.D. will flash if a faster range is selected.

3.5.3 ROLL MODE

Selection of this display mode provides a form of free running timebase not found on a conventional oscilloscope. Incoming data is fed continuously to the store. As the display is continuously updated from the right, the trace appears to be moving or rolling to the left similar to the view through a 10cm window of a strip chart recorder trace.

As information is being continuously written into store, at a trigger instant, the store will contain only pre-trigger information. Thus, by using the single shot facility (see Pre-Trigger Storage), pre-trigger information even from transient signals may be stored and displayed.

This mode of display is well suited to direct display of low frequency signals using comparatively slow sweep speeds.

As with the Refreshed mode, the Roll mode can be used on ranges 20 sec/cm to 0.2 msec/cm.

3.5.4 STORE AND RELEASE (REFRESH MODE)

These buttons operate in the Refreshed and Roll modes. Operation of the ARM button in the Refreshed mode retains any current sweep or the next full triggered sweep as a stored display, unaffected by subsequent trigger signals. L.E.D. lamps indicate the single shot sequence followed. The Armed lamp shows that the circuitry has been primed by operation of the button. This lamp goes off and the Triggered lamp comes on during a sweep. Finally this indication is replaced by the Stored lamp coming on when the stored sweep is complete. The sequence and resultant display is similar to operation of the single shot facility on a conventional storage oscilloscope after erasing any previous trace. The OS4020 has no need for an erase facility as the entry of new data into the store automatically rejects previous data.

Subsequent operation of the ARM button will repeat the single shot storage cycle, updating the display as required.

Operation of the RELEASE button will return the

instrument to the mode selected by the DISPLAY MODE switch.

PRE-TRIGGER STORAGE (ROLL MODE)

The effect of operation of the STORE button in the ROLL mode depends on the setting of the STORED TRIGGER POINT SWITCH. With this switch in the top (End Trace) position, the rolling trace will continue after operation of the STORE button until a trigger is received when the display will be frozen. Thus it shows a full trace of signal prior to trigger, i.e. trigger is at end of the trace, not at the beginning as on a conventional oscilloscope, mesh storage type or otherwise.

Operation of the STORE button at the¾ trace setting of the STORED TRIGGER POINT switch allows the display to roll on for ¼ of a sweep beyond the next trigger. The resultant frozen display shows ¾ of the trace occuring before trigger and ¼ after trigger. The actual trigger point on the waveform, ¾ from the left hand side of the screen, is shown by a bright-up spot. It may be necessary to adjust the Intensity setting to obtain contrast to see this spot.

Selection of the ½ or ¼ trace position of the Stored Trigger Point allows the proportion of pre-trigger display on subsequent storage cycles to be varied accordingly.

Note that the instrument will not accept trigger until the requested amount of (pre-trigger) information has been entered into the store. This ensures that all old information is displaced from the store. Thus if the instrument is taken straight from STORED to ARMED, by pressing the ARM button, the ARMED LED will flash to indicate that the command has been accepted, but the instrument is not available for trigger. When the correct amount of information has been entered into the store, the trigger is enabled and the ARM light will steady and remain on until the trigger is received.

The ability to display a trace of the incoming waveform prior to or about trigger, can be used up to sweep speeds of 0.2ms/cm, irrespective of the trigger rate. These present a meaningless display while free running prior to trigger in the Roll mode but are relevant when stored.

3.5.5 DISPLAY HOLD

Operation of the DISPLAY HOLD button prevents change of the data held in the store. It can be used in the Roll mode to instantaneously freeze the display if a feature of interest appears on the screen. Alternatively the store can be locked in the Refreshed or Stored modes. Subsequently the instrument can be used as a conventional oscilloscope in the Normal mode but the original locked display is recalled when returned to the Refresh mode. The DISPLAY HOLD button latches mechanically. To enable the instrument to be free to update the store as usual, the button should be pressed again to release. An L.E.D. indication warns that the DISPLAY HOLD or HOLD Alternate Sample button is pressed. It should be noted that movement of function switches after a display has been locked in the Roll mode, can disturb the display, particularly shifting the start point of the trace and the bright-up trigger marker spot if relevent. This disturbance is not corrected when the function switch is returned to Roll.

3.5.6 HOLD ALTERNATE SAMPLES

All the store functions described above operate irrespective of the setting of the 'Y' Mode switch. This is, they apply equally to the single trace display of CH1 or CH2 and the dual trace display of CH1 and CH2. This is not so for the HOLD ALTERNATE SAMPLES button. When this condition is applied in the Refreshed mode for single trace displays (CH1 or CH2), the effect is to produce a dual trace display. One trace is stored and the other free to follow updating signal inputs. This simultaneous display of stored and the incoming signal can be used to compare 'before' and 'now' traces or even to compare traces taken at different sweep speeds. (once a trace is stored its display is not altered by the changing of the TIME/CM switch). Operation of the HOLD ALTERNATE SAMPLES in the dual trace, CH1 & CH2, mode has the effect of freezing the CH2 trace, leaving CH1 free to respond to current signals.

Once the HOLD ALTERNATE SAMPLES button is pressed, it is possible still to go from Refreshed to Store and then to Release to Refreshed with the free trace following the mode selected, but the frozen trace remaining as when lock button was pressed. Operation of the HOLD ALTERNATE SAMPLES button in the ROLL MODE is less meaningful than in the Refreshed mode. Half of the display is frozen as before, giving a dual trace effect to single channel displays or locking CH2 only on dual trace displays. However, the frozen trace continues to move across the screen from right to left with display lost from the left appearing on the right.

3.6 DISPLAY QUADRANT EXPANSION

In both refresh and roll modes, X expansion and shift of the display is possible whether the display is "live" or "frozen" by HOLD or STORE. As in the normal mode the X EXPAND control allows variable expansion in the range X1 to X10. In addition, the DISPLAY SELECT control, which is only operative in these digital modes, will expand the trace to display store segments at the time/cm indicated by the offset green cursor on the TIME/CM control knob,i.e. two ranges faster than the recording rate. Each segment is approximately one quarter of the store, with sequential segments available for selection overlapping by approximately 50%. This overlap allows a point of contact which appears for example at the end of one segment to be positioned near to the centre of the screen at the next segment. When the trace is expanded by this method, the DISPLAY SELECT switch has the effect of a calibrated offset from the start of trace.

FULL STORE TIMEBASE RANGE	X-RESOLUTION SAMPLES/cm		OFFSET (cm) OF EACH SEGMENT EXPANDED (GREEN) CURSOR SCALE							
	Full Store	Segment	1	2	3	4	5	6	7	Segment No.
			0	512	1024	1536	2048	2560	3072	Starting address (decimal)
20, 2, 0.2 s/cm 20, 2, 0.2ms/cm	400	100	0	5.12	10.24	15.36	20.48	25.60	30.72	
50, 10, 5, 1, 0.5, 0.1s/cm 50, 10, 5, 1, 0.5, 0.1ms/cm 50μs/cm	400	80	0	6.4	12.8	19.2	25.6	32.0	38.4	

Fig. 3.1 Table of Quadrant Offsets

Please note that as the expansion produced varies accordingly to the timebase range selected for recording, the offset is similarly affected as shown in the Table of Fig. 3.1

Please note also that the DISPLAY SELECT operates on the display only and has no effect on the sampling rate of the instrument.

3.7 ALIAS EFFECTS

In the Refreshed and Roll modes, the instrument uses a sampling system to examine the incoming waveform. Any such system can give misleading results known as alias effects if the input signal has a significant component with a frequency approaching or above the sampling frequency. Fig. 3.2 shows the effect of the sampling process on a triangular input waveform (trace A).

Trace B shows the effect of sampling at a frequency close to four times that of the input if the display is formed by a series of dots. It will be seen that this can become a meaningless jumble. However, trace C shows the same sampled waveform reconstructed with the dot joining system employed in the 4020. Thus the display is formed by a series of straight lines, joining the successive sampled levels rather than a dot at each level, usually used on reconstructed displays. The dot joining approach is seen to retain the essential nature of the input waveform without ambiguity. This is particularly important as the horizontal dot density is much closer than that shown on the diagram. However, if the sampling rate is reduced further, the essential nature of the waveform will be lost. Trace D shows the effect of a sampling rate close to half the input frequency and Trace E the effect when the frequencies are nearly equal. In the latter case the display appears as the input form but at reduced frequency. The frequency division is the principle on which sampling oscilloscopes operate, and can cause confusion in this case.

The 4020 takes approx. 4000 samples per sweep. These are shared between traces on dual channel or alternate locked modes of operation. Assuming that the sampling rate should exceed the input signal frequency by a factor of between 4 or 5, the following table shows the maximum frequency which can be viewed on each range.

Time/cm Range	Single Channel	Dual Channel or Alt.Locked
0.2ms/cm	400kHz	200kHz
0.5ms/cm	200kHz	100kHz
1 ms/cm	100kHz	50kHz
2 ms/cm	40kHz	20kHz
5 ms/cm	20kHz	10kHz
10ms/cm	10kHz	5kHz
20ms/cm	4kHz	2kHz
50ms/cm	2kHz	1kHz
0.1s/cm	1kHz	500Hz
0.2s/cm	400Hz	200Hz
0.5s/cm	200Hz	100Hz
1 s/cm	100Hz	50Hz
2 s/cm	40Hz	20Hz
5 s/cm	20Hz	10Hz
10s/cm	10Hz	50Hz
20s/cm	4Hz	2Hz

The above table shows the order of frequency which can cause mis-leading displays. The actual amount of distortion depends on both the frequency and the waveshape involved. Individual peaks of sinusoidal signals can be -3db at a frequency approx. 10% above those shown above.

If alias effects are suspected, it is recommended that the fastest possible sweep speed is selected. Repetitive

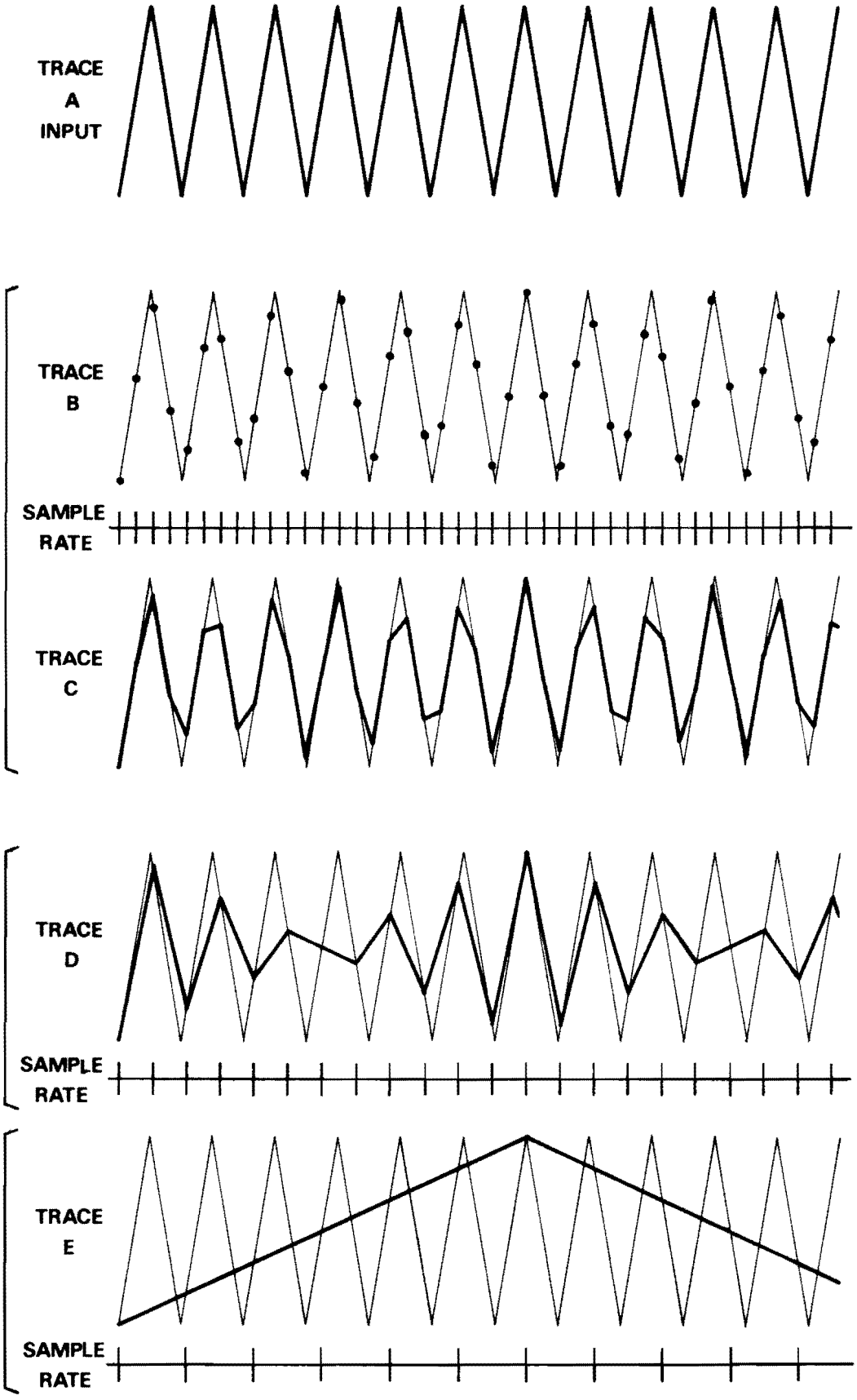


Fig. 3.2 Alias Effects

signals are best viewed in the normal mode if possible, before comparison with a refreshed trace.

It should be noted also that the sampling system will not detect narrow transients which occur between samples.

3.8 ADDITIONAL FACILITIES

3.8.1 CAL

These pins provide d.c. coupled positive-going square waves of 0.1V and 1V ±2% amplitude at approximately 1kHz frequency for calibration checks, shorting between the CAL pins will produce a square current wave-form of 1mA in the shorting link. This can be used for current probe calibration.

3.8.2 ADDITIONAL CONTROL SIGNALS

On the standard instrument, these signals appear at the sockets on the blow moulding at the rear of the instrument. If the instrument is fitted with a 4022 option, these signals appear on the misc. I/O connector as shown in Fig. 3.5

a) Gate Output - This is a TTL output which goes LO during a write sweep when the instrument is updating the information in store. It may be used to trigger a second oscilloscope for four trace operation. It is comparable with the Gate Output signal of a conventional oscilloscope.

b) Clock Output - TTL output at the sample rate of the instrument. It may be used to synchronise a second oscilloscope.

c) External Clock Input - TTL input, negative edge activated which will be rephased by the internal clock, there will be an uncertainty of ±0.25μsec after rephasing. See Fig. 3.3

d) Ready - TTL output which goes LO when clock edge (c) is received. Signal goes H1 to indicate ready for next clock signals (c) and (d) provide a two wire handshake. Note that for external clock frequencies much less than 1MHz, the response time of the instrument is such that READY need not be tested. See Fig. 3.3

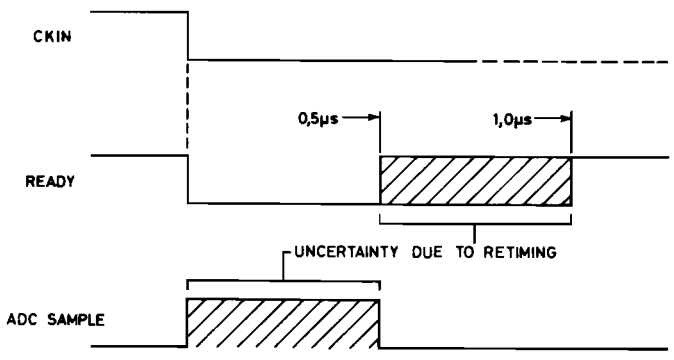


Fig. 3.3 External Clock Handshake Timing

e) External Clock Control - TTL input, LO to select external clock. Note that if no external clock is applied, this line may be used to suspend the store writing process and freeze the write counter.

3.8.3 USE OF OPTIONAL PASSIVE PROBE

A x 10 passive probe may be used to extend the voltage range and increase the input impedance of the Y amplifiers. The input resistance of a Y channel is 1MΩ shunted by approximately 28pF. The effective capacitance of the input lead must be added to this and the resultant impedance will sometimes load the signal source. Therefore it is advisable to use a 10MΩ x 10 probe. This reduces the input capacity and increases the input resistance, at the expense of the sensitivity. The probe contains a shunt RC network in series with the input and forms an attenuator with the input RC of the Y channel. To obtain a flat frequency response it is necessary to adjust the capacitance of the probe to match the input capacity of the Y channel as follows:-

1. In the Normal Mode, set the Y channel VOLTS/CM switch to 20mV/cm, and the TIME/CM switch to .2ms/cm.
2. Connect the probe to the CAL 1V pin.
3. Set the adjustable capacitor in the probe tip or termination with a small screwdriver for a level response with no overshoot or undershoot visible on the display.

3.9 FUNCTIONAL CHECKS

This section describes a test routine with checks that the instrument is functioning correctly in its main modes of operation, but it also provides examples of how to use and set the instrument.

3.9.1 NORMAL MODE

Switch on, put Display Mode switch to NORMAL. Put timebase switch to 1ms/cm; CH1 and CH2 attenuators to 0.2V/cm; Trigger Level Control knob pushed in; CH1, CH2 and X shift controls central; Y Mode switch to CH1 & CH2; Input coupling switches to GND; Trigger source switch to CH1; Trigger Coupling to A.C. Turn intensity control to clockwise end. Adjust CH1 and CH2 shift controls to obtain two traces. Adjust Intensity and Focus control to obtain finest possible traces. Rotation of the Trigger Level control through the central position will cause trigger L.E.D. to flash once. After at least 15 mins warm up, check that on both channels the vertical trace movement caused by turning the attenuator switches from 0.2V/cm to 0.5V/cm is less than 0.5cm. If not adjust the BAL. pre-set for that channel. Set input coupling switch to DC. Apply sine wave at approx. 1kHz to CH1 and select CH1 as trigger source. Adjust CH1 attenuator and/or signal amplitude to give about 5cm Y deflection. Adjust trigger level control to obtain stationary trace - check trigger L.E.D. is illuminated. Pull out Trigger level control to disable Bright Line

facility and turn until trigger is lost; trace should disappear. Trace should re-appear free running when Level control is pushed in. Reset Trigger Level control for a stationary trace.

3.9.2 REFRESHED MODE

With the oscilloscope in NORMAL mode, obtain a stable display of a 1kHz approx. signal. Switch to Refresh mode. Check that the trace responds to the Y shift control. Pull the trigger level knob to disable the bright-line and change the trigger level until the oscilloscope no longer triggers. The oscilloscope will retain a display of the last signal on which it triggered. Check this by proving that the displayed trace does not respond to the Y shift control. Change the frequency of the input signal to 10Hz approx., TIME/CM to 50msec/cm and adjust trigger level to suit. Note that if the bright-line is not disabled, it may cause mistriggering. Switching between NORMAL and REFRESHED will show the advantage of the flicker-free display obtained in REFRESHED mode.

3.9.3 SINGLE SWEEP

Switch the input coupling switch to the GND position and press the ARM button. The ARMED indicator should now be lit. Restore the input coupling switch to DC and note that the instrument performs a single input sweep and stops with the STORED indicator lit. The sequence may be repeated by pressing the STORE button again. There is no need to press RELEASE first.

3.9.4 DISPLAY HOLD

Press DISPLAY HOLD and note that the display freezes immediately regardless of the BRIGHT LINE. Note also that when Display Hold is released, store writing will continue at the point on the screen where it was frozen.

3.9.5 LOCK ALT. SAMPLES

With the oscilloscope in single channel mode, press the HOLD ALTernate SAMPLES button. Operating the appropriate shift control will result in two traces being displayed, one "frozen" and one "live". This may be used for before/after comparisons. Note that in dual channel mode, channel 2 is affected by HOLD ALT SAMPLES and channel 1 remains "live".

3.9.6 ROLL MODE

Switch display mode to Roll. Select a low sweep speed such as 1 sec/cm. Select CH1 only. Offset trigger level to one end, and check Hold and store L.E.D.'s are off. Movements of the CH1 shift control will now be seen to draw a trace on the screen similar to a strip chart recorder, with the "pen" at the right hand side of the screen, and the trace moving towards the left at the sweep speed selected. This movement can be arrested at any time by pressing the DISPLAY HOLD button.

3.9.7 PRE-TRIGGER STORAGE

Apply a low frequency signal of approximately 1Hz and with trigger coupling in the D.C. position adjust the trigger level control until the trigger source L.E.D. flashes continuously. The display will continue to move to the left. Remove the signal and press the Store button. On re-applying the signal sequence trigger-stored will be followed resulting in a stationary display. The length of time spent in the trigger condition and therefore the final waveform position is dependent upon the setting of the stored trigger point switch, and can be changed from zero to three quarters of the full sweep time. At normal to low settings of the brilliance control a bright dot can be observed marking the point of trigger (it is displaced to the left of the true trigger point by two samples. i.e. worst case is approximately 0.2cm on quadrant and x10 expansion. After a stationary display has been obtained, if the signal is not removed, but its frequency is changed by say 2:1, on pressing the store button again, the sequence, trigger-stored will be followed, resulting in a stationary display again. It will be found that the new display contains none of the "old" frequency, because the store will automatically take in just enough new information before becoming sensitive to trigger such that the next stored waveform consists of new information entirely.

3.9.8 QUADRANT EXPANSION

Obtain a display of a signal of slightly less than 1kHz as shown in Fig. 3.4 (a) with the TIME/CM set to 0.2msec/cm as indicated. Switching to quadrant expansion will change the display to 50μsec/cm as indicated by the green cursor on the TIME/CM Switch skirt. Note that in the example shown in Fig. Y, the first positive edge (1) is viewable on the second and third quadrants due to the overlap between quadrants. Similarly the second positive edge is viewable on quadrants 6 and 7.

Quadrant expansion, as well as allowing more detailed examination of waveforms, also allows increased accuracy of time measurements. In the example of Fig. 3.4 the position of edge (1) is measured on quadrant 2, then without touching the shift control, the display select switch is moved to quadrant 6 and the position of edge 2 measured.

The table of Fig. 3.1 states that all points on quadrant 2 are offset from quadrant 1 by 5.12cm. The position of edge 1 is thus 10.42cm (5.12 + 5.30) relative. Similarly the position of edge 2 is 25.60 + 6.10 = 31.70cm relative. The period of the waveform is thus 21.28cm at 50μsec/cm i.e. 1.06(4)msec. This measurement may be confirmed from Fig. 3.4 (a).

This calculation could more easily have been performed as below:

$$\underset{\text{Difference of offset}}{\frac{(25.60 - 5.12)}{20.48}} + \underset{\text{Difference of position}}{\frac{(6.1 - 5.3)}{0.80}} = 21.28\text{cm}$$

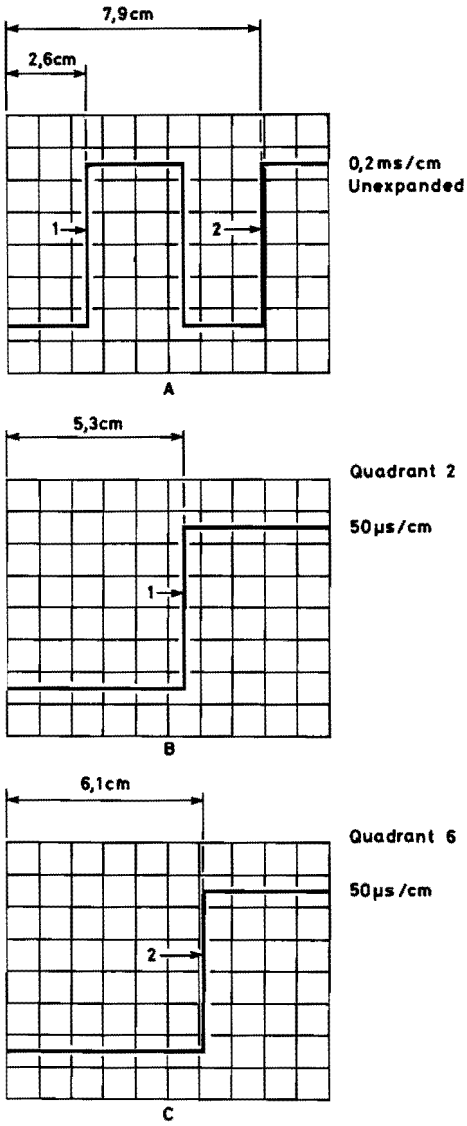


Fig. 3.4 Measurements by Quadrant Expansion

Where the accuracy of the difference of offset is that of the clock frequency i.e. ±1%. The difference of position is dependant upon the display and thus has a tolerance of ±3%. By making the difference of offset much greater than the difference of position (i.e. spread over a large number of quadrants) the accuracy of measurement approaches ±1%. In this example it is ±1.1%.

3.10 THE 4022 OUTPUT OPTION

3.10.1 ANALOGUE OUTPUTS

The 4022 output unit provides the user of the OS4020 with a means of obtaining fast, permanent records of displayed traces. It may be used with a wide variety of pen recorders of either XY or strip chart type. Both channels are available simultaneously for recorders with two pens. Alternatively the two channels may be reproduced sequentially on single pen recorders. A synchronised X ramp is available for use with XY recorders. Alternatively the CH1 and CH2 outputs can drive an XY display directly. The internal contacts can be used to control a chart motor and/or pen lift if required.

3.10.2 CHART RECORDER SPEED

The 4022 offers a wide range of read-out rates to suit the recorder being used. The rate should be chosen by considering the following:

1. A slow read-out rate, while faithfully reproducing the stored signal, will also show the discrete levels in the output waveform. A faster read-out rate and pen recorder speed will tend to smooth the output waveform.
2. If too fast a read-out rate is chosen, the pen recorder may be unable to follow any large amplitude fast change of signal. This is the slew rate limitation of the recorder.

The optimum read-out speed for any particular stored waveform is thus the maximum at which the pen recorder is capable of tracking the signal. The bandwidth of the 4103 output amplifiers is d.c. to 16kHz (−3dB) which is well above the limitations of most pen recorders.

3.10.3 USING WITH A PEN RECORDER

1. Connect the CH1, CH2 and X-ramp BNC sockets on the side as required.

   On single trace operation, the same signal will be present at CH1 and CH2 outputs. Set the sensitivity of the pen recorder inputs to accommodate ±400mV full scale on CH1 and CH2 and 0 to 1V for the X-ramp, i.e. each cm of c.r.t. deflection in Y corresponds to 100mV of output level.

   When 4022 is not reading-out, the analogue outputs return to 0V. This corresponds to mid screen on the c.r.t. display for the CH1 and CH2 outputs, and thus the recorder pen(s) should be set to mid scale unless specifically required otherwise. The ramp output moves positive from 0V, however, and the pen should be positioned to allow at least 1V positive travel for this signal.

2. Connect, if required, for remote start/pen lift.

   NOTE: The relay contacts are unprotected and inductive loads should be suppressed to stay within the contact rating. Although the contacts are isolated electrically from the oscilloscope circuitry, very rapid currect or voltage changes in the contact path could interfere with the operation of the oscilloscope.

3. The delay time from the closure of the relay contacts to the start of read-out is set by a pre-set control (START UP DELAY) on the side panel.
4. Obtain the required trace(s) on the OS4020 and store it using the SINGLE SHOT or HOLD functions. If the SPLIT TRACE facility is being used, the trace stored

with this control will appear at the CH2 output, the other trace appearing at the CH1 output.

5. Set the required read-out rate on the PLOT SPEED switch on the sub-panel. The calibrated times are per cm of unexpanded c.r.t. delection and should be muiltiplied by ten to obtain the total read-out time.
6. Set the PLOT MODE switch on the sub-panel to the MANUAL START position.
7. Set the PLOT button on the front panel of the OS4020 to initiate the read-out cycle. Note that the OS4020 is prevented from accepting new data into the store during a plot cycle and the display will be frozen. the PLOT indicator will light to indicate that a read-out cycle is in progress.

3.11 PLOT MODES

The PLOT MODE switch on the side panel selects one of three operating modes:-

3.11.1 MANUAL START

In this mode a single plot cycle may be initiated either by pressing the front panel START button or by applying a TTL low level, or contact closure to ground, to the REMOTE START input. The front panel indicator lamp will light immediately the start command is given and remain on for the duration of the read-out cycle.

3.11.2 AUTO–START

This facility is used in conjunction with the SINGLE SHOT store sequence on the OS4020. Whenever the STORED indicator lamp is lit to indicate the completion of a single shot store sequence, a single plot cycle will be initiated. At the end of this plot cycle the timebase of the OS4020 will be armed automatically, ready to execute a further single shot store sequence upon receipt of a trigger signal. In this manner the instrument may be left unattended to monitor and record intermittend transient signals.

Note that to initiate the auto procedure it is first necessary to press the ARM button to start the single shot store sequence.

Alternatively, a plot cycle may still be started in response to the START button or a REMOTE START input command as for the MANUAL START mode. At the end of a plot cycle started in this way, the timebase will be re-armed.

3.11.3 CONTINUOUS

With the PLOT MODE switch in this position, a plot cycle may be initiated in the same manner as the MANUAL START mode. However, instead of just a single sweep being generated, the unit will now read-out continuously until the START button is pressed again (or a REMOTE START command given). The indicator lamp associated with the START button on the front panel will be lit while the output unit is reading out.

3.11.4 PLOT TERMINATION

The plot may be terminated immediately and independent of the mode of operation by selecting DISPLAY HOLD and pressing the RELEASE button on the front panel single sweep section.

3.12 PLOT MARKER OUTPUT

If the CONTACTS output is used to start up a chart recorder motor, the START UP DELAY control would normally be set to allow the recorder to accelerate to full speed before information appeared at the CH1 and CH2 output socket. If it is required to mark the exact start of the recorder information, with an event marker pen say, the PLOT MARKER output should be used. This provides a TTL logic level signal which goes 'high' at the start of the recorded information and 'low' immediately at the end of it. The loading on this output should not exceed that permitted for a standard low power Schottky gate.

3.13 FUNCTION GENERATION

Although primarily intended to be used to drive pen recorders, the analogue outputs can be used for other application.

In the continuous mode the 4022 acts as a function generator, continuously repeating the one or two waveforms stored. Thus a single transient can be recorded at one speed and re-generated continuously at another faster or slower speed within the available stepped range of PLOT SPEED, with the following limitations:-

a) The CH1 and CH2 outputs have a bandwidth limited to 16kHz. This produces a limit which is a function of the signal stored as well as the replay rate.

b) the X output, limited to the same bandwidth takes approximately 90μsec to reset to OV (to 12 bit accuracy) at the end of sweep. Thus in continuous mode, the X output will depart from a true reproduction at plot speeds faster than 50msec/cm

* see also external plot clock section 3.10.9

3.14 ADDITIONAL FACILITIES

The signals below are accessed via the MISC I/O socket.

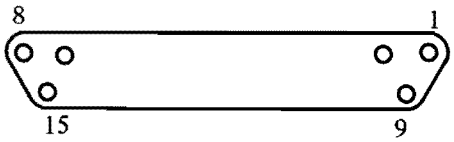
REMOTE START, pin 8: This input may be activated by driving to a TTL LO or by contact closure to Ov (available on the same socket). Its action is identical to the PLOT button on the front panel.

EXTERNAL PLOT CLOCK, pin 11: The internal timebase clock on the 4022 may be replaced by an external TTL clock by driving EXTERNAL CLOCK ENABLE pin 4, LO. As in the main instrument, the external clock is rephased by the internal 2MHz clock. When the PLOT is active, a positive edge on the external clock first increments the plot address counter and then causes data from that address to be latched and converted.

3.15 WRITE RATE RAMP

The function of the plotter may be changed to produce an X-ramp in synchronism with the write counter in the oscilloscope when the latter is in digital mode. This represents the timebase ramp found in normal mode. It is obtained by making connection to the MISC I/O socket as follows:-

(a) Connect pin 4 to Ov on pin 15. This enables external plot clock.



View on Connector

1	External Clock In	(4020)
2	READY	(4020)
3	GATE	(4020)
4	External Clock Enable	(4022)
5	N/C	
6	N/C	
7	Internally Connected	
8	Remote Start	(4022)
9	Clock Out	(4020)
10	External Clock Enable	(4020)
11	External Plot Clock	(4022)
12	Readout Marker	(4022)
13	N/C	
14	Write Rate Ramp Enable	(4022)
15	0V	

Fig. 3.5 Misc. I/O Connections

(b) Connect pin 11 to pin 9. This clocks the plotter at the write rate of the oscilloscope

(c) Connect pin 14 to pin 15. This enables the ramp.

The start and rate of the X-ramp will then be controlled by the main instrument. Please note the following limitations:-

(a) The maximum rate of the ramp is a previously described.

(b) The two Y channel outputs are not active.

(c) Grounding pin 14 disables the normal plotter functions.

(d) The ramp is synchronised to a triggered sweep and is not relevant in ROLL mode.

The write rate ramp may be used as the X-drive on a voltage controllable signal source to provide a sweep function i.e. signal frequency (or amplitude) proportional to X deflection.

3.16 DIGITAL INTERFACE

Digital interface to the oscilloscope is obtained via the digital I/O D-type connector on the plotter sub-panel. This interface, primarily intended for connection to a micro/mini-computer system, enables the reading and/or remote control of the following oscilloscope functions:

Timebase range – Refresh and Roll only

Mode – Normal/Refresh/Roll

Channel selection

Roll trigger point

Two dedicated outputs carry information as to whether the oscilloscope:

1. Has stored a trace.
2. Is plotting.

It is also possible to:

Arm the oscilloscope

Start a plot

Terminate a plot

The 4022 provides a remote/local facility on the programme oscilloscope functions. When in the local mode, the instrument will respond to front panel controls and store, but not respond to, remote control information. In the remote mode, these controls with a remote counterpart will respond to the remote setting and the front panel control is disabled.

Data access to the store is provided on a channel oriented sequential basis.

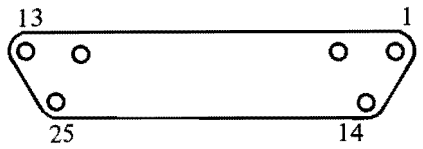
The address is provided internally with an auto-increment facility. When the handshake input is taken LO data will be written into the address indicated by the internal counter, then the latter is double incremented, i.e.moves to the next address in that channel.

The I/O functions are implemented in Low Power Skottky T.T.L. cable length, loading and frequency of operation must be chosen to suit.

3.16.1 INTERFACE SIGNAL LINES (see also section 4.11)

Data Lines: BØ – B7. These bi-directional data lines allow transfer of data between the external controlling device and the 4022. The direction of transfer is controlled by the read and write lines. When neither read or write is selected, BØ-B7 remain in a high impedance state.

$\overline{\text{Read}}$, $\overline{\text{Write}}$: Inputs active low level internal pull up. When $\overline{\text{Read}}$ is taken LO, data will be transferred from the 4022 to the external device. When $\overline{\text{Write}}$ is taken LO, data will be transferred from the external device



View on Connector

1	BØ
2	B2
3	B4
4	B6
5	0V
6	Internally Connected
7	N/C
8	$\overline{\text{WRITE}}$
9	MUX2
10	$\overline{\text{RDO}}$
11	$\overline{\text{STO}}$
12	Internally Connected
13	HSM
14	B1
15	B3
16	B5
17	B7
18	0V
19	N/C
20	N/C
21	MUX1
22	$\overline{\text{READ}}$
23	$\overline{\text{XREM}}$
24	Internally Connected
25	Ready

Fig. 3.6 Digital I/O Connections

NB. Connections to Pins 12 and 25 of Fig. 3.6 Digital I/O Connections are reversed from S/No. 300 onwards.

to the 4022 upon receipt of the handshake input. The condition of both LO may cause bus contention and should be avoided.

Handshake master (HSM): Input negative edge active. Timing signal to strobe data into the port. Increments address when accessing data store, read or write, (Increments after writing).

Ready: Output, high level indicates "ready". Indicates completion of response to handshake.

Mux 1, Mux 2: Inputs, level sensitive, internal pull-ups. These two signals are used to select the area within the OS4020/4022 being accessed by the data lines. These signals must be stable before HSM is asserted and must remain stable until READY becomes true. When MUX 1 is set LO, the oscilloscope will give store access to the 4022, execute the DISPLAY HOLD function, and light the PLOT L.E.D. Note that MUX 1 = 0 disables the analogue plot function.

$\overline{\text{XREM}}$: Input, active LO, internal pull up. When set LO, all programmable parameters in the oscilloscope will switch from their front panel settings to their programmed settings. The UNCAL L.E.D. on the front panel will flash when $\overline{\text{XREM}}$ = LO.

$\overline{\text{STO}}$: Output active LO. Indicates when the oscilloscope has entered the STORED mode at the end of a single sweep sequence.

$\overline{\text{RDO}}$: Output active LO. Indicates when the 4022 is engaged in an output plot.

3.16.2 INTERNAL CONTROL

There are three locations, accessible via the 8 bit data bus: Group 1 & Group 2, containing miscellaneous oscilloscope control functions, and the oscilloscope data store. Selection of these locations is controlled by MUX1 and MUX2 as shown in Fig. 3.7.

Group 1 and Group 2, are organised bit-wise as shown in Fig. 3.8. Each bit read indicates the actual state of the function indicated.

MUX 1	MUX 2	LOCATION
0	0	DATA STORE even location *
0	1	DATA STORE odd location *
1	0	GROUP 1
1	1	GROUP 2

* See Fig. 3.10 for significance of odd and even locations.

Fig. 3.7 Internal Addressing

L5, L6, L9, L10. L11 are the timebase control signals and are programmed in accordance with Fig. 3.11. **PT0** and **PT1** specify the pre-trigger requirement and are as shown in Fig. 3.12. The **$\overline{\text{DWC}}$** bit, when set LO produces the DISPLAY HOLD function, but lights the PLOT L.E.D.

Setting the **CH1** or **CH2** bit selects the channel indicated, setting both produces dual channel operation.

$\overline{\text{XNORM}}$ and **$\overline{\text{XROLL}}$** indicate the display mode as shown in Fig. 3.9.

Note that if a timebase range of 1 sec/cm or slower is selected, NORMAL mode is not available. If NORMAL mode is selected, the instrument will actually enter REFRESH mode without affecting the reading of $\overline{\text{XROLL}}$ and $\overline{\text{XNORM}}$.

A LO written into the **$\overline{\text{SPL}}$** will start a plot. Similarly **$\overline{\text{CPR}}$** will abort the plot and reset the address counter.

The unlatched functions produce their specified effect every time a LO is written and do not require HI's to be written. For example, if the control and data lines

GROUP 1 READ	7	6	5	4	3	2	1	0
WRITE	$\overline{\text{DWC}}$*‡	PTO*	PT1*	L7*	L10*	L5*	L11*	L6*

GROUP 2 READ	7	6	5	4	3	2	1	∅
	1	1	1	1	CH1*	CH2*	$\overline{\text{XNORM}}$*	$\overline{\text{XROLL}}$*
WRITE	X	$\overline{\text{CPR}}$†	$\overline{\text{SPL}}$†	$\overline{\text{ARM}}$†				

* Under control of remote/local † Not latched ‡ No local equivalent read 1 in local mode rather than the programmed value. These may differ of the instrument is responding to front panel controls.

Fig. 3.8 Bit map of Group 1, 2 locations

$\overline{\text{XNORM}}$	$\overline{\text{XROLL}}$	DISPLAY MODE
∅	∅	N/A
∅	1	NORMAL
1	∅	ROLL
1	1	REFRESH

Fig. 3.9 Display Mode Control

are set up to write a LO into the $\overline{\text{ARM}}$ bit. every time the HSM line is driven LO, the oscilloscope will be ARMed.

The stored functions in Group 1 and Group 2 do not power up in any pre-determined state and should therefore be loaded before $\overline{\text{XREM}}$ is driven LO.

Vertical Mode	Store Contents	
	Odd	Even
Single Channel	Used Sequentially	
Single Channel Hold Alt.	Held Live	Dual Trace
Dual Trace	CH2	CH1

Fig. 3.10 Channel Organisation

3.16.3 INITIALISATION

The sequence below indicates one possible method of initialisation, starting with $\overline{\text{XREM}}$ = 1:-

1. Drive MUX 1 = 1, MUX 2 = 0, $\overline{\text{READ}}$ = 0. Fig. 3.11(b) shows that valid data, in this case, the local settings of GROUP 1 will appear within 150 nsec. Read and store data.
2. Drive $\overline{\text{READ}}$ = 1, $\overline{\text{WRITE}}$ = 0 place data obtained in (1) on bus.
3. Drive HSM = 0 when data is stable.
4. Drive HSM = 1. This will have copied the local settings into the remote store.
5. Repeat (1) – (4) with MUX 2 = 1 to initialise Group 2.
6. Driving $\overline{\text{XREM}}$= 0 at this point would cause the duplicate parameters to be used.

3.16.4 READING STORE DATA: MINIMUM HARDWARE SOLUTION

Although the store data is channel organised, use may be made of the fact that the handshake is not required to read data, only to increment the address counter. MUX2 may be manipulated to ensure that both odd and even store locations are read on a single pass. For the minimum system, MUX2 may be connected to HSM and the pair driven by a TTL signal. The starting conditions are $\overline{\text{READ}}$ = 0, MUX1 = 0, MUX2 = HSM = 0 with the counter cleared (see later). The contents of store location zero are available at the output. When MUX2/HSM goes HI location one contents appears (see Fig. 3.11 for timing). When MUX2/HSM goes LO, the internal address counter (double) increments and the contents of location 2 becomes available. The entire contents of the store may be read in this fashion. If MUX1 is driven HI, control of the address counter is given back to the plot circuitry. If no plot is in progress, (as will be the case) the address counter is cleared. This offers a simple alternative to $\overline{\text{CPR}}$ for clearing the counter.

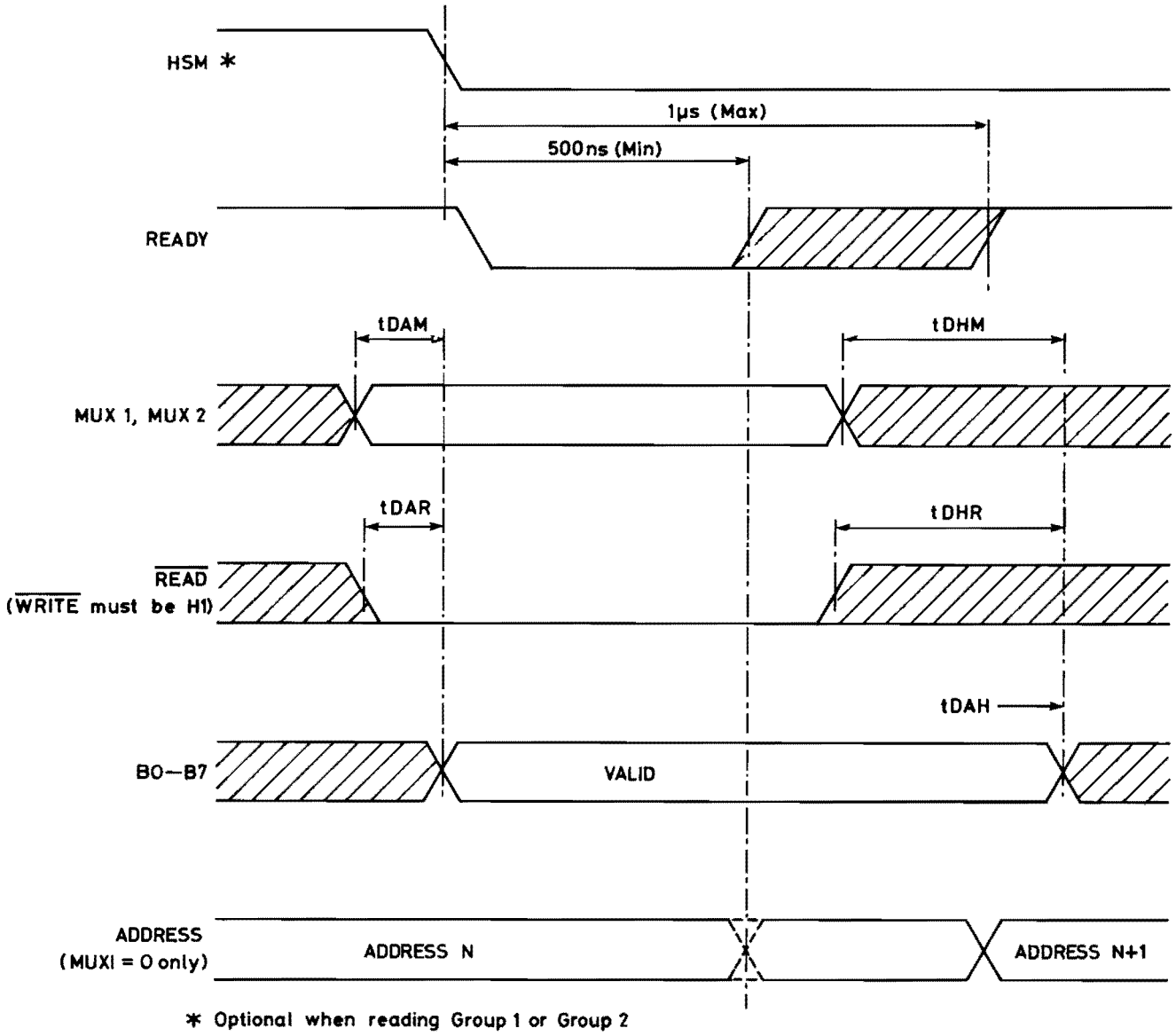
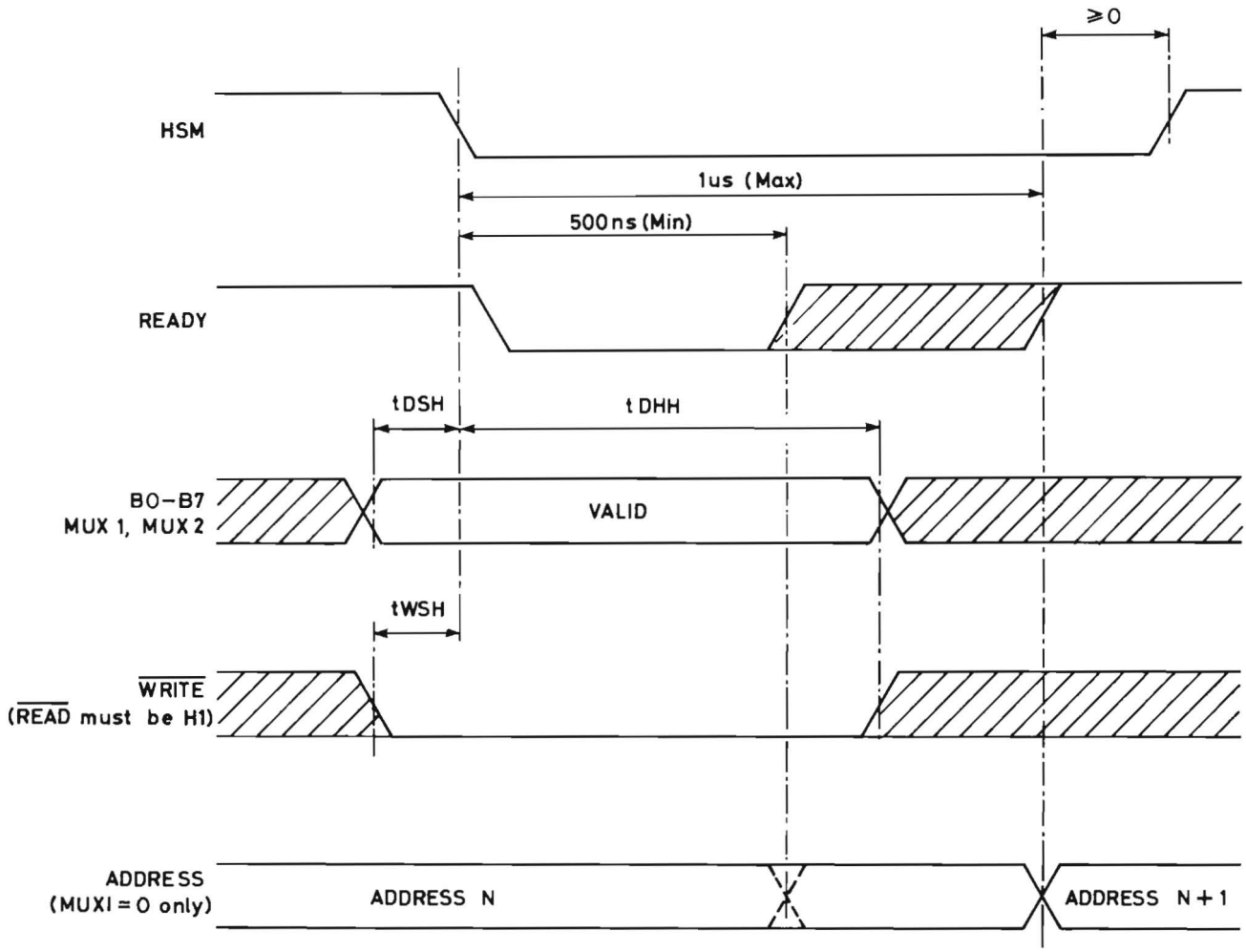


Fig. 3.11 4022 Read Timing



	Group 1/2	Store Data
tDSH Set up time: Data Valid to Handshake	⩾ 0ns	⩾ 0ns
tWSH Set up time: Write to Handshake	⩾ 0ns	⩾ 0ns
tDHH Data Hold time from Handshake	600ns(mm)	600ns

Fig. 3.12 4022 Write Timing

	Time/cm (unexpanded	Division Ratio		Timebase Control Line Signals L6	L11	L5	L7	L10	L8	L9
Over-range	1μsec/cm to 0.1msec/cm	1	ALTERNATE / NORMAL MODE ONLY	0	0	0	0	0	0	1
DIGITAL MODE Range available on Time/cm switch	0.2msec/cm	1		0	0	0	0	0	0	0
	0.5 "	2½		0	0	0	1	0	0	0
	1 "	5		0	0	0	0	1	0	0
	2 "	10		0	0	1	0	0	0	0
	5 "	25		0	0	1	1	0	0	0
	10 "	50		0	0	1	0	1	0	0
	20 "	100	CHOP	0	1	0	0	0	0	0
	50msec/cm	250		0	1	0	1	0	0	0
	0.1sec/cm	500		0	1	0	0	1	0	0
	0.2 "	1,000		0	1	1	0	0	0	0
	0.5 "	2,500		0	1	1	1	0	0	0
	1 "	5,000		0	1	1	0	1	1	0
	2 "	10,000		1	0	0	0	0	1	0
	5 "	25,000		1	0	0	1	0	1	0
	10 "	50,000		1	0	0	0	1	1	0
	20 "	100,000		1	0	1	0	0	0	0
Extended range available by remote programming	50sec/cm	250,000	REFRESHED/ ROLL ONLY	1	0	1	1	0	1	1
	100sec/cm	500,000		1	0	1	0	1	1	1
	External clock	--		1	1	1	X	X	1	1

Fig. 3.13 Timebase Control Signals

Trigger Point Selection	PTØ	PT1
¼	1	0
½	0	1
¾	1	1
END TRACE	0	0

Fig. 3.14 Pre-trigger Control Signals

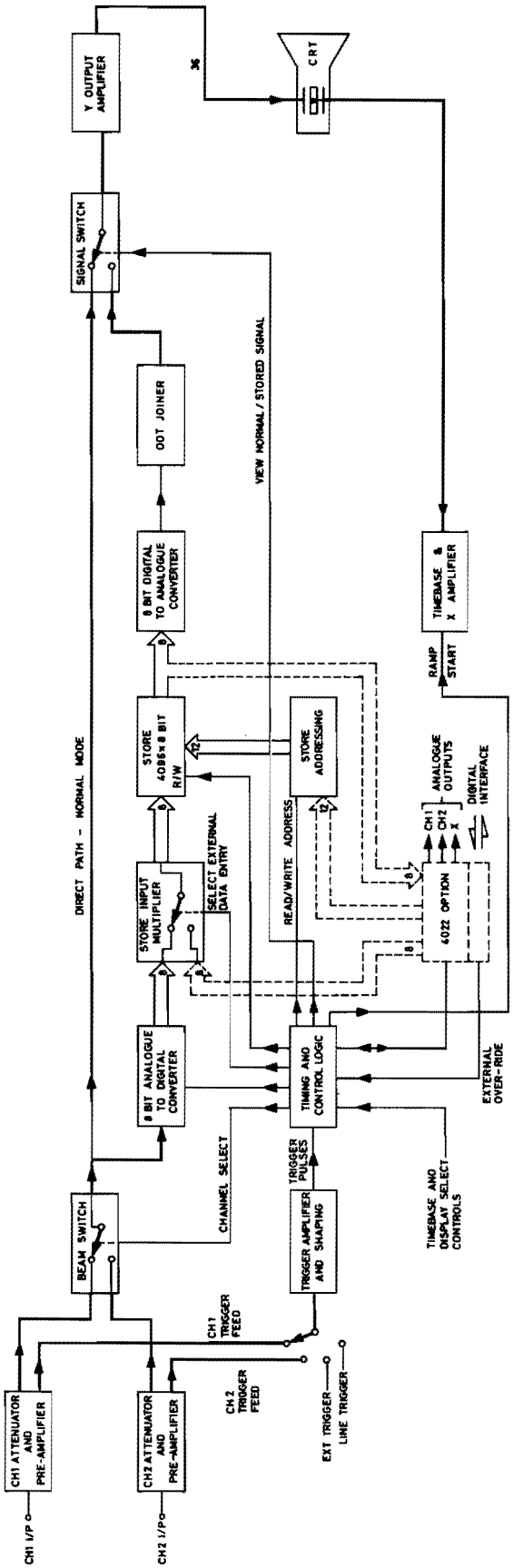


Fig. 4.1
Block Diagram of Instrument

Circuit Description

Section 4

4.1 SYSTEM DESCRIPTION

With the MODE switch in the NORMAL position the instrument operates as a conventional oscilloscope. Referring to Fig. 4.1, input signals are applied to two identical pre-amplifiers which incorporate the sensitivity controls, both variable and switched, and also the Y shift and input coupling controls. The outputs of these pre-amplifiers are applied to the beamswitch and also to the trigger selector switch. The beamswitch selects one or other of the two channesl and in dual trace, is operated either in a chopped or alternate sweep mode, dependent on the setting of the timebase range switch. The output of the beamswitch is applied via the signal switch to the Y output amplifier which drives the vertical deflection plates of the c.r.t. A trigger signal is selected by the trigger selector switch and shaped into fast pulses by the trigger amplifier which contains the trigger level, slope and coupling controls. These trigger pulses are supplied via the control logic to the timebase and initiate a linear ramp, the duration of which is determined by the resistors and capacitors switched by the timebase range switch in the usual manner. The ramp is applied via the X amplifier to the horizontal deflection plates of the c.r.t. A bright line facility is available such that when no trigger signal is being received, the timebase is made free to run, producing a visible base line.

When the MODE switch is in the REFRESHED position, the signal switch is changed over so that the output from the Dot Joiner is routed to the Y output amplifier. Analogue signals from the beamswitch are applied to the Analogue to Digital Converter (ADC) which produces an 8 bit binary code (word) representing the instantaneous signal level at 500 nanosecond intervals. The data produced by the ADC can be loaded into a store under the control of the timing logic. The store can hold 4096 such 8 bit words and the data is entered at a rate such that the information contained in the whole store represents one complete sweep. This data is then continuously read out (non-destructively) at a fixed rate and reconstituted as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output amplifier to give a continuous display of the store contents. Since the output from the DAC is in the form of discrete levels, a dot joiner is included to join these levels and provide a continuous display.

In both REFRESH and ROLL modes, the timebase sweep is controlled by a separate timing chain to provide total sweep periods of 4msec, 1msec, and 0.8msec. The 4msec ramp is used to display the entire 4k store, the other two ramps providing x 4 and x 5 expansion respectively for quadrant display (see below). The display sweep is synchronised to the store read out cycle and is independent of the setting of the timebase switch.

Note that the trigger amplifier is now entirely dissociated from the timebase since the latter is running continuously. The function of the trigger amplifier is to initiate a write cycle, when a screen full of new information will be entered into the store.

The rate at which data is entered into the store is defined by a programmable digital divider, which divides down the main 2MHz clock under the control of the timebase range switch to provide 400 samples per cm unexpanded.

Dual trace operation is catered for by operating the beamswitch in the chop mode at half the data entry rate, storing samples of CH1 in even numbered store locations and those of CH2 in odd numbered. The store is read out at a rate fast enough to avoid flicker and so an alternate sweep technique is used with even numbered locations read out on one sweep and odd numbered on the next.

The HALF HOLD facility inhibits the writing of data into odd numbered store locations. In dual trace mode, this will have the effect of holding CH2 information. In single trace mode a copy of the current signal will be held.

The STORE control provides a conventional single shot facility to enter one triggered sweep of data into the store, while the LOCK STORE controls inhibit immediately the entry of any new data.

The ROLL mode of operation is similar to the REFRESHED mode except in the way in which new data is entered into the store. Instead of waiting for a trigger pulse to initiate a new data input cycle, data is continuously entered into the store. Thus, if data entry is stopped on receipt of a trigger pulse, the content of the store will be information stored before the trigger pulse, rather than after it as in a conventional trigger sequence. To expand this facility, which operates only in conjunction with the single shot store controls, a switched delay is incorporated marked STORED TRIGGER POINT which allows the input of new data to continue after a trigger is received, for a time corresponding to ¼, ½ or ¾ of the store length. This allows the amount of pre-trigger and post trigger information retained in the store to be varied to suit the application. Calibrated expansion of the stored waveform, activated by the quadrant expansion switch, is obtained by increasing the display sweep speed as described above. The various segments are obtained by presetting the store read address counter for the start of the display sweep. At least 1024 bytes are displayed.

CIRCUIT REFERENCES

Each component in the instrument is specified by a circuit reference consisting of a letter prefix and a number. The number also indicates which printed circuit board assembly the component is mounted on as shown below:-

CIRCUIT REFERENCE No.	
0 – 99	Main Frame Component
100 – 399	Analogue to Digital Converter Assembly
400 – 499	E.H.T. Board
500 – 599	Power Supply Board
600 – 699	Timing Logic Board

700	–	799	Store Logic Board
800	–	899	Output Unit 4022 – Fitted as an option
900		1099	Timebase Board

Note that in some sectors of the circuit, transistors are referenced TR and integrated circuits IC. In others they are referenced Q and U respectively.

To assist in circuit comprehension, section 4.10 is included with a list and brief description of all control lines with a mnemonic reference and this is followed by a cross reference list between the most significant IC's and the relevant section for description of their operation and function.

The location of the various assemblies is shown in Figs. 5.1 and 5.2

4.2 POWER SUPPLIES

4.2.1 GENERAL

Referring to Fig. 5.17 all the power supplies for the instrument are derived from the transformer, T51. Two tapped primary windings are switched by S52 to allow for three supply voltage ranges and fuse FS51 provides fault protection. The supply indicator LED is supplied from the unregulated –6V supply via current limiting resistors R57 and R58.

4.2.2 LOW VOLTAGE SUPPLIES

Five separate secondary windings supply bridge rectifiers, BR51–BR55, mounted on the transformer and provide unregulated supplies of +170V, +26V, –26V, +18V, –10V and +8V accross the reservoir capacitors, C509A, C510, C511, C512, C502 and C51 respectively. Note that the –10V and +8V supplies are floating with respect to ground due to the action of the regulators. The +170V supply is further smoothed by R540 and C509B and protected by fuse, FS501. The +26V, –26V, +18V and –10V supplies are fed to high performance integrated circuit regulators, IC503, IC504, IC501 and IC502 respectively to provide stabilised lines of +20V, –20V, +12V and –6V. These devices contain all the circuitry necessary for a conventional series regulator, together with current limiting and thermal shutdown facilities to protect the device against overloads arising from short circuits etc. Note that the two 20V lines are in fact provided by 15V regulators in conjunction with zener diodes, D503 and D504.

The +8V supply feeds a discrete series regulator comprising transistors, TR505–TR510, and associated components, to provide a stabilised +5V line. The long tailed pair, TR 505 and TR506, compares the output voltage with the voltage across the zener diode, D505, and provides an error signal which is passed via the emitter follower, TR509, to the series pass transistor, TR510. A second long tailed pair, TR507 and TR508, senses the voltage drop across the current sensing resistor, R522, and if the supply current rises above 3 amps will shut down the regulator by reducing the reference voltage at the base of TR505. The resistor network, R518, R517 and R520, determines the limiting current and also provides a 'foldback' limiting characteristics by reducing the permissible output current of the regulator as the output voltage fails. This prevents excess dissipation in the series pass transistor under short circuit conditions. The zener diode, D506, prevents the output voltage of the regulator rising excessively high under fault conditions and thus protects from damage the integrated circuits supplied from this line.

4.2.3 E.H.T. SUPPLIES

The two remaining secondary windings are associated with the cathode ray tube (c.r.t.) supplies. The 6.3V winding feeds the c.r.t. heater and the 850 volt winding provides the –1kV and the +3kV supplies. Stabilisation of both lines against supply voltage variations is achieved as follows. One end of the 850V winding feeds the rectifier diodes in the normal manner, the other end passes to ground via a bridge rectifier, BR401. The alternating current in the winding passes through R406 and TR402 as direct current developing a steady voltage across C402. This voltage, controlled by the conduction of TR402, is effectively subtracted from the peak voltage available at the 'hot' end of the winding and thus by varying the base-emitter voltage of TR402, the rectified high voltage supplies can be controlled. The average value of the base-emitter voltage of TR402 is established by the voltage at TR403 emitter. This in turn is controlled by the voltage at TR403 base set by the feedback resistor, R411, from the –1kV supply line and the combination of R409 and R410, thus establishing a closed feedback loop. A small current also flows from the base of TR403 via R407 to the unregulated –26V supply. Since this voltage changes with the line voltage this trims out any remaining fluctuations in the E.H.T. supplies due to supply cariations. The –1kV supply is derived by the diodes, D404, D405 and D406, feeding the reservoir capacitors, C404, C407 and C406. The voltage is smoothed by R413, R414 and C405, C408 and C409 and applied to the grid of the c.r.t. The cathode potential of the tube is held positive w.r.t. the grid as determined by the brilliance control, R419, and the second anode potential is set by R416 to optimise the focus. Small positive voltages set by R417 & R408 are applied to the third anode and interplate shield to minimise raster distortion.

4.2.4 GRATICULE ILLUMINATION

The graticule is illuminated by two lamps, ILP1 and ILP2. The supply for these lamps is derived from the emitter follower, TR401, and controlled by the potentiometer, R402, This circuit is supplied from the 8 volt winding of the transformer via diodes, D53 and D54.

4.2.5 THE TRACE ROTATION COIL

A coil, L51, fitted round the neck of the c.r.t. inside the magnetic shield, is used to align the trace with the horizontal graticule lines. The current for this coil is taken from the pre-set potentiometer, R529, through R530 on the power supply board. The direction of rotation can be reversed by interchanging the coil connections at the power supply board.

4.3 THE Y AMPLIFIER

4.3.1 THE Y PRE-AMPLIFIER

The attenuator and pre-amplifier in Channel 1 are identical to those in Channel 2. Accordingly only Channel 1 will be described. Referring to Fig. 21 the input signal is applied to the front panel socket, SKV, and then to the 3 position lever switch, S1, via R22. This switch selects AC or DC input coupling by including or by-passing C20 in the signal path. On the middle position of the switch, the input socket is disconnected and the input to the amplifier is connected to ground. Input sensitivity selection is performed in two stages; the six lowest ranges, 5–200V/cm, are obtained by switching the gain of the amplifier as described later. The 0.5 – 20V/cm ranges are provided by switching in a ÷ 100 attenuator section before the amplifier and repeating the gain switching. This attenuator is formed by R24 and R351 with C305 to set the h.f. response. C303 is adjusted to maintain the total input capacitance of the highest ranges equal to the lower ranges. Diodes, D301 and D302, limit the peak signal voltage at the amplifier input to approximately 8 volts and in conjuction with R26, protect the instrument against damage from inputs of up to 400 volts peak.

The input stage consists of the field effect transistor, TR301, connected as a source follower driving the emitter follower, TR305, via R303. The operating current of TR301 is defined by TR302 which is an identical transistor mounted in a common package with TR301 to ensure close matching and good thermal tracking. TR302 is self biased such that the operating current will develop a voltage across R308 equal to the gate-source potential. Since this same current flows in TR301 and R303 is identical to R308, the voltage at the base of TR305 is equal to the gate voltage of TR301. The drain-source voltage of TR301 is maintained constant by 'bootstrapping' with TR304 and D303. The drain-source voltage of TR302 is also maintained constant by the cascode transistor, TR303. Diode, D304, prevents the base-emitter junction of TR305 becoming reverse biased under overdrive conditions. The voltage at the gate of TR302 can be varied by R373 to balance out small variations in matching characteristics.

The signal at the emitter of TR305 is applied via the switched network, R28/34, and the common base stage, TR306, to the shunt feedback amplifier formed by TR307, R312 and R311. This can be regarded as a 'virtual earth' amplifier with R311 as the feedback resistor and the R28/R34 network as the input resistor. Thus, the overall gain of the stage is selected by S3B to provide the six basic input sensitivities of the instrument. The common base transistor, TR306, is interposed to balance the d.c. offset voltage introduced into the signal path by TR305. Diode D305 is fitted to protect TR306 from reverse base-emitter voltages. The output from the collector of TR307 is taken via R315 to the base of TR309, which, together with TR310, forms a long-tailed pair. Transistors, TR315 and TR308, are connected in a similar fashion to TR306 and TR307 and provide a balancing d.c. voltage at the base of TR310. The mutual conductance of the long-tailed pair is determined by series conbination of R319, R320 and R3. Resistor, R3, is the variable sensitivity control and is shorted by S13 when in the 'CAL' position. The preset potentiometer, R319, sets the overall gain of the pre-amplifier and C309 provides h.f. compensation.

Movement of the displayed trace will occur when the variable sensitivity control, R3, is operated unless the voltages at the emitters of TR309 and TR310 are equal (except for the input signal) and this balance is set up using potentiometer, R369. The collector current of TR309 feeds into a load resistor on the timebase board to provide an internal trigger signal.

4.3.2 BEAM SWITCH

The collector current from TR310 is passed through a cascode transistor, TR317, to the emitter of the beam switch transistor, TR319. A d.c. current determined by the shift control potentiometer, R1, and the series resistor, R387, is injected at the emitter of TR317 to provide a shift range of ±12cms. If the base of TR319 is held high (approx. 3.3 volts) the signal current will pass through the forward biased diodes, D313, D315 and D316, to the load resistor, R389. If the base voltage of TR319 is low (approx. 0.4volts) the signal current will flow through TR319 to ground and D313 will become reverse biased isolating Channel 1 from the common load resistor, R389. An identical beam switch circuit controls the output of the Channel 2 pre-amplifier but the drive to transistor, TR320, is the complement of that to TR319.

For dual trace operation the beam switching technique employed depends upon the main operating mode switch. In the NORMAL mode the channels are switched on alternate sweeps when the timebase range switch is set to 2 msec/cm or faster. On the lower timebase ranges the beam is chopped at a 250kHz rate. In the REFRESHED and ROLL modes the channels are always chopped at a rate dependent on the setting of the timebase range switch as previously described.

4.3.3 SIGNAL SWITCH

The combined input from both channels appears across R389 at a level of approximately 37mV/cm. This signal

is taken via R201 to the Analogue to Digital Converter (section 4.4) and also via emitter follower, TR321, to the signal switch formed by diodes, D317 to D320. This determines whether the signal passed to the Y output stage is the direct signal from the pre-amplifiers (NORMAL mode) or the stored signal from the Digital to Analogue Converter (REFRESHED and ROLL modes). In the NORMAL mode, transistor TR324 is turned off and its collector is at a high level thus turning TR325 fully on. The voltage at the junction of diodes D319 and D320 will be low and both diodes will be reverse biased. The two diodes, D317 and D318, will be forward biased and conducting however, and a signal at the emitter of TR321 will be transferred to the junction of D318 and D319, and via R379 to the Y output stage. When a high level is applied via R362 to the base of TR324, this transistor is turned on, TR325 becomes cut off and the situation is reversed with D317 and D318 reverse biased and the signal from TR322 emitter transferred to the output stage. The stored signal from the Digital to Analogue Converter is applied via R355 to the base of TR322. To compensate for the d.c. level shift introduced into the signal path by the emitter followers, TR321–TR322, a bias supply is provided for the output stage by transistor, TR323, which is operating under quiescent conditions identical to transistors, TR321 and TR322. The collectors of all these three transistors are supplied via R391 and clamped by D321 to approximately –0.7V in order to reduce dissipation in the devices.

4.3.4 Y OUTPUT AMPLIFIER

The Y output amplifier is a conventional two stage differential amplifier. Input signals from the signal switch are applied via SK.U to the base of TR409 and a bias signal at the same d.c. level (approx. +0.6 volt) is fed to the base of TR408. These two transistors form a long-tailed pair with the gain determined by the resistor combination, R437 and R438, in conjunction with the collector load resistors, R441 and R442. The two resistor-capacitor combinations, R443, C424, C426 and R448, C430 provide pulse response correction. The zener diodes in the collectors, D411 and D412, set the collector-emitter voltage across each transistor so that variations in power dissipation (and hence junction temperature) or the transistor with signal amplitude, are minimised. The output signal from this stage is applied to the bases of a second long-tailed pair, TR406 and TR407, which are connected in cascode configuration with TR404 and TR405 respectively.

The c.r.t. deflection plates are driven from the collectors of TR404 and TR405 with inductors, L401 and L402, providing shunt compensation. The networks, C419, C420, R425 and C421, R427 across the gain setting resistors, R426 and R435, provide h.f. compensation to ensure good pulse response.

4.3.5 BLANKING AMPLIFIERS

There are two separate blanking amplifiers producing intensity modulation of the c.r.t. display and these operate with three separate input signals viz:

i) The Sweep Blanking Signal. This cuts off the beam except when a display sweep is in progress.
ii) Chop Blanking. This is a short duration blanking pulse applied in the NORMAL mode only when the beamswitch is being switched from one channel to the other at the fast chopping rate.
iii) Trigger Point Bright-Up. This is a short duration bright-up pulse applied once per sweep when a trace has been stored in the ROLL mode of operation.

The Sweep Blanking signal is amplified by a d.c. coupled amplifier comprising TR513 and associated components. The sweep blanking signal is derived from a TTL logic gate (IC901) in the timebase via R969.
When no sweep is in progress the sweep blanking signal is at a low level (<0.4 volt) and transistor TR513 is cut off. The collector voltage is this condition is determined by the resistor chain, R526, R527 and R528, at approximately 90 volts. This voltage is applied to the second grid electrode (blanking electrode) of the c.r.t. and the beam is cut off.

When a sweep is initiated the sweep blanking input from the timebase rises to a high logic level (approx. 4 volts) turning on transistor TR513. The base drive to this transistor is limited by D507 becoming forward biased to avoid saturating the transistor and the collector voltage falls to 4 volts, thus unblanking the c.r.t. beam. The remaining two input signals are amplified by the circuit comprising TR514, TR515 and TR516. Both the Chop Blanking (CB) and Trigger Bright-Up (TBU) are TTL signals from the logic boards. For detailed information on the timing of these signals see section.

The Trigger Bright-Up signal is inverted by the common emitter stage, TR514, and applied to the base of TR515 via R508. The Chop Blanking signals are applied directly to the base of TR515 via R507 and the speed-up capacitor, C505. The signal at the collector of TR515 is fed to the base of TR516 via the d.c. level-shifting network, D508 and C519. The pulses occurring at the collector of TR516 are a.c. coupled to the grid of the c.r.t. by C506. The resistor, R533, serves to isolate the c.r.t. grid from the relatively low output impedance of the power supply and the clamping diode, D509, prevents the grid from being driven positive w.r.t. the supply, and thus possibly positive w.r.t. the cathode.

4.4 ANALOGUE TO DIGITAL CONVERTER

4.4.1 BLOCK DIAGRAM DESCRIPTION

The function of the Analogue to Digital Converter (ADC) is to quantise the instantaneous signal magnitude into one

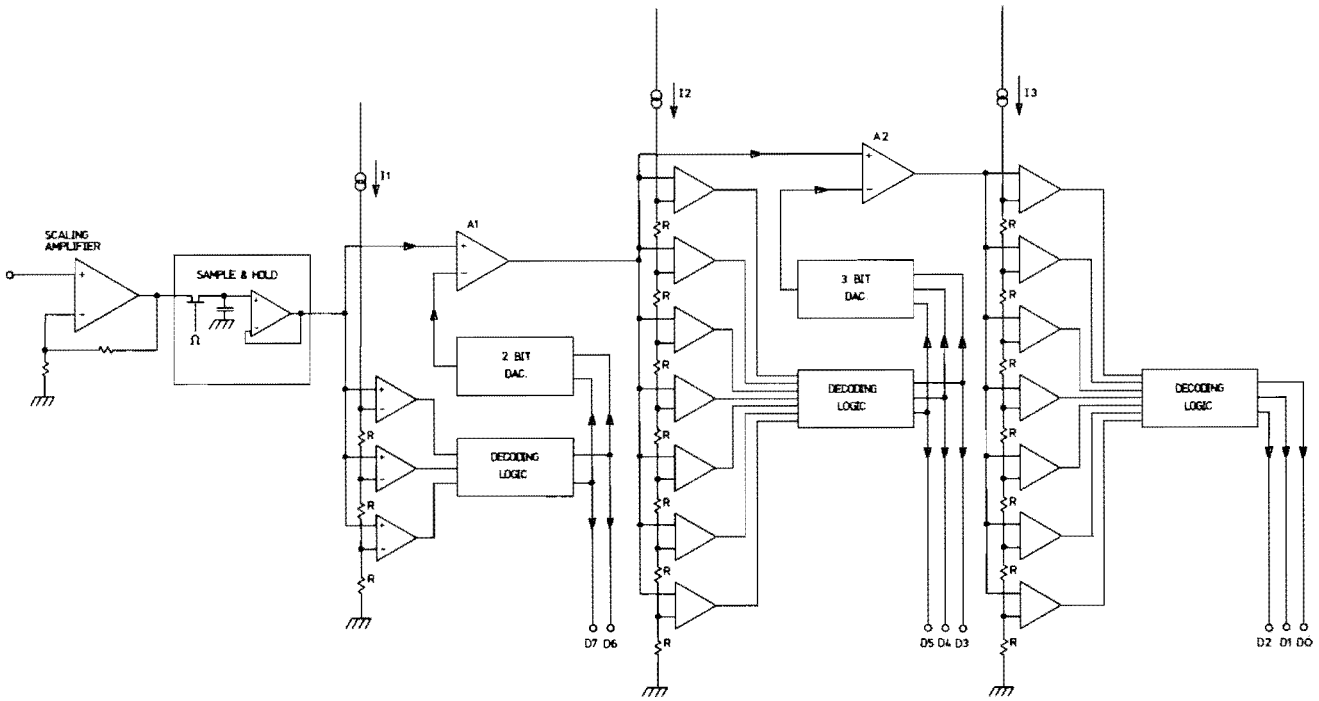


Fig. 4.2 Block Diagram of ADC

of 256 levels. These levels are represented by an 8 digit binary code (8 bit word) and the conversion is performed once ever 500 nanosec.

Referring to the block diagram Fig. 4.2. the input is applied, via a scaling amplifier, to a sample-and-hold circuit. This samples the signal level every 500ns and presents this level to the first row of comparators. These compare the signal against 3 fixed voltage levels corresponding to ¼, ½ and ¾ full scale input voltage. The output states of these three comparators are then decoded to give the first two most significant bits of the output data, D7 and D6. A 'remainder' signal is produced by subtracting from the original signal the voltage represented by the two bits already decoded. This operation is performed by a summing amplifier, A1, and a 2 bit Digital to Analogue Converter (DAC). The reference voltages for the comparators are generated by the precision resistors, R, and the current source, I1. These voltages correspond exactly to the voltages subtracted from the input signal in the summing amplifiers. Typical waveforms are shown in Fig. 4.3.

This process is then repeated using a row of 7 comparators to decode the next 3 bits of data and a further DAC and summing amplifier to drive the final row of 7 comparators.

4.4.2 SCALING AMPLIFIER

Referring to the circuit diagram Fig. 5.12 the analogue input signal from the beamswitch is applied via R201 to the base of TR201. TR201 and TR202 are a Darlington connected pair which, together with TR203 and TR204, form a conventional long-tailed pair amplifier. The output signal is taken from the collector of TR203 via the emitter-follower, TR205, and fed to the base of the sample-and-hold input transistor, TR206. The gain of the scaling amplifier (approximately x12) is determined by applying negative feedback via the potential divider network, R211, R207 and R208. Potentiometer, R217, and resistor, R209, introduce a d.c. offset into the amplifier output by drawing current through the feedback network. The diodes, D215 and D216, are normally reverse biased and clamp the output signal of the amplifier to within the working range of the ADC.

4.4.3 SAMPLE-AND-HOLD

The signal from the scaling amplifier is presented via the emitter follower, TR206, to the sampling transistor, TR208. This is a junction f.e.t. and its gate is controlled by the monostable circuit formed by the monostable circuit formed by TR209, TR207, TR210 and TR212.

The sample-and-hold cycle is initiated by a timing pulse from the ADC logic board applied to the base of emitter follower, TR226. This is amplified by the common emitter amplifier, TR227, and differentiated by C214. The negative going edge of this pulse appears at base of TR209 and turns off the transistor. The collector voltage of this transistor rises and turns on TR210 via emitter follower, TR207, and the potential divider, R222, R226. The negative-going signal at the collector of TR210 is fed back via emitter follower, TR212, D207 and C212 to the base of TR209 thus

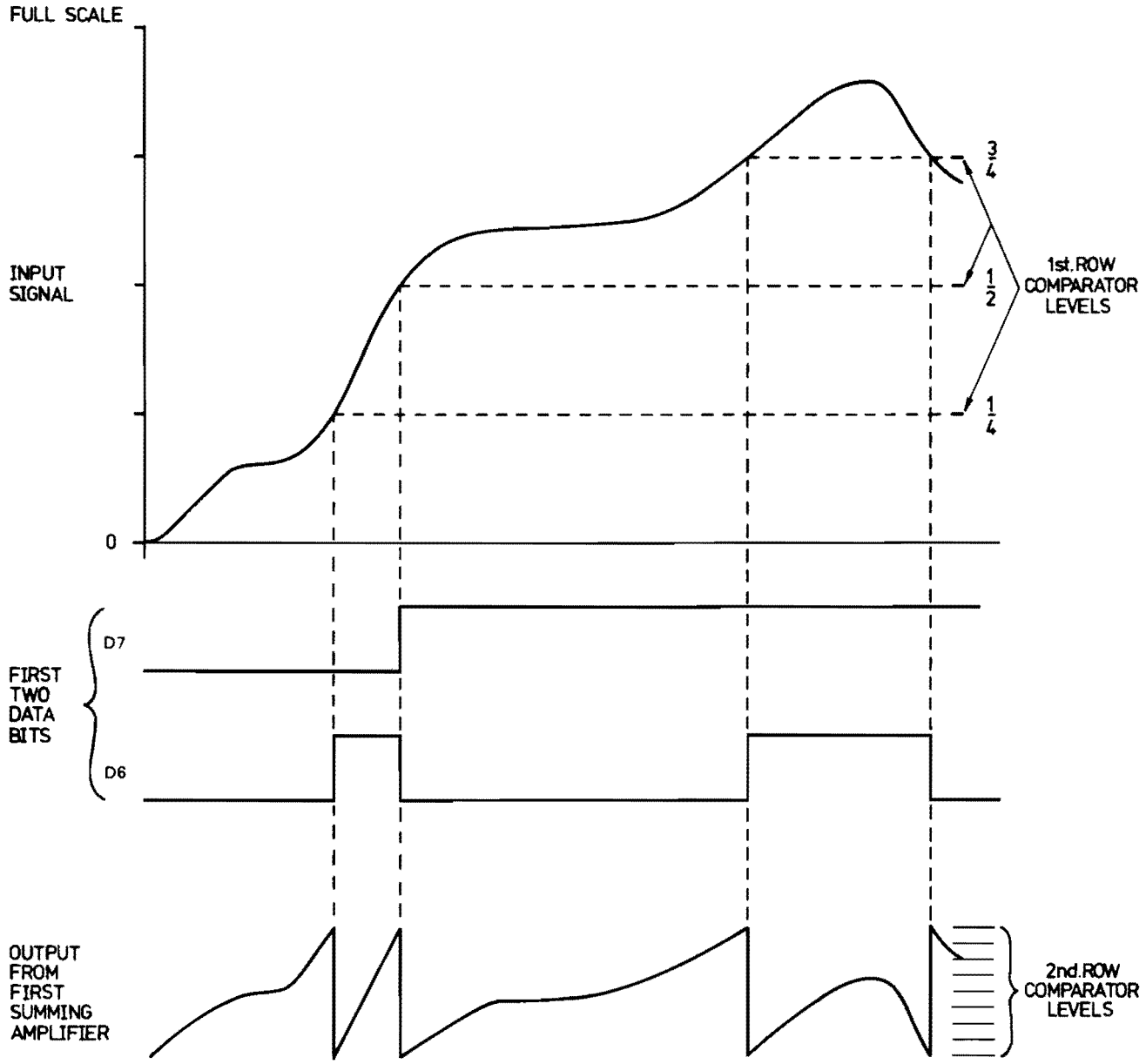


Fig. 4.3 Typical Signal Waveforms (ADC)

maintaining the circuit in this state until C212 charges up via R218, and TR209 turns on again. In this way a large positive-going pulse, approximately 100nsec. long, appears at the gate of TR208. During this time TR208 conducts and charges C210 to the input signal voltage present at the emitter of TR206. The injection effect of the gate-drain capacitance in TR208 is compensated by driving TR211 gate with the inverse of the signal fed to TR208 gate. Similarly the drain-source capacitance of TR208 is balanced by an anti-phase signal applied via C206. The voltage stored across C210 is buffered by a voltage follower comprising TR213, TR214 and TR215. TR213 is a source follower driving the emitter follower, TR215. The operating current of TR213 is defined by an identical transistor, TR214, operating in a similar manner to the Y Pre-Amplifier input stage as described in section 4.3. The low impedance output at the emitter of TR215 is fed to the first row of comparators, IC111 and IC112, and also to the first summing amplifier, IC102a.

4.4.4 COMPARATORS AND DECODING LOGIC

The comparators are very high gain integrated circuit differential amplifiers. The signal is applied to the non-inverting input and a reference voltage to the inverting input. If the signal voltage is less than the reference voltage the output of the comparator will be at its low limit. When the signal rises above the reference voltage the output goes to its high limit. The gain of the device is sufficiently high to ensure that the output will be at one limit or the other under most practical circumstances. The reference voltages for the comparators are generated by chains of precision resistors, R266–R268, R278–R284 and R146–R152, in conjunction with constant current source circuits. Since the digital to analogue convertors shown in the block diagram also employ current sources, these are grouped together and described later.

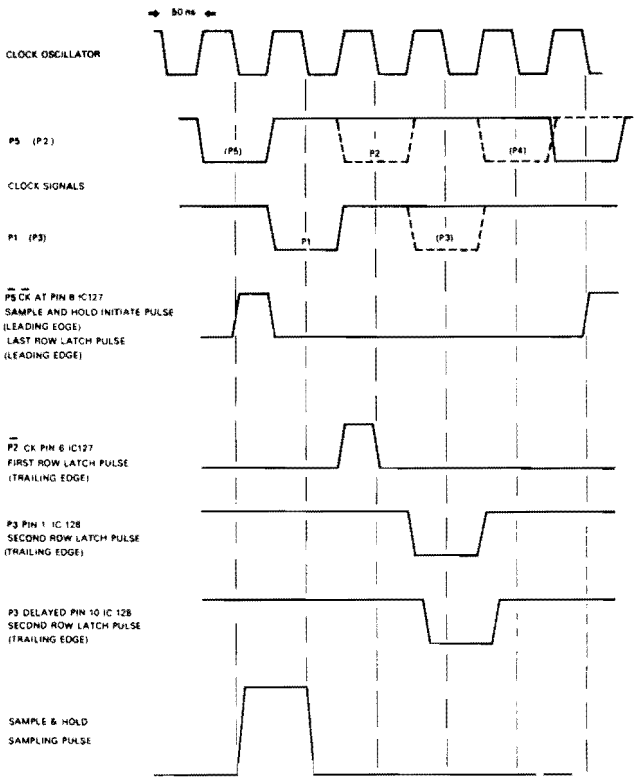


Fig. 4.4 Timing Signal Waveforms (ADC)

The outputs of the comparators are taken to the decoding logic. This provides binary coded output data corresponding to the state of the comparators, and is implemented with T.T.L. integrated circuits. Since the signal applied to each row of comparators is dependent on the state of the previous row, the full 8 bit conversion is carried out in a 'ripple through' fashion with a time lag between each of the three sections to allow for the settling time of the comparators and summing amplifiers.

The timing signals for the system are derived from a 10MHz oscillator driving a divider which generates the basic 5 phase 2MHz clock. This circuitry is included on the timing logic board (See Fig. 5.13). The waveforms and relative timing are shown in Fig. 4.4 and the method of deriving them is explained in section 4.5.3. The five subsidiary clock pulses are labelled P1 to P5 and these are gated with the original clock frequency in various combinations to derive the timing signals for the decoding logic as shown.

The outputs of the first row of three comparators are applied to the latching bistables, IC120a, b, c, which are clocked approximately 100nsec. after the end of the sample-and-hold pulse to allow the comparators to settle. Binary decoding is performed by IC121b, c, and the decoded outputs applied to the first two switched current sources which perform the function of the first DAC in the block diagram Fig. 4.3.1.

The outputs of the second row of comparators are latched in two stages. The three outputs necessary to obtain the two most significant of the three bits of data available from this stage are latched in IC123a, b and IC124a. The outputs of these three latches are decoded

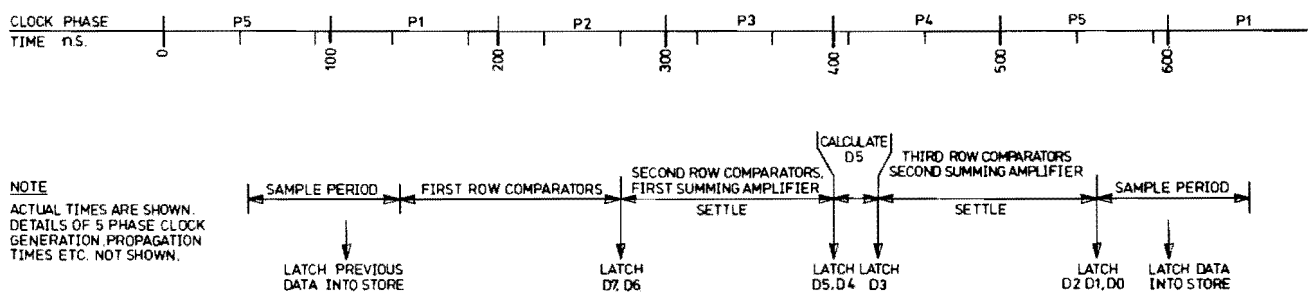


Fig. 4.5 Timing Chart (ADC)

in a manner similar to the first row of comparators, by IC122c, d. The decoding of the third data bit is carried out directly from the comparator outputs by IC122a, b, IC121a, d and IC125a. The decoded output is then latched by IC124b. To allow for the delay incurred by these gates, the clocking pulse to IC124b is delayed with respect to that applied to the other three latch bistables, by the four invertors, IC128a, b, e, f. The decoded binary outputs are applied to the remaining three switched current source circuits and remaining undecoded fraction of the analogue input signal applied to the final row of seven comparators. The decoding logic the final row is identical to that for the second row, except that the least significant of the three decoded bits is not latched at all hence there is no need for a delayed clocking pulse to this section.

The relative timing of the various operations performed during each cycle is shown in Fig. 4.5.

4.4.5 CURRENT SOURCES

Within the A–D convertor circuit, Fig. 5.12, there are a total of eight current source circuits. Three are employed supplying a fixed current to each of the resistor chains which define the reference voltages for the comparators.

The remaining five are switched by the data outputs from the decoding logic. A common reference voltage is supplied to all of the current source circuits by the voltage regulator, IC101. The bases of the p.n.p current source transistors, TR132, TR136, TR139, TR141, TR144, TR147, TR150 and TR151, are connected to this reference line and precision resistors in the emitter circuit define the collector current in each transistor. The regulator, IC101, establishes the common reference line by comparing the voltage across R107, R266, R267 and R268 which is proportional to the output current of the first current source, with its own internal stable voltage reference. This internal reference, which is available at pin 4 of IC101, is attenuated to a suitable level by the potential divider chain, R104, R105 and R106, and applied to one input of the error amplifier, pin 2. The other input of the error amplifier on pin 3 senses the voltage across the resistor chain mentioned. In this way the regulator compensates for the effects of supply line drift, temperature sensitive transistor characteristics, etc. A current limit facility is provided by the regulator: when the voltage drop across the series resistor, R103, exceeds one forward base emitter drop (approximately 0.6 volt), the regulator is shut down preventing overdissipation.

Two of the current sources, TR132 and TR141, feed buffer transistors, TR133 and TR140, respectively, in order to supply the relatively high currents required by the first two comparator voltage reference chains.

The switched current sources are all identical with regard to circuit operation. Taking TR136 as an example, the base of TR134 is driven by the most significant bit data output at standard T.T.L. logic levels. A high level at this point causes collector current to flow through the load resistor, R113, and the catching diode, D101, turning off TR135. The current source transistor, TR136, then operates in the normal manner with its emitter current defined by R114 and R115. A low level at TR134 base turns off the transistor and R113 pulls TR135 base positive, turning this transistor fully on a robbing TR136 of its emitter cirrent.

The currents of the first two switched current source transistors, TR136 and TR139, flow into a low impedance node in the first summing amplifier and the remaining sources, TR144, TR147 and TR150, into a similar point in the second summing amplifier.

4.4.6 SUMMING AMPLIFIERS

The two summing amplifiers employed in Fig. 5.12 are identical except for the value of the feedback resistor fitted. The component references mentioned in the following description apply to the first amplifier which drives the second row of comparators. IC102 is an integrated circuit array of five closely matched transistors, two of these forming a long-tailed pair differential input stage with a third acting as a current sink for this stage. A p.n.p. common emitter stage, TR219, amplifies the signal developed across the collector load resistors, R237 and R246, and an emitter follower, TR212, provides a low output impedance. These stages form a high bandwidth, differential input amplifier with negative feedback applied via R249 to the inverting input at the base of IC102b. The analogue input signal from the sample-and-hold output transistor, TR215, is applied to the non-inverting input at the base of IC102a, and appears at the output of the amplifier at the emitter of TR221 by virtue of the unity voltage gain feedback arrangement. However, the current from the switched current sources is injected into the inverting input of the amplifier at the base of IC102b and flows through the feedback resistor R249 developing a negative offset voltage at the output, proportional to the total current injected. Thus the output signal from the amplifier represents the analogue input signal minus the first two bits of data already detected, which correspond to ¼. ½ or ¾ of the full scale input. The signal fed to the second row of comparators and the second summing amplifier input, ranges from zero to one quarter full scale.

The second summing amplifier operates in an identical manner except that the feedback resistor, R256, is one quarter of the value of R249. This affects only the magnitude of the injected currents which represent the three bits of data detected by the second row of comparators, that is, 1/32 to 7/32 full scale.

4.5 STORE CONTROL AND LOGIC

4.5.1 GENERAL

The heart of the digital storage system is an 8 bit wide, 4096 long, static random access memory. Random access in this case means that a new non-sequential address may

be presented to the store each 250nsec. This address may be supplied from one of three sources:

1. The write address counter. This 12 bit counter specifies the address into which input data is to be written as part of a trace recording sweep.
2. The read address counter. This 12 bit counter specifies the address from which data is to be read for the c.r.t. display.
3. An externally supplied (12 bit) address, which will be supplied by the 4022 option when fitted. This enables the 4022 to specifiy the address:-
   a) that data will be read from the plot output.
   b) that data will be read from for presentation to the digital interface.
   c) that data supplied from the digital interface will be written into.

4.5.2 OPERATION IN REFRESHED MODE (See Fig. 4.6)

At all times, the data which is in the store is displayed. The display rate is constant and is unaffected by writing into store. As shown in Fig. 4.12, the store address bus is continually switched between the read and write address counters. Data from the store becomes stable toward the end of a read period and is latched at the end and presented to the D to A converter.

The start of a display sweep may be taken as the point at which the read counter is freed to count. It will proceed to increment at a rate of 1MHz. The read address counter presets the ramp bistable which in turn starts the ramp generator, producing an X-ramp, in synchronism with the read counter. Data is read, non-destructively from all 4096 Store locations and converted to an analogue current. The dot joiner provides a smooth transition from one sample to the next. After the last sample has been read and displayed, the ramp bistable is cleared, causing the ramp to reset. The read counter is held at zero to allow time for the ramp to reset before the cycle starts again.

When the instrument is in dual trace or half hold mode, the display cycle is modified to display even numbered store locations on one sweep and odd numbered store locations on the next. In dual trace, these will be CH1 and CH2 locations respectively. The least significant read address bit is intercepted before it reaches the store and is replaced by a signal which changes state at the end of each display sweep. This produces the required alternate effect. The rate at which sample pulses are sent to the dot joiner is halved as only half of the store is displayed on each sweep. CH2 samples are displaced to the right of those of CH1 on the CRT following the manner in which they were sampled.

If display expansion is selected, the above cycle is modified in that the displaying sweep is faster and that the read counter is not cleared at the end of sweep, but is returned to the start address of that segment. End of sweep occurs when 13cm (approx) have been displayed.

Newly converted data from the A to D converter is presented to the store input at 500nsec intervals continually. At the fastest timebase range, each of these samples would be written into store during a write sweep. A reduction in timebase rate is effected by regularly accepting one sample for each N arriving where N is the timebase division ratio as shown in Fig. 3.13. Between write sweeps, the write address counter is cleared and the write enable line is permanently HI, ignoring all data presented to the store. The update bistable is freed to accept trigger pulses. When a trigger pulse is received (or after a 250msec wait when AUTO TRIGGER is selected) the UPDATE line goes HI starting the write sweep. When the next write rate pulse arrives, the current data from the ADC is written into the first store location as dictated by the write address counter. The latter is then incremented. In this manner, data is written into all the following store locations. After the last location has been written into, the update bistable is cleared terminating the write sweep. If the instrument is not in the single shot mode, the update bistable is immediately freed to accept the next trigger pulse. The single shot mode is initiated by pressing the arm button. The ARMED LED will light until the UPDATE line goes HI, when the TRIG'D LED will light. A write sweep then takes place as previously described. However, at the end of the sweep, the STORED LED is lit and the UPDATE bistable is NOT freed to accept trigger pulses. While the STORED LED is lit, the WRITE ENABLE is permanently HI protecting the data in store.

Pressing the DISPLAY HOLD button overides the UPDATE signal forcing the WRITE ENABLE LINE permanently HI and freezing the write address counter immediately. When the button is released, writing will continue from the store location at which it was stopped.

If the HOLD ALT. SAMPLES button is pressed writing is disabled whenever the least significant write address bit is HI, thus write protecting odd valued store addresses.

4.5.3 OPERATION IN THE ROLL MODE (see Fig. 4.7)

The essential feature of ROLL mode is that when the instrument is free running, data is written into store continually, unaffected by trigger. The roll effect is created by offsetting the display sweep such that the address currently being written into appears at the right hand edge of the display. This offset is accomplished by adding the contents of the read address counter to that of the write address counter to produce a new read address for the display. If the initial assumption is made that the read address is incrementing substantially

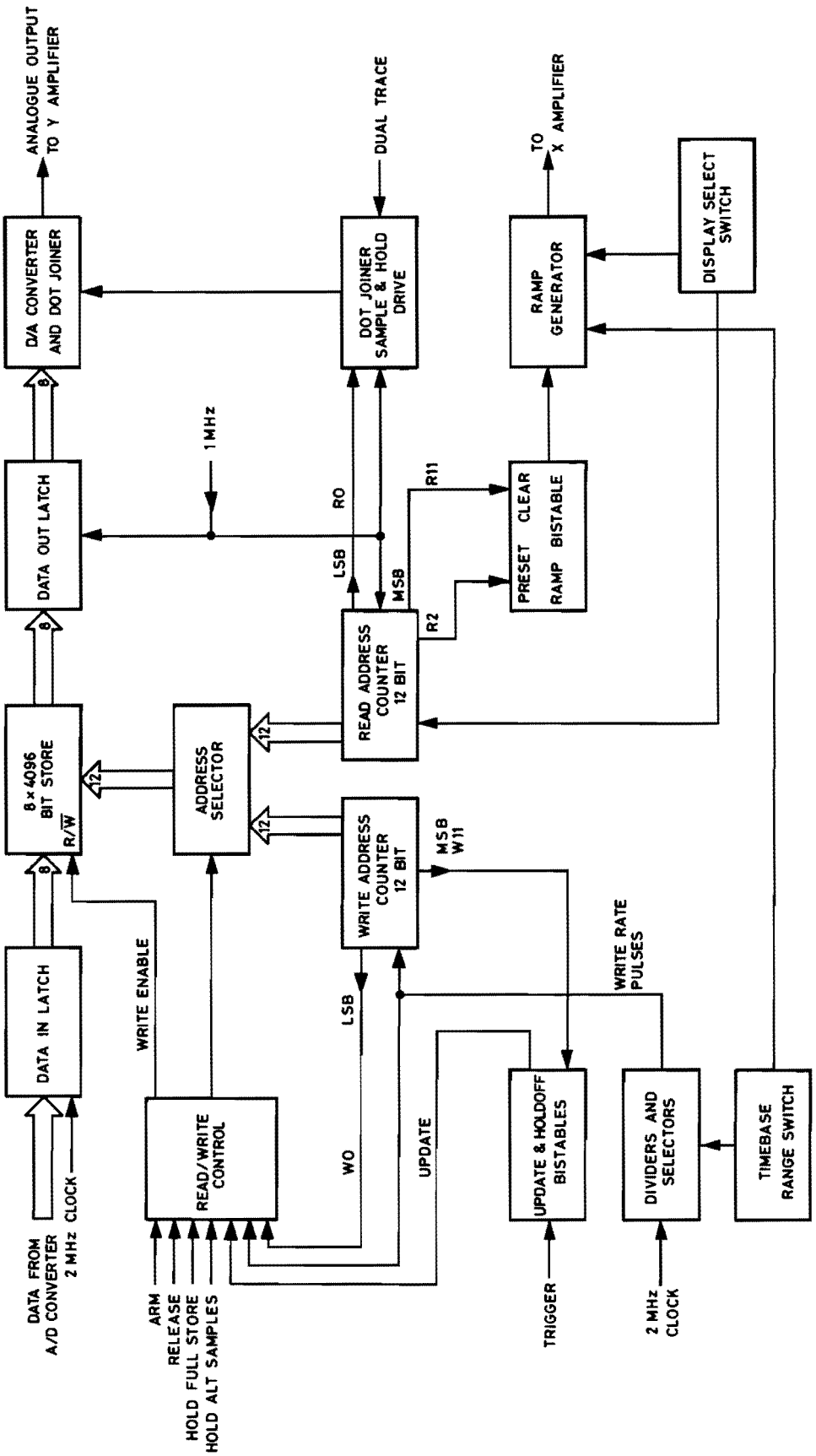


Fig. 4.6 Logic Function Diagram: Refreshed Mode

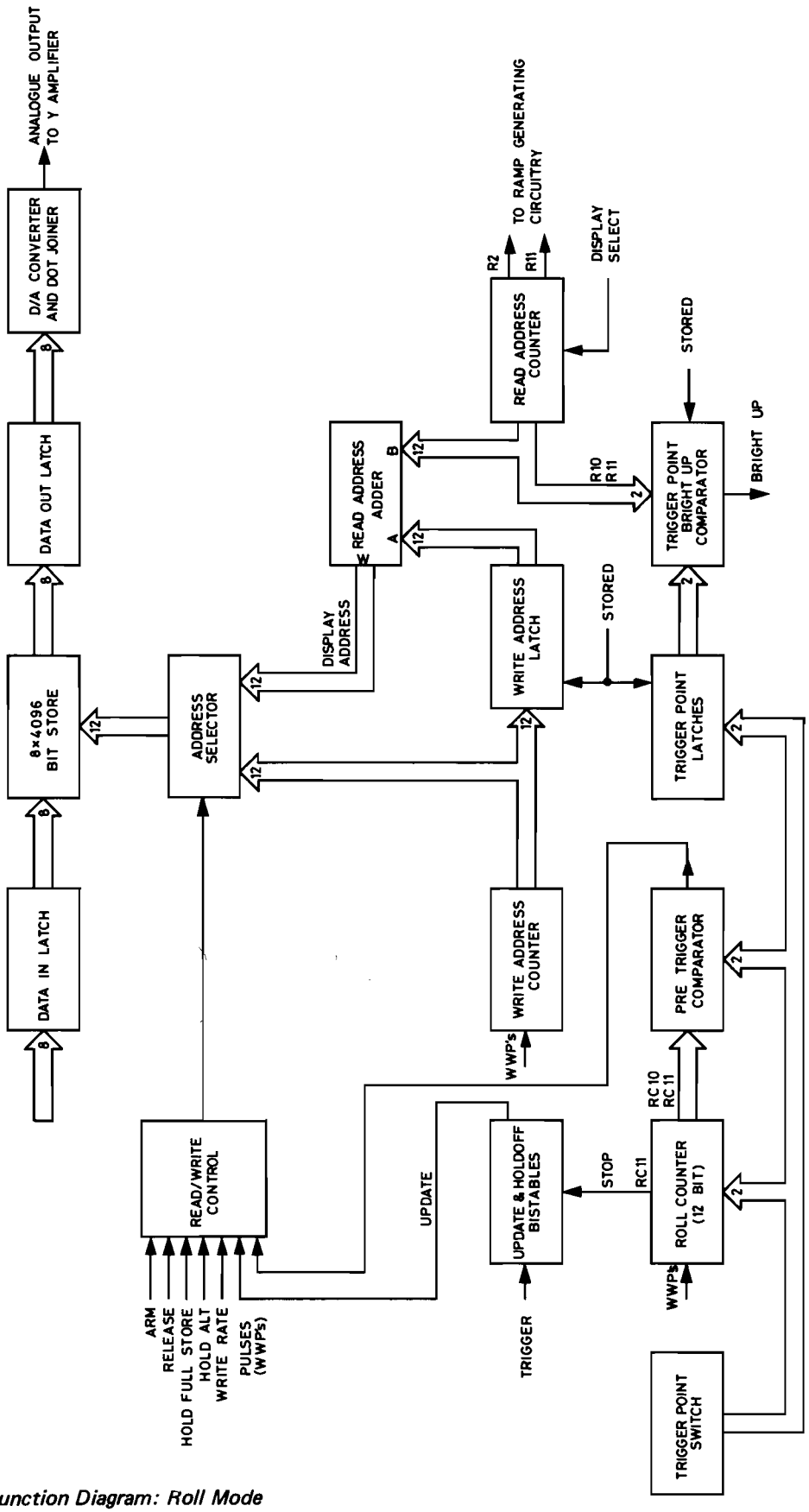


Fig. 4.7 Logic Function Diagram: Roll Mode

faster than the write address counter, then it is apparent that as the read counter cycles from 0 to 4095, the display address will cycle from the current write address through 4095, zero and back up to write address minus 1. At the fast write rates, the visual effect is less meaningful.

As in the REFRESHED mode, the display is continuous, the action of read address counter and ramp generator being as previously described. When the instrument is free running, the write address latches are made transparent, allowing the current write address to the adder. The conditions which have to be met by a ROLL SINGLE SWEEP are:

1) The trigger point must appear in the selected position.
2) The store must contain all new information i.e. there must be no discontinuity at the trigger point.

Point (2) may be satisfied by rolling (entering data) at least until the pre-trigger fraction of the store has been refilled before accepting trigger. Then, even if the oscilloscope triggers immediately, requirement (1) will ensure that only new information is captured. This will be referred to as the pre-trigger requirement.

As writing is continuous in the ROLL MODE, point (2) is only considered relevant when exiting the stored mode or from switch-on.

The single sweep is best described by assuming the instrument to have reached the STORED condition (from a previous single sweep). Under these conditions, the store will be frozen and the roll counter cleared. When the ARM button is pressed, the roll process previously described will start and the ARM LED will flash but the trigger circuit will be held off. The roll counter will start to increment at the same rate as the write counter. The pre-trigger comparator trips when the contents of the roll counter agree with the pre-trigger requirement. At this point the ARMED LED will steady and trigger will be enabled. This represents the earliest point at which the instrument may be allowed to trigger if all new data is to be entered into store. The roll continues but the roll counter is held at the current pre-trigger selection. It will follow if the switch is moved. When a trigger is accepted, the LED sequence moves to TRIGGERED, the UPDATE signal goes HI and the roll counter is freed to count. At that instant, all data in the store is pre-trigger. When the roll counter overflows, the instrument moves to STORED and the update bistable is cleared terminating in the write sweep. In the example quoted of ¾ pre-trigger, at the instant of trigger the roll counter would be held at ¾ and all displayed data would be pre-trigger. It can be seen that as the roll counter progresses to full count, ¼ store of post-trigger information would be written into store.

If END TRACE is selected, the instrument will move straight from TRIGGERED to STORED. When the instrument reaches the STORED mode, the write address latches freeze the final contents of the write counter stabilising the display. The trigger point selection is also latched. The trigger point now appears ¼, ½, ¾ or full screen from the left hand edge of the screen. As the latter always corresponds to a read counter address of zero, the trigger point on the display is indicated by causing a bright-up when the read address corresponds to the (latched) trigger point selection. If ARM is pressed, the above cycle is repeated. If release is pressed, the roll and write counters are released to count. The roll counter counts to its pre-trigger point as defined above. If the ARM button is pressed after this point is reached, the trigger circuit will be enabled immediately.

4.5.4 DISPLAY MODE CONTROL (Fig. 5.13)

Switch S601 produces two signals to the Display Mode circuitry arriving at U607 pin 13 and U611 pin 3 as shown in Fig. 4.8.

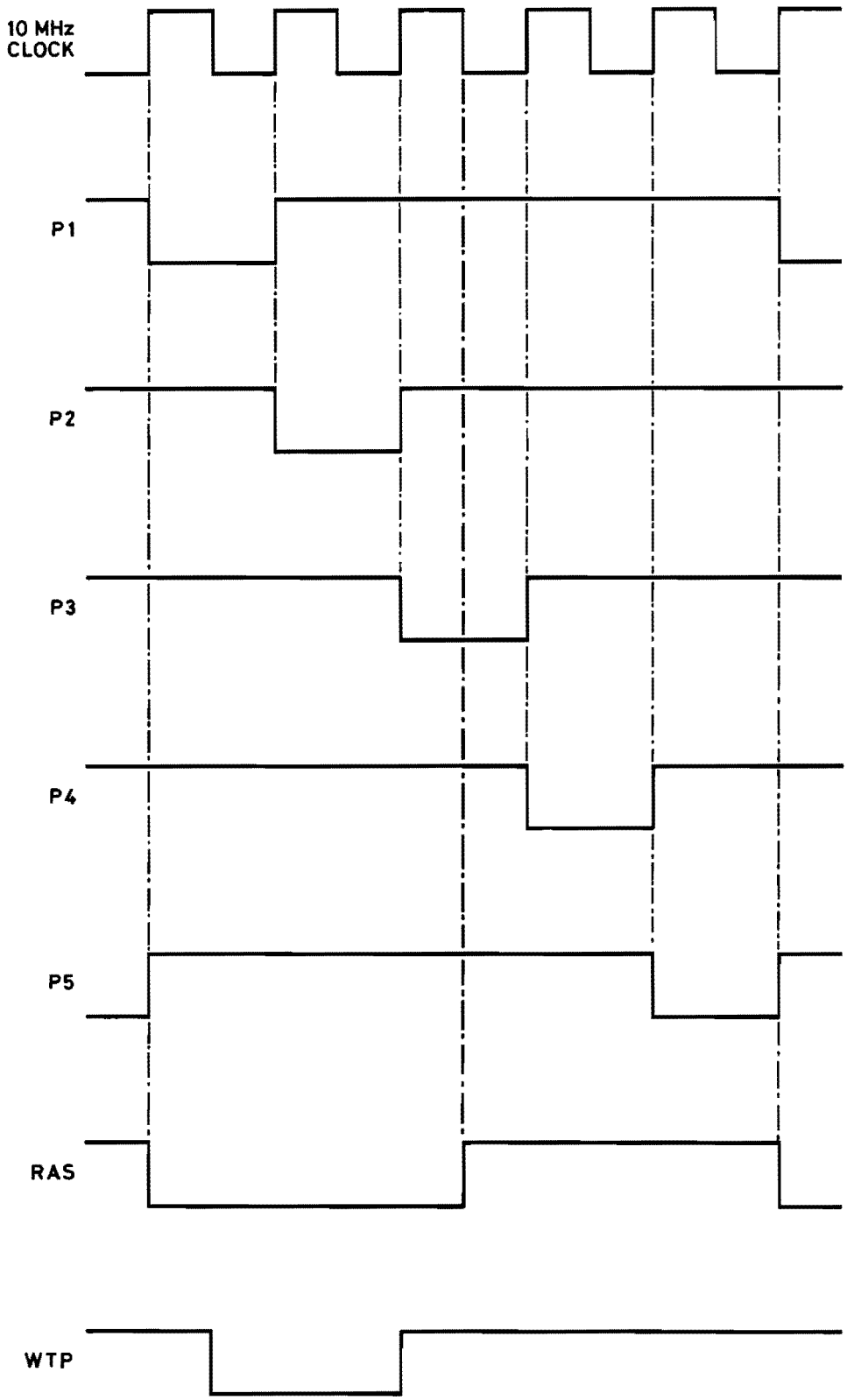
Mode Selected	U603 Pin 13	U611 Pin 3	U607 Pins 4,12	U607 Pins 5,11	U607 Pins 6 10
NORMAL	0	1	1	1	0
REFRESHED	1	1	0	1	1
ROLL	1	0	1	0	1

Fig. 4.8 Display Mode Signals

U607 pin 3 will normally follow U611 pin 3 except when one of the bottom 5 timebase ranges is selected. Under those circumstances U632 pin 2 is driven LO which in turn forces U607 pin 3 HI, converting the selection of NORMAL mode to REFRESHED.
The (b) outputs of U607 produce the NORM, REF & ROLL signals, the (a) outputs drive the corresponding LED's. The STO input to pin 2 causes the (a) outputs to go HI turning off the LED's.

4.5.5 CLOCK GENERATOR AND RANGE DIVIDERS (Fig. 5.13)

The clock oscillator consists of Q601 and Q602 connected as an emitter coupled multivibrator, with the frequency adjusted to 10MHz by C607. Q603 translates to TTL levels. U641 (a) & (b) provide buffered CK and $\overline{CK}$ respectively for distribution. U618, a quad D-type device, is connected as a shift register Q0→ Q1→Q2→Q3 with the shift register input provided by the output of U619 pin 6. The latter remains HI until all Q's are HI whereupon it goes LO. This LO gets shifted to Q0 after one clock period causing a HI again. Thus each Q output produces a LO for one clock period as shown in Fig. 4.9. U619 pin 6 represents P5, but due to propagation delays through the shift register it has a narrow spike after each active



NOTE. FOR CLARITY DEVICE DELAYS ARE NOT SHOWN.

Fig. 4.9 Major Timing Signals

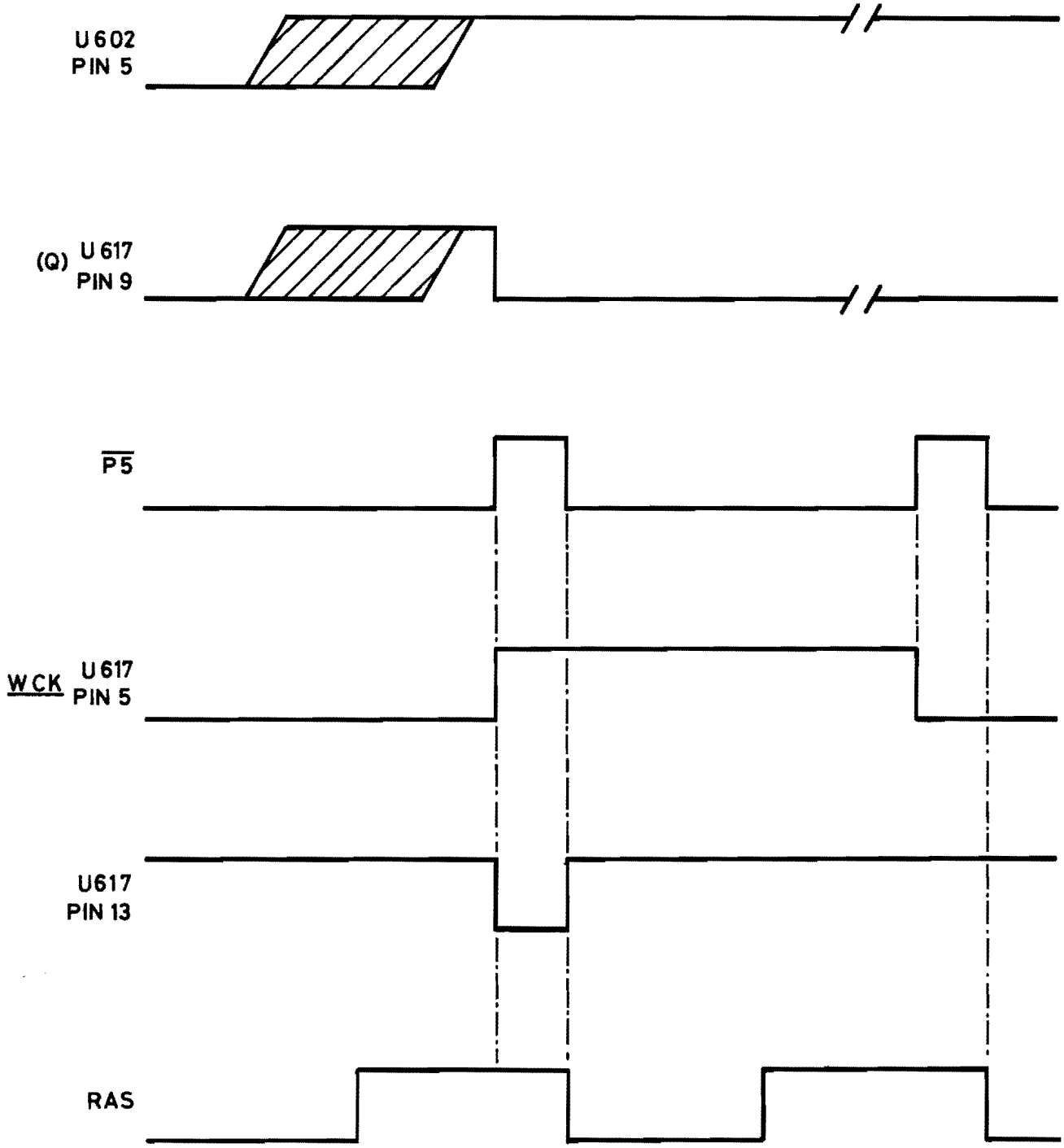


Fig. 4.10 Write Clock Retiming

clock edge. The P5 pulse is thus generated by extending the shift register with U631(a). P1 — P5 provide fine timing for critical events within the 500nsec basic period of the instrument. Another major timing signal is RAS (see Fig. 4.9). It runs at the 2MHz basic frequency and defines the READ/WRITE distinction. U642 (b) and (c) provide a set/reset bistable which is reset by the start of P1 and set at the middle of P3 (gating $\overline{CK}$ and $\overline{P3}$ by IC 642 (d) provides the required signal).

The other major repetitive signal is the Write Timing Pulse WTP, which is used to provide the Write Enable pulse to the stores. Its width and positioning with respect to RAS allows for data and address settling times. Similarly to RAS, it is driven LO half way through P1 and driven HI at the start of P3.

RAS is also used as the range divider input and represents the fastest data capture rate available. U606, a dual decade divider, produces RAS/5 on pin 7 and RAS/2½ on pin 5, the latter being achieved by producing two output pulses for every five applied. Data selector U616 enables a selection of RAS, RAS/2½ or RAS/5 to be made by control of its two select inputs. All other required ranges are obtained by decade division from U616 pin 7, the above mentioned output. U601, U609 and half of U606 produce five further decades of division. Data selector U602 then selects one of these divisions under control of its three select inputs. Fig. 3.13 shows the division ratios achieved. Note that if all select inputs of U602 are HI, then external clock is selected. The signal at the output pin 5 of U602 is at the required data capture rate, but must be rephased to the master timing signal RAS. U617 accomplishes this as shown in Fig. 4.10. A positive edge from U602 clocks a '1' through to the Q (pin 9) of U617 to appear at the D input of 617(a). The next positive edge of $\overline{P5}$ clocks this through to the Q of U617(a) which in turn is gated with $\overline{P5}$ to clear U617(b) taking the D of U617(a) LO. At the next positive edge of $\overline{P5}$, therefore the Q of U617(a) goes LO. The Q of U617(a) is thus a positive pulse of one RAS period duration at the selected write rate. It is termed the write rate clock, WRC. Note that if the fastest write rate is selected, then WRC will be permanently HI.

4.5.6 READ CHAIN (Fig. 5.14)

The read address counter is a 12 bit counter made up from a dual four bit binary counter U735 and a parallel loadable four bit counter U736. As previously mentioned, the store read sequence is independent of the write sequence and continuous. Indeed the read counter is not even stopped in NORMAL mode. The read clock, RCK, provided via SKAX pin 4 comes from U625 pin 10 inverted by U636(c). As shown in Fig. 4.12 the read clock is at 1MHz (RAS/2) rate, continuous, and increments the read counter at the end of a read period. This allows 250nsec for each change to ripple through the counter. The read chain interacts with the display ramp circuitry to a large extent. No real detail will be given at this stage as it is dealt with in section 4.6.7. The collector of Q710 is connected to that of Q919 in the timebase such that the former is driven LO whenever (and however) the display ramp is reset. Assume that the clear has just been removed from the counter and that the entire store is being displayed. The counter starts from zero and data is read from each store location (see Fig. 4.12 for timings) to 4095, when the count reaches 8, falling edge of R2 starts a display sweep. When the counter overflows to zero, the negative edge on R11 fires the end sweep monostable U731(a) turning on Q710, which in turn, initiates a display-ramp reset and fires the display hold-off monostable U731(b). The latter stops the read counter for a period long enough to allow the display ramp to reset fully before the sequence starts again. The hold-off signal DHO holds the two least significant address counters cleared but parallel loads U736 (with zero in this case). Quadrant expansion requires that the read counter starts from a number defined by the expansion switch. (see Fig. 4.11). This is achieved by presetting U736, during hold-off as previously described, as shown in Fig. 4.11.

	L2 U736 (Q_B)	L15 U736 (Q_C)	L1 U736 (Q_D)
FULL STORE	0	0	0
1st QUADRANT	0	0	0
2nd	1	0	0
3rd	0	1	0
4th	1	1	0
5th	0	0	1
6th	1	0	1
7th	0	1	1

Fig. 4.11 Programming of U736.

U736 QA (A8) and all lower address lines are held LO during the hold-off period. The quadrant sweep ends either by analogue termination (see Section 4.6.7) or by R11 going LO (whichever happens first) firing the hold-off mono. The entire store is displayed at 400 samples per cm and thus the entire store may be displayed in 10.24cm. Under these circumstances, the negative edge of R11 arrives before the display ramp reaches its analogue reset voltage. When quadrant expansion is selected, reset is analogue except in the case of the last quadrant. The display is limited to approximately 13cm, which at 80 samples/cm (x5 expansion) displays just over 1024 samples. At 100 samples/cm (x4 expansion) displays approximately 1300 samples. The frequency of the clock to the counter is not affected by quadrant expansion. The

read address passes through the READ/PLOT multiplexer (see Fig. 4.12) to the address adder (U726 to U728) where it is added to the contents of the write address latches to produce the display address. The latter then passes through the READ/WRITE multiplexer U717 to U719 to the store. In the REFRESHED mode, the write address latches are cleared and thus the displayed address is equal to the read address. In roll mode, the latches hold the current write address retimed to be stable during the read period and thus the display address is equal to the sum of the read and write addresses. D7 is inverted at the store input (and is of course stored in inverted form) and then inverted after being held in the store output latch U704 producing no overall inversion. However, clearing U704 will produce a steady half-full-scale signal useful for calibrating the DAC. In NORMAL mode the read counter continues as a signal source for the calibrator and chop but as the End-sweep and Display Hold-off functions are not required U731a & b are disabled by $\overline{\text{NORM}}$ and the read counter continues uninterrupted.

4.5.7 THE WRITE CHAIN (Fig. 5.14)

Write timing signals are shown in Fig. 4.13. The rate and manner by which data is written into store is not affected by the REFRESHED/ROLL selection and proceeds as follows.

The output from U617(a) is the Write Rate Clock (WRC). In the period under consideration it passes through to U619 pin (8) or U604 pin (8) as appropriate to appear at U632 pin (6) as the Write Gating Pulse WGP. Consider the positive edge of one such pulse as a T + O. Reference to the ADC timing chart Fig. 4.4 in conjunction with Fig. 4.13 shows that an ADC sample will be presented to the converter at approximately T + 150nsec. This is the sample to be associated with T + O. The beam switch is changed at T + 100nsec (if in dual trace). Due to device delays this change arrives at the sample and hold immediately after the latter has operated and is ready for the next sample. As indicated in Fig. 4.13, the converted T + O sample is latched at T + 600. As shown this is written into store in the immediately following write period. Ideally, the write counter should be incremented immediately after writing i,e, at T + 850nsec as shown by dotted line on WO. To reduce this delay, the address counter is incremented before writing and the beam switch is inverted to compensate utilising the symmetry of the beam switch signal (solid line on WO). Note that as the write counter is incremented before writing, the initial store location is not written into at the start of a write sweep.

The connections of U619, U604 & U632 produce an and/or select on WRC with common connections such that WGP stays HI if:

a) The HOLD button is pressed, $\overline{\text{HLD}} = 0$

b) The STORED LED is lit, $\overline{\text{STO}} = 0$

REFRESH MODE, using U604 imposes the further requirement that RFQ should be HI for WGP pulses to be present. ROLL MODE imposes no further requirements.

The $\overline{\text{WE}}$ signal is produced by gating delayed WGP with WTP by U623. The input to pin 4 ensures that $\overline{\text{WE}}$ is HI if WO = 1 and HOLD ALT samples is selected. The clear to the Write Counter (WCC) is driven by U605 and U610 such that the counter is only cleared when the following are all true:-

a) RFS = 1 in Refreshed Mode

b) $\overline{\text{HLD}} = 1$ no Display Hold applied

c) $\overline{\text{STO}} = 1$ not in STORED mode at end of Single Sweep

d) RFQ = 0 a write sweep is not in progress.

This ensures that the write counter can be cleared only between triggered sweeps in Refreshed Mode.

4.5.8 WRITE OPERATION IN REFRESHED MODE

The write circuitry interacts with the trigger circuitry in the production of the RFQ signal. Detailed information is available in section 4.6.10.

The write sweep starts when a trigger signal drives RFQ HI. This enables WGP, removes the clear from the write counter and writing takes place as previously indicated. When the write counter over-ranges, the falling edge of W11 (on SKM 5) drives RFQ LO ending the write sweep. The latter is almost immediately available to be driven HI by a trigger signal.

4.5.9 SINGLE SWEEP – REFRESHED MODE

A simplified diagram of the single sweep circuitry is shown in Fig. 4.14.

The single sweep starts when the ARM button is pressed. The ARM signal going HI drives ARM REQUEST (ARQ) HI. U645(b) is a dummy under these circumstances with its Q output being HI or going HI almost immediately. The clock input of U622(a) is thus driven LO causing the Q to go HI. This is the ARMED (RMD) condition. RMD acting through U621(b) clears the ARQ signal. It also causes U608 pin 6 to go LO turning on the ARMED LED. As soon as RFQ goes HI, indicating a triggered sweep is in progress U608 pin 8 $\overline{\text{TRG}}$ goes LO indicating that the TRIGGERED state has been achieved. This signal acting on U608 pin 4 turns off the ARMED LED. Acting through buffer U612(c) it turns on the TRIGGERED LED. Note that if the single sweep had been started during a sweep, the RFQ signal would already have been present and the instrument would have skipped the ARMED state. The TRIGGERED state persists until W11 goes LO (this defining the end of sweep) clocking the RMD signal through to the Q of U622(b) indicating STORED mode (STO). This, acting through U621(c) clears the RMD signal turning

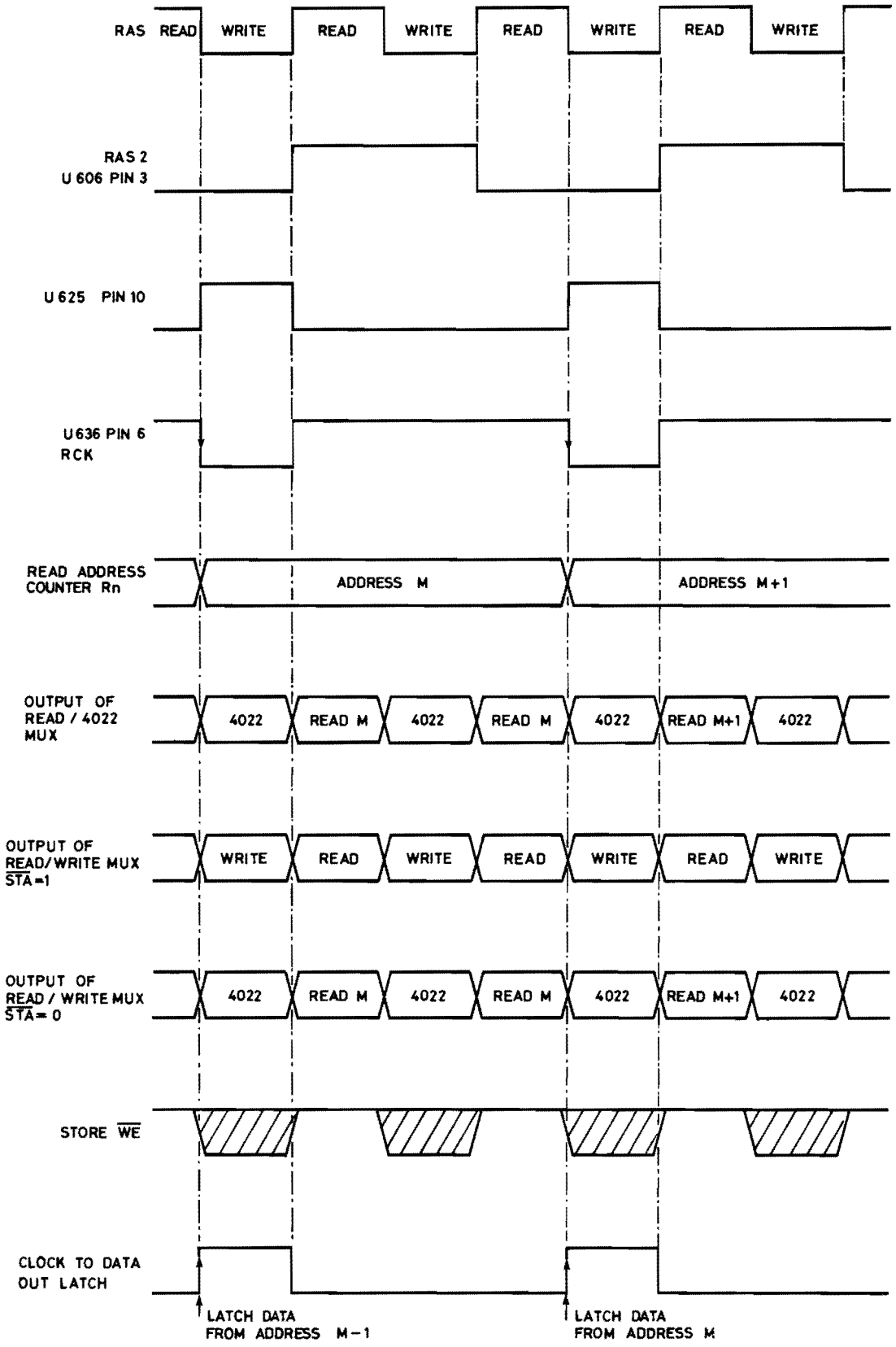


Fig. 4.12 Read & Multiplexer Waveforms

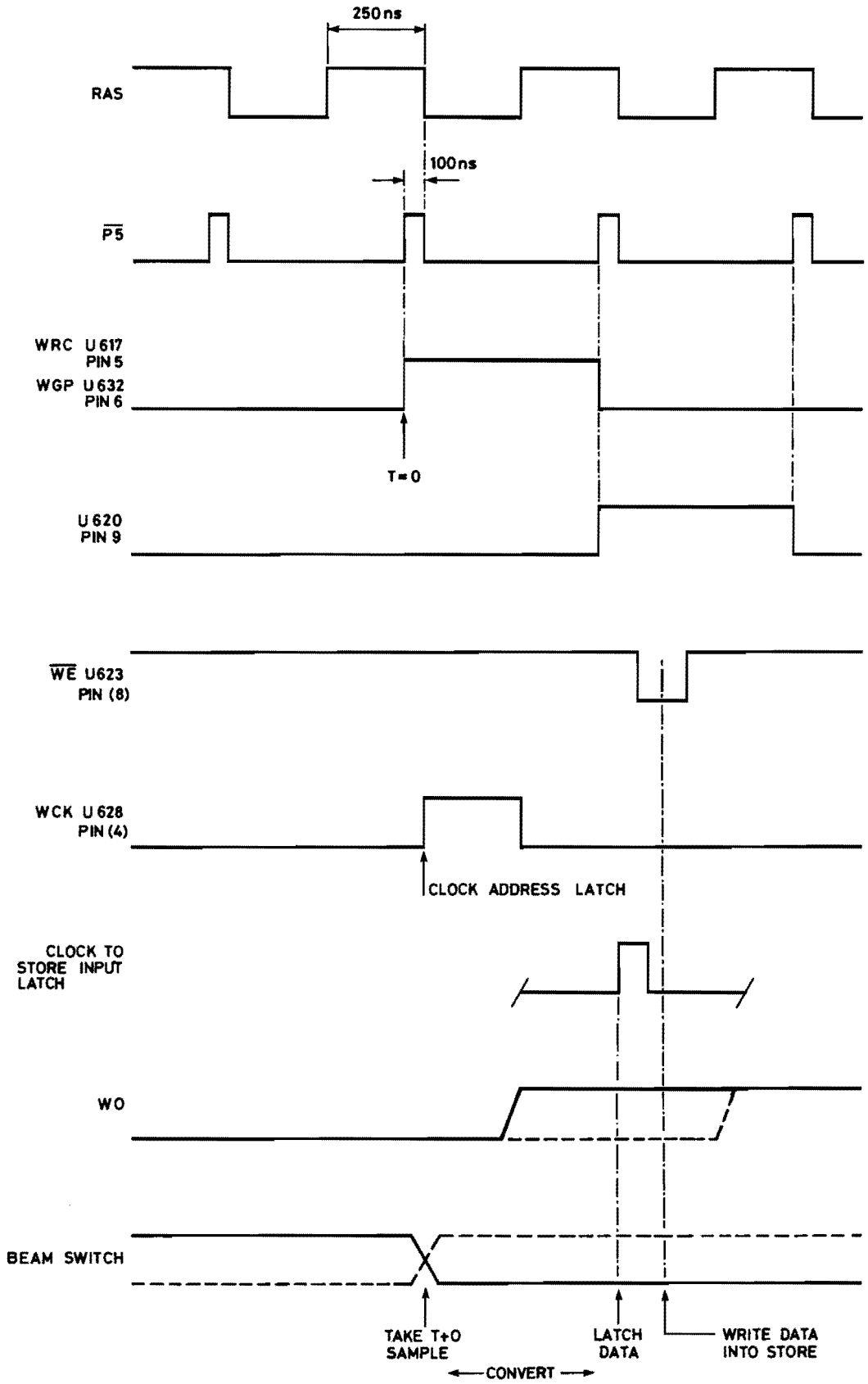


Fig. 4.13 Write Waveforms

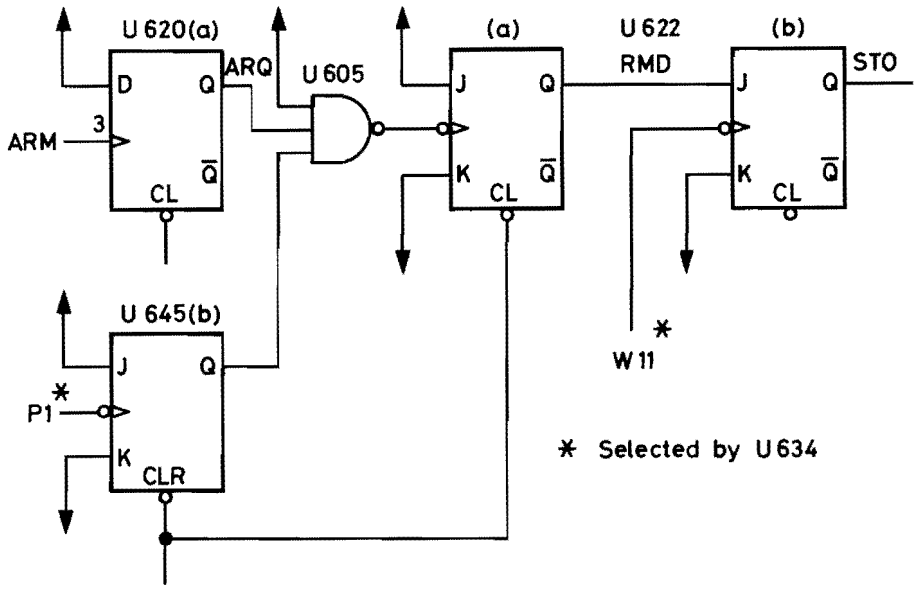


Fig. 4.14 Schematic of Single Sweep Circuitry: Refreshed Mode

off the ARMED LED. The STORED signal also affects the following:-

a) Acting through U621(d) it turns on the STORED LED
b) Acting on U604 & U619(b) it stops the clock to the write counter and also the write enable to the store, freezing the display.
c) It clears U645(b) (important in ROLL mode).
d) Acting on U607 it turns off the NORMAL/REFRESHED/ROLL LED's.
e) Acting through U610(b), U635(c) & (d) & thence to SKM(15), it causes RFQ to be held LO disabling further triggers (see section 4.6.10 for more detail).

If the arm button is pressed, ARQ acting through U621(c) clears U622(b) removing the STORED signal and starting another single sweep.

Pressing the RELEASE button clears U620(a) and U622 by drawing the common line on U621(b), (c), (d) HI

4.5.10 SINGLE SWEEP – ROLL MODE

As mentioned in section 4.5.3 the roll counter U640a & b plus U646 forms the major part of the ROLL SINGLE SWEEP. U644 (c) & (d) form a two bit comparator to compare PT0 with RC10 and PT1 with RC11 (refer to Fig. 3.12 for details of PT0 and PT1).

The roll counter receives clocks at the rate and timing of those to the write counter with the difference that they are continuous. The counter can only be stopped by clear/parallel load. When starting from zero, the roll counter increments until RC10 & RC11 equal PT0 & PT1 respectively whereupon the output of the pre-trigger comparator U644 pins 10 & 11 goes HI clocking a HI level through to U645(b) Q. This in turn, acting through U608(d)/U613(a) clears U640 and parallel loads U646. This condition is stable and indicates that the required minimum amount of pre-trigger data has been written. The parallel load ensures that RC10 and RC11 follow PT0 & PT1 when the pre-trigger requirement is changed.

The gate U605 driving U622(a) produces the effect that the latest of ARQ and pre-trigger comparison to arrive will clock U622(a) and produce the ARMED state. Should ARQ arrive first, U608(a) will gate the FLASH signal on pin 2 through to flash the ARMED LED. When RMD goes HI U608 (b) pin 6 goes LO turning on the LED steadily. The RMD signal acting through U610c, b, U635c, d enables the trigger circuitry (see section 4.6.10 for detail). As before, RFQ goes HI when a trigger is received, causing the instrument to enter the TRIGGERED MODE. The $\overline{TRG}$ signal, acting on U608(d) removes the clear from U640 and the 'load' from U646. The roll counter, now counts to ensure that the required amount of post trigger information is captured. This criterion is satisfied when the roll counter overflows to zero and RC11 going LO clocks U622(b) to drive the instrument into the STORED mode. In the special case where END TRACE is selected, the pre-trigger comparison does not occur until the counter has overflowed, and thus, RC11 cannot clock U622(b). U621(a) detects this switch setting and causes RC11 to be replaced by $\overline{TRG}$

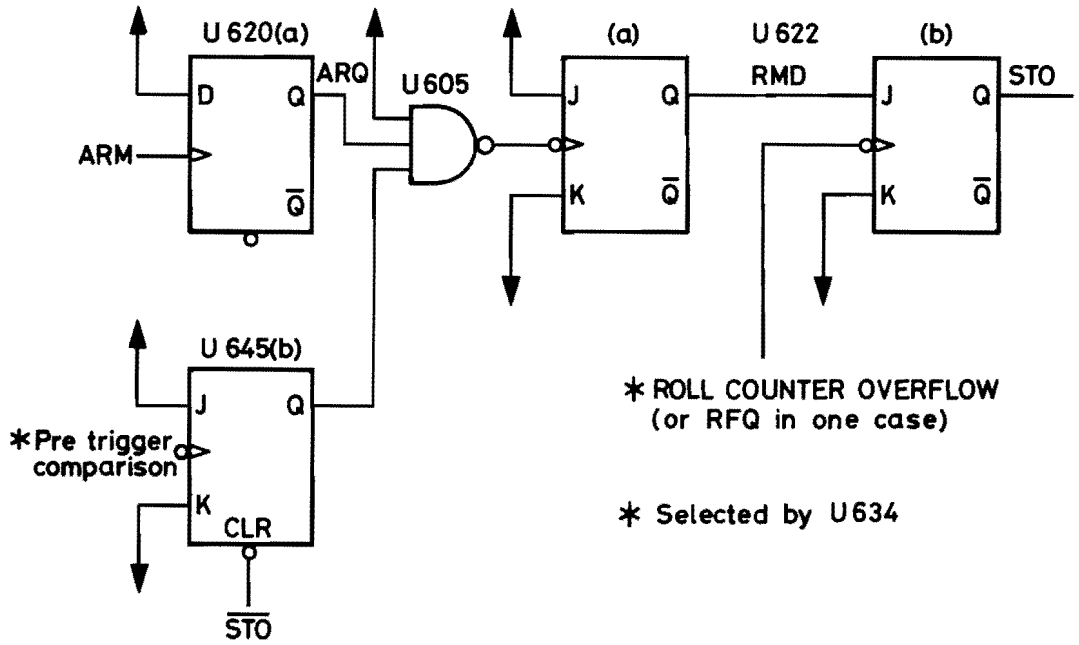


Fig. 4.15 Schematic of Single Sweep Circuitry: Roll Mode

for this purpose causing the instrument to move straight through TRIGGERED and into STORED mode.

The STORED signal holds the ROLL counter at zero and freezes the display etc. as previously described. When the instrument leaves the STORED mode, the roll counter is immediately freed for its pre-trigger count.

4.5.11 TRIGGER POINT BRIGHT-UP

Latches U643a & b are clockedby the write counter clock and thus when writing stops, they latch the value of PT0 and PT1 used during a single sweep. The comparator mode from U644a & b produces a positive edge whenever R10 & R11 equal PT0 & PT1 respectively. This signal clock a LO level to U615a $\bar{Q}$ to bright-up the trace. U637(a) acting through U638 ensures that the bright-up is only enabled when the instrument is in ROLL mode with STORED LED on. The R1 input to U638 terminates the bright-up after 2μsec.

4.5.12 BEAM SWITCHING (Fig. 5.13)

The static selection of CH1 or CH2 is provided by U633a & b. Selecting CH2 puts a LO on pin 1 forcing the output pin 3 HI. If CH2 is selected the LO in pin 13 drives pin 11 HI. Pins 1 & 2 are then HI driving the output LO. When DUAL TRACE is selected, the selection is controlled by pin 12. U626, which drives this pin, is connected as a selector. In NORMAL mode, the signal on its pin 3 is used. In the other two modes the signal on pin 5 is used.

NORMAL MODE

U645a provides the chop and alternate beam switching signals according to the timebase range selected (see Fig. 3.11), controlled by U638 pin 12. The latter goes HI to select Alternate. This signal drives the preset and clear of U645a HI. The RBQ signal on the clock of U645 causes the bistabel to change state at the end of each sweep as required for 'Alternate'. When U638 is LO, U645 is cleared. Under these circumstances, the Q output may still be driven HI if the preset input is also driven LO. In this case, the R1 signal acting through U632c causes the Q output to switch at 250kHz, the chop frequency.

DIGITAL MODES

Input pin 5 of U626 is driven by the Q output of U631b. The latter is a retimed version of W0 (described in section 4.5.7) which provides a beam switch synchronised to the write address counter.

4.5.13 CHOP BLANKING (Fig. 5.13)

This signal is only required in NORMAL mode to mask transients involved with chopping between CH1 & CH2. In both other modes, U612b grounds the chop blanking signal. The blanking signal is a.c. coupled and thus no blanking is produced by a static signal.

The signal on U625 pin 6 turns off the blanking when ALTERNATE is selected. The signal on pin 5 turns on the blanking when dual trace is selected. Chop blanking waveforms are shown in Fig. 4.16.

4.6 TRIGGER AND TIMEBASE (Fig. 5.16)

4.6.1 GENERAL

A block diagram is shown in Fig. 4.17.

The selected trigger signal is applied to the trigger amplifier, where it is amplified and level shifted by the trigger

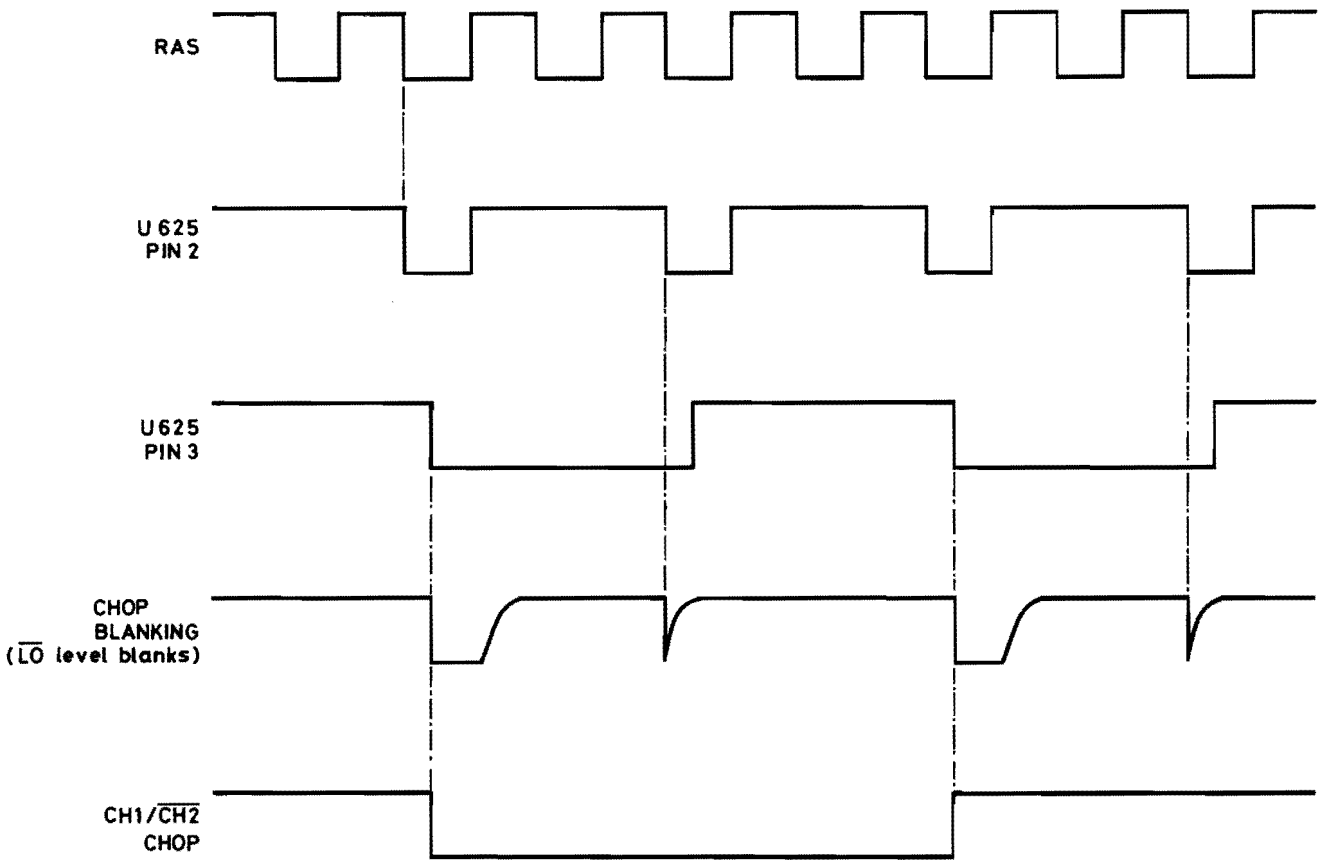
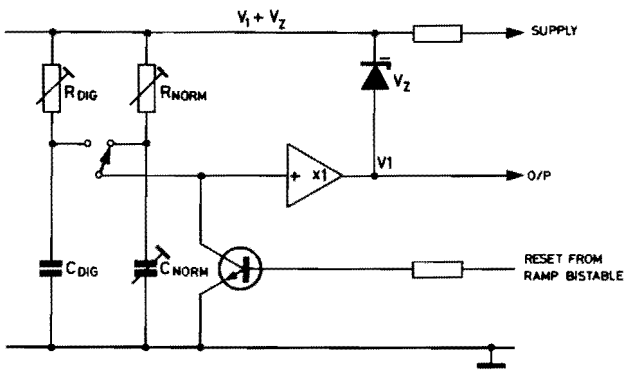


Fig. 4.16 Chop Blanking Waveforms

level control. This signal is passed to the slope selection switch which provides the option of inverting the signal to provide triggering on the reverse slope. The Schmitt trigger produces a signal of fixed amplitude and fast edges as the triggering signal.

The Refresh bistable provides the signal indicating that the oscilloscope is triggered and may be set, as shown by the Schmitt trigger output. The bright-line circuit detects an interruption in trigger signals and after a short period of approximately 250ms, produces a d.c. (continuous) trigger to the Refresh bistable. The NORMAL mode hold-off circuit disables trigger at the end of each sweep to allow the ramp to reset fully. It will over-ride both bright-line and trigger. The reset/hold-off bistable resets the Refresh bistable and hold keeps it reset when required in the digital modes.

The ramp generator is of the bootstrap form shown below. The buffer amplifier and zener diode produce a constant voltage of VZ across the chosen R and thus a constant current through it to charge capacitor C linearly. The transistor used to reset the ramp is driven by the RAMP BISTABLE ($\overline{RBQ}$). In NORMAL Mode, both R_{NORM} & C_{NORM} are switched by the timebase switch. In the digital modes, C_{DIG} is fixed and R_{DIG} switched to produce the three sweep rates required (controlled by PTL & QTL).



4.6.2 TRIGGER CIRCUIT (Fig. 5.16)

The line, CH1, CH2 and Ext. trigger signals, appear on R912, 913, 914 & 915 respectively. R59 mounted on the transformer and connected to the low voltage winding, forms one arm of a potential divider with R912, resulting in a ±50mV line frequency waveform appearing on R912, R913 and R914 are the collector loads of each TR309,

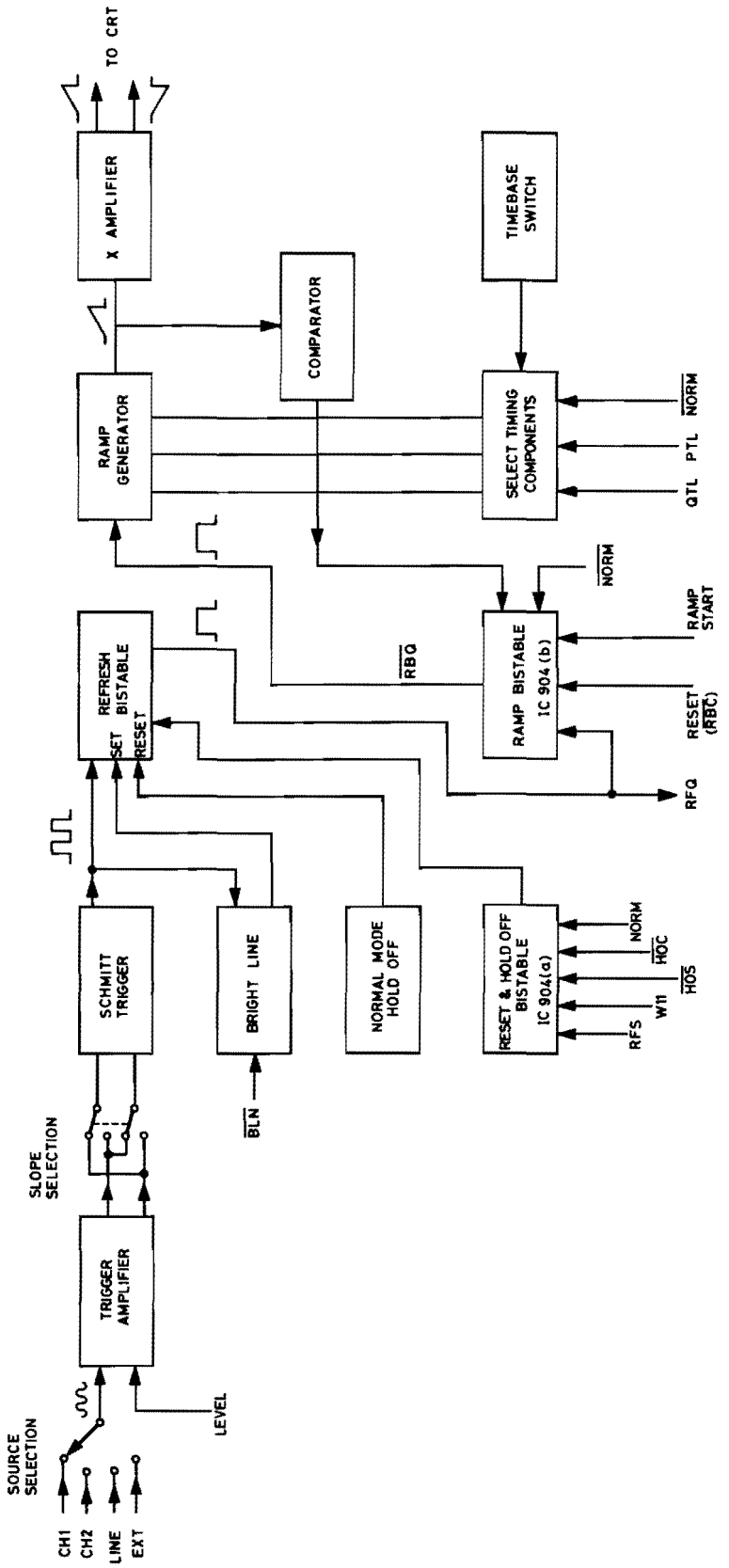


Fig. 4.17 Block Diagram of Trigger/Timebase

in CH1 and CH2 preamplifiers. One centimeter of Y deflection results in a signal of approximately 25mV on these loads. R90 and R915 form an approximately 200:1 attenuator to external trigger signals. R1010, R1011, and R1008, R1009 are adjusted to take the collector currents which flow in the CH1, CH2 trigger leads, thus maintaining the voltage across R913 and R914 near zero in the absence of Y signals. One of these signals, selected by S900aR, the trigger source and slope switch, is passed to S901, the trigger coupling switch, and from there to the base of TR914. There are four possible signal paths, a.c. coupled via C907, H.F. rej. via C907 and R916 with C909 by-passing h.f. signals to ground. (fco ≙ 15kHz), LF, rej. via C908 with R917 bypassing l.f. signals to ground (fco ≙ 15kHz) or d.c. coupling.

TR914, acting as an emitter follower, passes the trigger signal to the amplifier pair, TR915 and TR916, the potential derived from the level control R7 being passed via emitter follower, TR917, to the base of TR916. Thus the amplified trigger signal appearing between the collectors of TR915 and TR916 contains a d.c. component determined by the setting of R7. The gain of this amplifier is determined by R919, 925, 920 and is approximately 4X. The signal is passed via S900bR to the input of amplifier, TR901/TR902. If CH1, CH2 or EXT are selected the collectors of TR915 and 916 are connected to the bases of TR901/902 for positive slope, and TR902/901 for negative slope. If line trigger is selected, the slope switching is reversed since the line trigger signal is antiphase to the a.c. supply. TR901/902 form a differential amplifier whose output on the collector of TR902, drives the Schmitt trigger circuit TR903/TR904. The gain of amplifier TR901/902 is approximately 20 and the output d.c. voltage is adjusted with the common emitter resistor, R1012.

The function of the trigger circuit, TR903/904 is to generate a fast negative edge at the collector of TR904, independent of the rate of change of the applied signal. The signal appearing on the collector load of TR903/R932, is coupled via the network, R933, C902 and R935 to the base of TR904, whose emitter is connected to the emitter of TR908 and to the emitter resistor, R934. The emitter coupling introduces positive feedback which results in latching action as follows:-

When the base of TR903 is at a low voltage, TR908 is off, its collector potential is high, therefore the base potential of TR904 is high, turning on TR904. The emitter potential of TR904 is now higher than the base potential of TR903. When the base of TR903 goes more positive than the emitter of TR904, TR903 starts to take some of the emitter current of TR904, causing a reduction in its collector voltage which is communicated to the base of TR904, thus causing a further reduction in the current flowing. This effect is regenerative finally leaving TR903 on and TR904 off. The base potential of TR904 is now below that of TR903. As R932 is small, the change in base potential of TR904 is small (≙600mV between these two conditions) so that an a.c. signal of greater amplitude than this applied to the base of TR903 (if its d.c. level is adjusted) will cause the circuit to alternate in state. Thus the output of the circuit for any input above a minimum will consist of a series of equal amplitude pulses. C903 is a speed-up capacitor used to reduce the fall times of the output waveform.

4.6.3 BRIGHT-LINE AND TRIGGER INDICATOR (Fig. 5.16)

The waveform appearing at the output of the Schmitt circuit is coupled via R937/C904 to the detector circuit, D901, TR905 and C906. Positive going transitions on the Schmitt output result on C904 charging up D901. Negative transitions result in the base of TR905 being driven negative, and C906 is charged negative by the emitter current of TR905. If no more negative inputs are applied, C906 charges slowly positive through R939, until the base-emitter junction of TR906 is forward biased. TR906 is then turned on and pulls the base of TR909 negative via R948, turning off TR909, and switching of the l.e.d., D916. If a trigger signal amplitude or level is altered such that the Scmitt trigger generates pulses again, C906 will be charged negative, TR906 is turned off and TR909 is turned on causing D916 to be lit. TR906 also controls the emitter current of TR911 via D903. The base biasing network, R950/R949, of TR911 is controlled by the $\overline{\text{BLN}}$ line via TR910. When $\overline{\text{BLN}}$ is low, TR910 is on, and the base voltage of TR911 is approximately 4V positive with respect to the emitter of TR906, hence when TR906 turns on and saturates, current will flow in TR911 and its load R970, such that TR911 will saturate. Its base voltage under these conditions is approximately 1.5V w.r.t. the emitter of TR906. When $\overline{\text{BLN}}$ is high, TR910 is off and the base voltage of TR911 is equal to the emitter voltage of TR906, therefore no current will flow in TR911 when TR906 is turned on. TR910 can be held off by S7 ("Pull for bright line off" on front panel). The current drawn by TR911 through R970 acts as a d.c. trigger on the timebase bistable in the absence of Schmitt trigger pulses and is only allowed when S7 is open.

In REFRESHED and ROLL modes, auto-trigger is created by manipulation of the $\overline{\text{BLN}}$ signal. During the write process, WO, clocking the retriggerable monostable U647, causes $\overline{\text{BLN}}$ to stay HI turning off TR911. Should writing (and hence WO) stop for more than 200msec, the monostable will time-out and $\overline{\text{BLN}}$ will go LO. Under these circumstances TR906 would already be on (as its time constant is shorter) and thus $\overline{\text{BLN}}$ going low will turn on TR911 to the effect previously described. This may also be disabled by S7.

4.6.4 REFRESH BISTABLE (Fig. 5.16)

The refresh bistable consists of TR912 and TR913, cross coupled via R951 and R955 with C915 and C916 as speed-up capacitors and R953 and R954 as collector loads. The collector forTR913 drives the inverter, TR908, via network, R952. C914, R947 and D900, with the load resistor of TR908, R944 connected to the +5V logic supply line. Thus the output at the collector of TR908 is

in phase with the collector of TR912 and is a T.T.L. compatible signal designated in the logic RFQ diagram. A T.T.L. signal on R946 will control the state of TR907 via network, R946/R945. The collector load of TR907 is connected to the base of TR912, hence a low on R946 will cause TR907 to turn on and therefore the timebase bistable TR912 and TR113 will be reset into the condition of TR912 on, TR913 off. The driven end of reset R940 is designated as the input of the refresh bistable on the logic diagram. This bistable can be set (Q output high) by the occurrence of a negative edge at the output of the Schmitt trigger (collector TR904) via C905, and D904 allows the negative pulse to pass if the junction of R938/R963 is near ground potential. If the junction of these resistors is at approximately +5.5V, D904 is reverse biased sufficiently to prevent (hold-off) the trigger pulses from reaching the bistable input. (See section 4.6.8 on Hold-Off). The bistable can also be set (Q output high) by the d.c. trigger current from the bright line circuit via R970. (See section 4.6.3 on Bright Line). This current is also blocked by the hold-off voltage while junction R938/R963 is high.

4.6.5 RAMP GENERATOR (Fig. 5.16)

With reference to schematic in section 4.6.1 the buffer amplifier consists of emitter followers TR921, TR922 & TR923. Zener D905 provides the constant voltage. R_{NORM} is selected from R93- R98 and C_{NORM} is selected from C93, C94 and C95/C96. TR920 resets the ramp. Similarly C930 is C_{DIG} and R_{DIG} is provided by switching in R1031+R1032 and R1033+R1034. The selection of NORMAL or DIGITAL components is provided by TR928 & TR929. The junction of D909 & D910 is driven to be 0.6V(Vbe) below the voltage of the sources of the F.E.T.'s. In the NORMAL mode, the base of TR931 will be higher than that of TR930 and the former will this be on, pulling the gate of TR929 negative with respect to its source and thus turning it off. As TR930 is off, its collector rises until caught by D909, setting the gate voltage equal to the source voltage to minimise the channel resistance of the f.e.t.

When the digital mode components are selected, TR929 will be on, bringing the sources of TR937 and 938 to the same potential as that of TR929. In a simlair manner to that described, either (or both) if TR937 and TR938 may be turned on with zero volts Vgs when its driving transistor is off. Fig. 4.18 shows the selection of resistors and consequent ramp period. As the read counter changes at 1 sample per microsecond, these ramps produce calibrated displays of 400, 100 & 80 samples per cm. When the DISPLAY SELECT switch selects FULL STORE, the signal $\overline{ALL}$ goes LO, turning off U642a and setting QTL HI, the $\overline{ALL}$ signal drives PTL HI. Information as to whether X4 or X5 is required, is obtained by OR'ing together the ÷2½ and ÷5 signals from the timebase switch. This is applied to U629a & b for latching. The two latches enable different expansion on even and odd display sweeps when required. If HOLD ALTERNATE SAMPLES is pressed, the clock to U629(a) stops, latching the expand information. When the write chain is stopped, the clock to both latches stops.

P	Q	Transistor switched on	Resistor(s) selected	Ramp Rate
0	0	NOT AVAILABLE		
0	1	TR938	R1033+R1034	400μs/cm
1	0	TR937	R1031+R1032	100μs/cm
1	1	BOTH	PARALLEL COMBINATION	80μs/cm

Fig. 4.18 Ramp Rate Selection

If HOLD ALTERNATE SAMPLES is not pressed, both latches produce the same output. Selector U626 routes the required signal through to U642 according to the state of the modified least significant read address bit.

4.6.6 X OUTPUT AMPLIFIER (Fig. 5.16)

TR924 and TR927 form a p.n.p. differential amplifier whose gain is controlled by the network, R987, R988, R6, R990 and R991. The base of TR924 is driven by the ramp generator and the base potential of TR927 is controlled by the X shift potentiometers, R8A and R8B. Preset controls, R988 and R990, are set so that as R6 is varied from maximum resistance to minimum, the gain is changed by 10 times. As the dynamic range of this amplifier is then only approximately 1.5V under these conditions, D913 and D914 are required to protect TR924 and TR927. The mixed sweep plus shift signal produced by this stage at its output loads, R983 and R998, drives the differential high voltage amplifier, TR925/TR926, whose collectors are connected via R985/R992 to the X plates of the c.r.t.

4.6.7 TIMEBASE SEQUENCE IN NORMAL MODE (Fig. 4.19)

In this mode, selector IC903(b) routes RFQ to the clock input of the Ramp Bistable IC904(b) and IC903(a) routes the $\overline{Q}$ of the Ramp Bistable to the clock of the Hold-Off bistable.

Assuming that the bright-line is disabled, a typical sequence starts with a negative edge from the Schmitt trigger. This sets RFQ HI which is turn clocks the Ramp Bistable setting RBQ HI. The latter turns off the clamp transistor TR920 and the ramp starts. The voltage on the base of TR919 rises until, at a point where the X deflection has reached approx 13cm, TR919 turns on and clears IC604. Positive feedback from C923 produces a stable reset even at slow ramp speeds. The ramp bistable turns on the clamp transistor and clocks IC904a. The latter drives the reset of the Refresh bistable. On the timing logic board, RFQ is gated through U635(b) and (a) to the clear the HOLD-OFF bistable thereby returning all logic signals to their starting state.

4.6.8 NORMAL MODE HOLD-OFF (Fig. 4.19)

In Normal Mode only, TR918 is turned on grounding one end of the hold-off timing capacitors. When RBQ goes

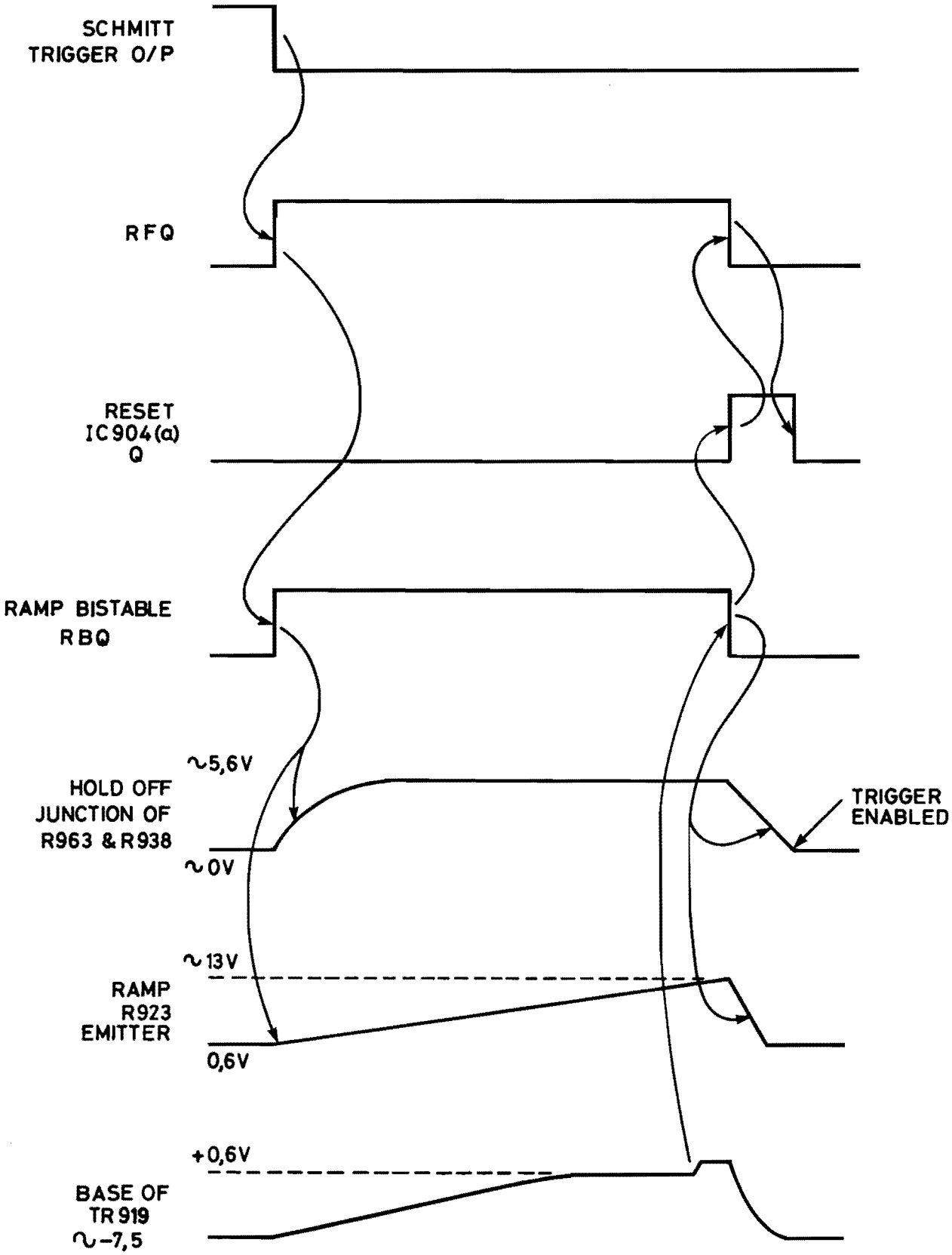


Fig. 4.19 Timebase Waveforms: Normal Mode

HI, IC901 pin 13 goes LO and IC901(a) turns off R962 then charges the hold-off capacitor through D902 heading for +20V until the voltage on the capacitor reaches 5.6V. At this point the diodes D912 and D911 turn on and clamp the voltage. This voltage, acting through R938 drives the junction of C905 and D904 positive, reverse biasing D904 and blocking trigger pulses. When RBQ goes LO, IC901 pin 1 goes LO turning on D912 which in turn drives the anode of D902 to approximately 0.8V, reverse biasing it. The hold-off capacitor then discharges through R963 heading for −20V. It is clamped when it reaches approximately 0.2V by D902. By this means, trigger pulses are prevented from starting another sweep until the ramp timing capacitor has been discharged completely.

4.6.9 DISPLAY IN DIGITAL MODES

In both digital modes, the trigger and ramp generator circuits are completely divorced and will be described separately.

The ramp start signal ($\overline{R}_2$) from the store board is routed by IC903(a) to the clock input of the Ramp bistable. The latter controls the start and stop of ramp as previously described. The $\overline{NORM}$ signal, being HI, selects the digital ramp timing components. As described in section 4.6.5, the read counter is a self-controlling loop. Each time R_2 goes LO, the Ramp Bistable is clocked. Once its Q has been driven HI, further clocks have no effect. When RBQ is driven HI, the ramp starts and continues until the RAMP bistable is cleared either by TR919 as previously described, or by Q710 on the store board.

4.6.10 OPERATION OF TRIGGER IN REFRESHED MODE

The RFs signal on IC903 pin 1 routes W11 to the clock of the HOLD-OFF bistable IC904(a). Pins 10 & 11 of IC903 are driven LO by NORM, disabling that half of the IC.

A typical write sweep (shown in Fig. 4.20) starts with RFQ being driven HI by a trigger signal. RFQ enables the write chain as previously described. The next point of interest is at the end of the write sweep when W11 goes LO. This clocks the Hold-Off Q HI which in turn drives RFQ LO. As in the NORMAL Mode, RFQ is coupled to the clear of the Hold-Off bistable and will clear the bistable returning all signals to their original state ready for the next trigger. Should the sweep have been a single sweep, $\overline{STO}$ will be driven LO by W11 (dotted traces). STO, acting through U610(b), U635 c & d drives the preset of the Hold-Off bistable LO, which drives the Q HI despite the LO on the clear input. This holds RFQ LO regardless of trigger signals. When STO goes LO again, the clear on the Hold-Off bistable becomes effective and the instrument is available for trigger.

When the instrument is in either of the digital modes, the analogue hold-off circuit is disabled and the hold-off capacitors discharge. This would render the instrument available for trigger the moment it is switched to NORMAL causing possible malfunction. However, monostable U647(b) is fired by switching to NORMAL. Its Q, acting through U635d presets the Hold-Off bistable, resetting RFQ and holding off trigger and allowing the ramp to reset fully. At the end of the monostable period, the Hold-Off bistable is cleared in the normal way.

4.6.11 OPERATION OF TRIGGER IN ROLL MODE

No signals are routed to the clock input of the Hold-Off bistable in ROLL mode. Trigger has no effect in ROLL mode, except in Single Sweep. Fig. 4.21 shows that the Hold-Off bistable is normally set by $\overline{HOS}$ holding RFQ LO regardless of trigger. $\overline{HOS}$ is set LO by RMD acting through U610c & b, U635c & d. $\overline{HOC}$ is held HI by RMD acting through U635a. As described in section 4.5.7 writing does take place under these conditions, which represent the basic ROLL mode. When the ARM button is pressed, RMD will at some later point go HI and, by the mechanism explained above, this causes $\overline{HOS}$ to go HI and $\overline{HOC}$ LO. This sets the Hold-Off Q LO rendering the instrument responsive to trigger. When trigger occurs RFQ goes HI. At a point defined by the roll control circuitry, $\overline{STO}$ goes LO, stopping the write process. This returns RMD to its original LO state causing Hold-Off Q to go HI which sets and holds RFQ LO.

The instrument will remain in this state until $\overline{STO}$ is driven HI either by pressing the release button, in which case the instrument returns to the basic roll mode, or by pressing ARM (dotted traces) to start another single sweep.

4.7 D/A CONVERTER AND DOT JOINER

The D/A converter is provided in a single integrated circuit, U701. The latched eight bit binary outputs from the store, D0 to D7, are applied to the input, pins 12 to 5, and determine the output current from pin 4 as a proportion of the input reference current to pin 14. The reference input is fed through R702 from the zener diode, D701. R701 provides fine adjustment of this current to set the full amplitude of the analogue output.

The output from the D/A converter is in the form of a step waveform which follows each successive change of digital input. The purpose of the subsequent dot joiner circuit is to convert this into a series of straight lines joining these successive levels.

As the D/A output level sttles to a new value, amplifier U702 detects its difference from the dot joiner output, and sets a voltage via sampling switch, Q702, on a storage capcitor, C712. This voltage is sufficient to drive the integrating amplifier, U703, to correct the error by the time the next sample is taken.

In more detail, the gain of U702 and of the complete system is defined by the input resistor, R705, the shunt feedback resistor, R712 and the voltage divider, R740,

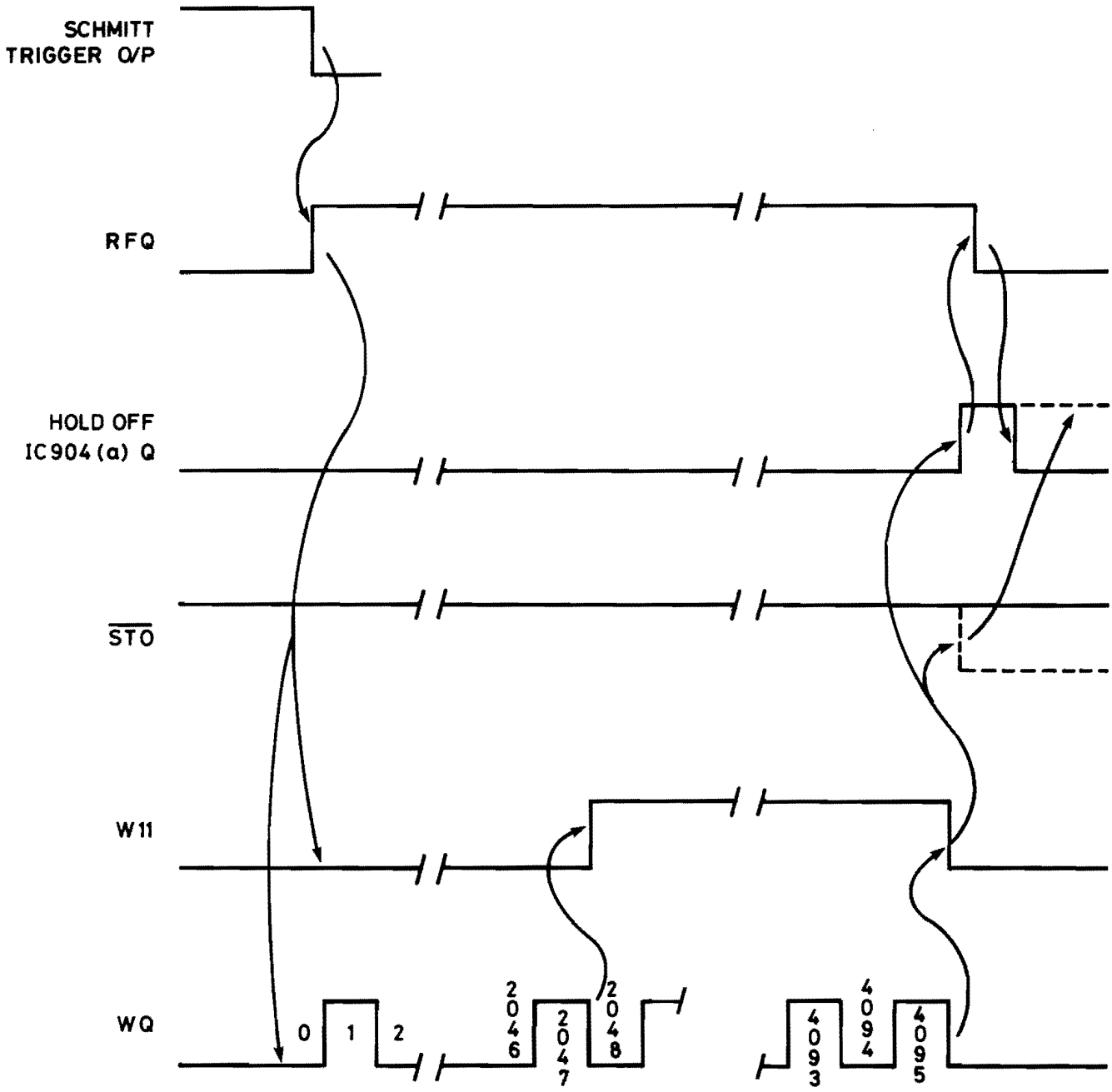


Fig. 4.20 Triggered Sweep Waveforms: Refreshed Mode

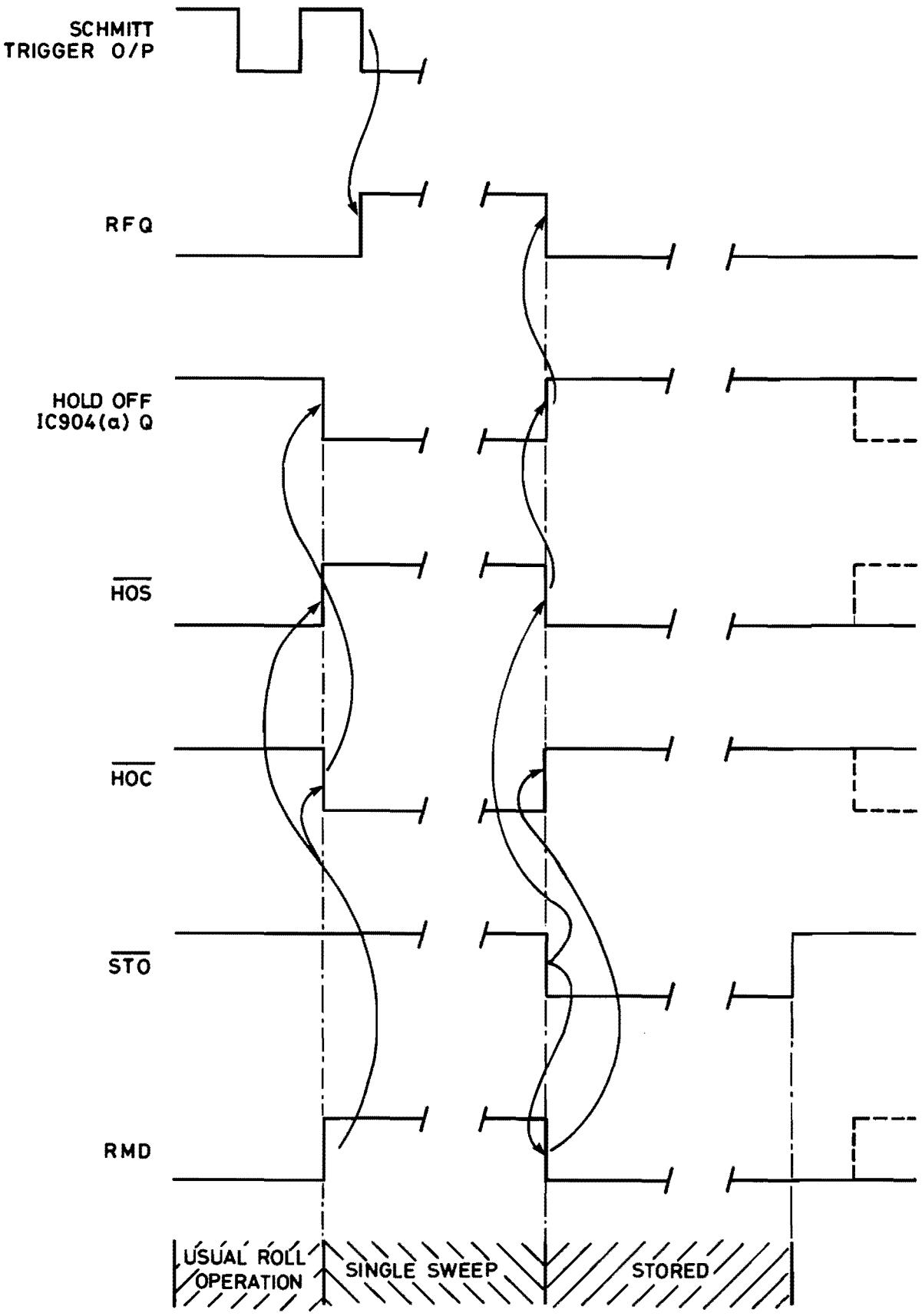


Fig. 4.21 Triggered Sweep Waveforms: Roll Mode

and R708. The preset potentiometer, R715 with R711, provides a zero setting control to centre the displayed waveform. The output of U702 is buffered by emitter follower, Q701, to drive the 'hold' capacitor C712 through the sample switch, Q702.

The data from the store is latched at the end of P5, and the D/A converter and U702 are allowed to settle before Q702 is switched on during a P4 pulse. These pulses are a.c. coupled by C711 into the base of the saturated switch, Q705. This transistor is normally conducting so that D704 holds the gate of Q702 near to −10V. Q702 is thus non conducting. During the P4 period the drive to C711 goes negative, Q705 is turned off and its collector rises toward +5V. The emitter follower, Q703, takes the gate of Q702 rapidly toward +5V until its collector-base junction clamps at 0V. In this condition Q702 conducts. At the end of the P4 period, Q705 is turned on and D704 returns the gate potential rapidly to −10V. Q706 and Q707 generate a similar but inverted drive waveform which is applied via C713 to C712 to compensate for the inherent gate to source capacitance of Q702 which injects an unwanted portion of the gate switching signal into the storage capacitor. The −10V line is defined by the zener diode, D707.

The integrator formed by U703, can be considered to operate in its simplest form when f.e.t. switch, Q708, is on. In this condition the rate of change of output voltage for a given input voltage is determined by the input resistor, R724, with R725 and the feedback capacitor, C719. The input voltage from C712 is buffered by the emitter follower, Q704. R725 is used to adjust the output slope so that the detected error is reduced to zero at the next P/4 sample period. If R725 is mis-set, the output will overshoot or undershoot in response to a step change of input but when set correctly the system will balance in one sample period.

The above condition applies in a single trace when every store location is displayed on a sweep. In dual trace mode, alternate locations are displayed on each sweep and thus the sample & hold pulse rate is halved. The integrator time constant is doubled to match this by turning off Q708 and thus doubling the input resistance to the integrator. U614 halves the sample & hold pulse rate by comparing the modified Ro with the unmodified Ro. This also displays odd and even location samples in their correct relative positions, i.e. even samples displaced to the left of odd ones.

4.8 CALIBRATOR (Fig. 5.16)

This consists of a current adjusted to 1mA applied to TR932 and TR933. Read address line R9 drives the base of TR932 at 976Hz causing the current from TR934 to be switched alternately between TR932 and TR933. Precision resistors R1020 (100Ω) and R1019 (900) produce the required voltages.

4.9 REMOTE FUNCTIONS (Figs. 5.13, 5.14)

When the remote activation signal $\overline{\text{REM}}$ is driven LO, signals REM3, REM4, REM5 & REM6 go passively HI. REM2 goes actively HI and REM1 goes LO. REM3–6 enable DISPLAY MODE, CHANNEL SELECT and END TRACE controls to be driven in WIRE-AND fashion from the external socket.

On the timebase board, $\overline{\text{REM}}$, driving on U725 pin 11 and U724 pin 11, disables the front panel HOLD and HOLD ALT. SAMPLES buttons.

REM 2 disables the front panel ARM button when HI. REM1 biases the ARM R-S flip-flop, U725, such that it may be driven by a single signal (external ARM) on pin 3.

In a similar manner when EXTERNAL CLOCK SELECT goes LO then U603a, b, c & d outputs go passively HI. SKL pins 7, 10, 5, 11 & 6 may then be driven externally. If they are not driven, the resultant HI level appearing on U602 pins 9, 10 & 11 selects the signal on pin 12 which is the external clock. The latter is then processed in the same way as the internal clock.

4.10 MNEMONICS

Whenever a mnemonic has a definable effect e.g. MCL, a HI level produces that effect. The inverse e.g. $\overline{\text{MCL}}$ indicates LO to produce the effect. Both forms do not necessarily exist. Where no definite effect is expected e.g. CK, an arbitrary sense is chosen but, for example, $\overline{\text{CK}}$ is still the inverse of CK.

ALL	Display ALL 4k Bytes (DISPLAY expansion)
ARM	Signal from ARM push-button
ARQ	Latched version of above
BEN	Enable data buffer from OS4020 to 4022
BLN	Auto-trigger drive to bright-line circuit
CK	Master 10MHz clock
DHO	Display Ramp Hold-off
DTH	Dual trace or half hold
END	Terminates single sweep
FLASH	0.5Hz signal to flash LED's
HHD	Hold Alternate samples
HLD	Hold display
HOC HOS	set & clear inputs of digital trigger hold-of bistable
LDO	Latch data from store output
MCL	Master Clear on Power-on, Release or Normal Mode
NORM	Normal Mode
P1–P5	Five phases of 2MHz clock
PON	Power-on reset

PTO, PT1	Trigger point selection lines
PTL, QTL	Select ramp rate
R0–R11	Read counter address lines
RAS	Read Address Strobe 2MHz
RBC	Ramp Bistable Clear
RBQ	Ramp Bistable Q
RC0–RC11	Roll counter output lines
RCK	Read counter clock
REF(RFS)	Refreshed Mode
REM	Relinquish control to remote
RFQ	Refresh bistable Q
RMD	Armed to accept trigger
ROLL	Roll Mode
SRO	Start Read-out (4022)
STA	Store Access to 4022
STO	Stored (at end of single sweep)
SWA	Select Write Address
TRG	Triggered (single sweep)
W0–W11	Write counter address lines
WCC	Write Counter Clear
WCK	Write Counter Clock
WE	Write enable of stores
WEN	Enable write (from 4022)
WGP	Write gating pulse
WGP'	Delayed WGP
WLC	Write latch clear
WRC	Write rate clock (continuous)

4022 Option Mnemonics

A0 – A11	Plot Address Lines
AUT	Auto Plot Mode Selected
CNT	Continuous Mode selected
CPR	Clear (terminate) Plot & Reset Address counter
HSQ	Retimed Handshake signal
PRC	Plot Rate Clock (Continuous)
SAD	Store Address Disable – defeats STA
SPL	Start Plot via digital I/O
STA	Disable write chain & give store access to 4022 Option

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U616		4.5.5
U617		4.5.5
U618		4.5.5
U619		4.5.5
U620a		4.5.9
U622		4.5.9
U623		4.5.7
U626		4.5.12
		4.6.5
U629		4.6.5
U631a		4.5.5
U633a, d		4.5.12
U634		4.5.9
		4.5.10
U640		4.5.10
U641a		4.5.5
U642		4.5.5
U643		4.5.11
U644a, b		4.5.11
" c, d		4.5.10
U645a		4.5.12
" b		4.5.9
U646		4.5.10
U647		4.6.3
		4.6.10
U701		4.7
U702		4.7
U703		4.7
U704		4.5.6
U717		4.5.6
U718		4.5.6
U719		4.5.6
U720		4.5.7
U721		4.5.7
U726		4.5.6
U727		4.5.6
U728		4.5.6
U729		4.5.6
U730		4.5.6
U731		4.5.6
U732		4.5.6
U733		4.5.6
U734		4.5.6
U735		4.5.6
U736		4.5.6

4.11 4022 OPTION SYSTEM DESCRIPTION

4.11.1 GENERAL

ANALOGUE OUTPUT SECTION

The 4022 gains access to the oscilloscope store at the expense of the write chain but without disturbing the read sequence previously described.

The plot is controlled by a range divider as in the write chain of the oscilloscope. At a rate thus defined, data is read from the store and latched for presentation to a D to A converter. In dual trace mode the data is latched in

the appropriate channel as indicated by the least significant address bit. In single trace mode, both channels latch all data. The address counter is incremented immediately after the data has been latched. The address counter also drives a 12 bit D to A converter to produce the X-ramp output.

When the 4022 is operating in MANUAL mode, the plot is started manually and terminates when the address counter overanges. In AUTO mode the plot terminates similarly but at the same time ARMing the oscilloscope. The next "STORED" signal provides a START PLOT signal.

DIGITAL I/O SECTION (See Fig. 4.23)

The internal portion consists of three bidirectional busses connecting with the oscilloscope. One handling store data, the other two handling oscilloscope control. These three busses are connected to the single external bus via 3-state devices, the selection of the source/destination controlled by signals MUX1, MUX2, $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ under handshake control. The Group 1 and Group 2 lines are WIRE-OR'D to open collector devices within the oscilloscope, with $\overline{\text{XREM}}$ specifying the source of control. When $\overline{\text{XREM}}$ is HI both GROUP latches are switched to their high Z state giving control to the oscilloscope. When $\overline{\text{XREM}}$ is LO, the oscilloscope open collector devices are turned off and the GROUP latches are enabled. Control information previously stored in these latches will then be used. The associated group buffers enable the external device to read the current state of the control lines (regardless of control source). The signals $\overline{\text{ARM}}$, $\overline{\text{CPR}}$ and $\overline{\text{SPL}}$ are not latched. A LO written into any of these locations will cause the relevant line to go LO for 0.5μsec before returning HI, eliminating the need to program a LO then a HI. When Group 2 is read, the most significant four lines (corresponding to these signals) are not driven.

When GROUP 1 or GROUP 2 is read, the data lines will stabilise shortly after the setting of MUX1, MUX2 and $\overline{\text{READ}}$ without action of the HSM line. The handshake has no effect. (It would probably be used for reasons of consistency). Store access is obtained in the multiplex time slot used by the analogue output as previously described. The handshake control is timed around this. The handshake is substituted for A0 within the address counter, providing the auto double increment while MUX2 is substituted for A0 sent to the store, thus defining odd/even.

When the 4022 is set up to read data from the store, the store input multiplexer selects ADC data, but the write chain is disabled. The 3-state buffer at the store output is enabled and sends data from the oscilloscope to the latch in the 4022. This latch is clocked continually capturing the same data repeatedly until the address is changed.

A typical read sequence starts with the address counter at zero (or one if MUX2 = 1). When MUX1, MUX2 and $\overline{\text{READ}}$ are set-up, valid data from location zero (one) appears on the bus. When the HSM is driven HI, the address counter double increments and data from address 2 (3) is latched with READY indicating valid data. This may then be repeated. When the 4022 is set up to write data into the store, the store output buffer is driven into its High 2 state and the store input multiplexer is switched to the 4022. Data from the external socket passes through buffer, multiplexer and is held in the data in latch. A write sequence starts with address counter as above, and valid data presented at the external socket. When HSM us driven HI, the store input latch is clocked and then WEN drives the write control to allow one write pulse through to the store. The address counter then (double) increments. The timing of HSM and READY ensure that the store data/address set-up and hold times are observed.

4.11.2 PLOT TIMEBASE (Fig. 5.19)

The range dividers are identical in function to those in the main instrument. The RAS input is buffered by U838(d) and drives U813(a) which produces ÷2½ and ÷5 outputs. U823(a) selects ÷1, ÷2½ or ÷5 and U813(b), U812 & U811 provide further decades of division. The required decade is selected by U840 (see Fig. 4.25). U821a & b retime the signal and produce a pulse one RAS period wide as the plot PRC clock (PRC).

4.11.3 PLOT ADDRESS (X) COUNTER (Fig. 5.19)

This is a 12 bit-ripple through counter with A9–A11 produced by U814 and A1–A8 by U816. A0 is provided by U822(a). The clock input to the counter is continuous but the counter is stopped (and reset) by applying a clear.

4.11.4 X–D.A.C. (Fig. 5.19)

U805 converts the 12 bit address into an output voltage with +10V corresponding to all inputs LO and –10V corresponding to all inputs HI. U839 inverts and shifts this signal such that all address lines LO produces 0V at the output of U839 and all HI produces 1V. R839 provides adjustment of shift and R840 adjusts the gain.

4.11.5 Y–CHANNEL LATCHES AND D.A.C.'s (Fig. 5.19)

The two channels are identical and so only CH2 will be described. Data from the instrument store is latched (as described later) to produce a steady input to the DAC. $\overline{D}_7$ is inverted after latching as in the main instrument so that clearing the latch produces a half-full scale signal. The DAC, U 819 produces a (negative) current output which is porportional to the digital input and the reference current driven into a virtual earth; pin 14. Amplifier U830 turns this current into an output voltage. As the DAC current is unipolar, a half scale offset current is injected through R824 (adjusted by R816) to make it bipolar. The scaling is adjusted by R817 changing the voltage at the wiper of R816. Note that this has the same effect on both the reference and offset currents, and thus produces no change in offset.

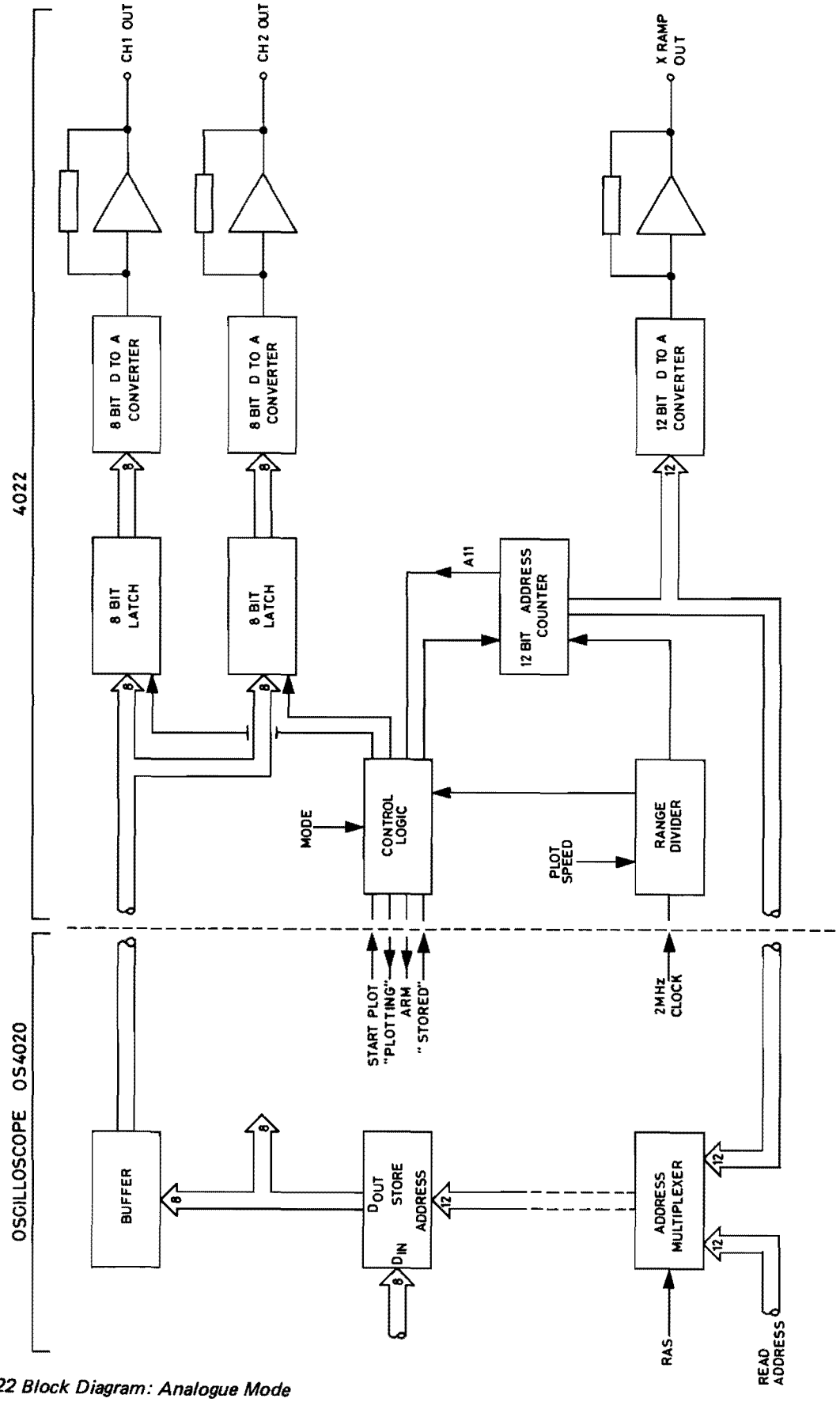


Fig. 4.22 4022 Block Diagram: Analogue Mode

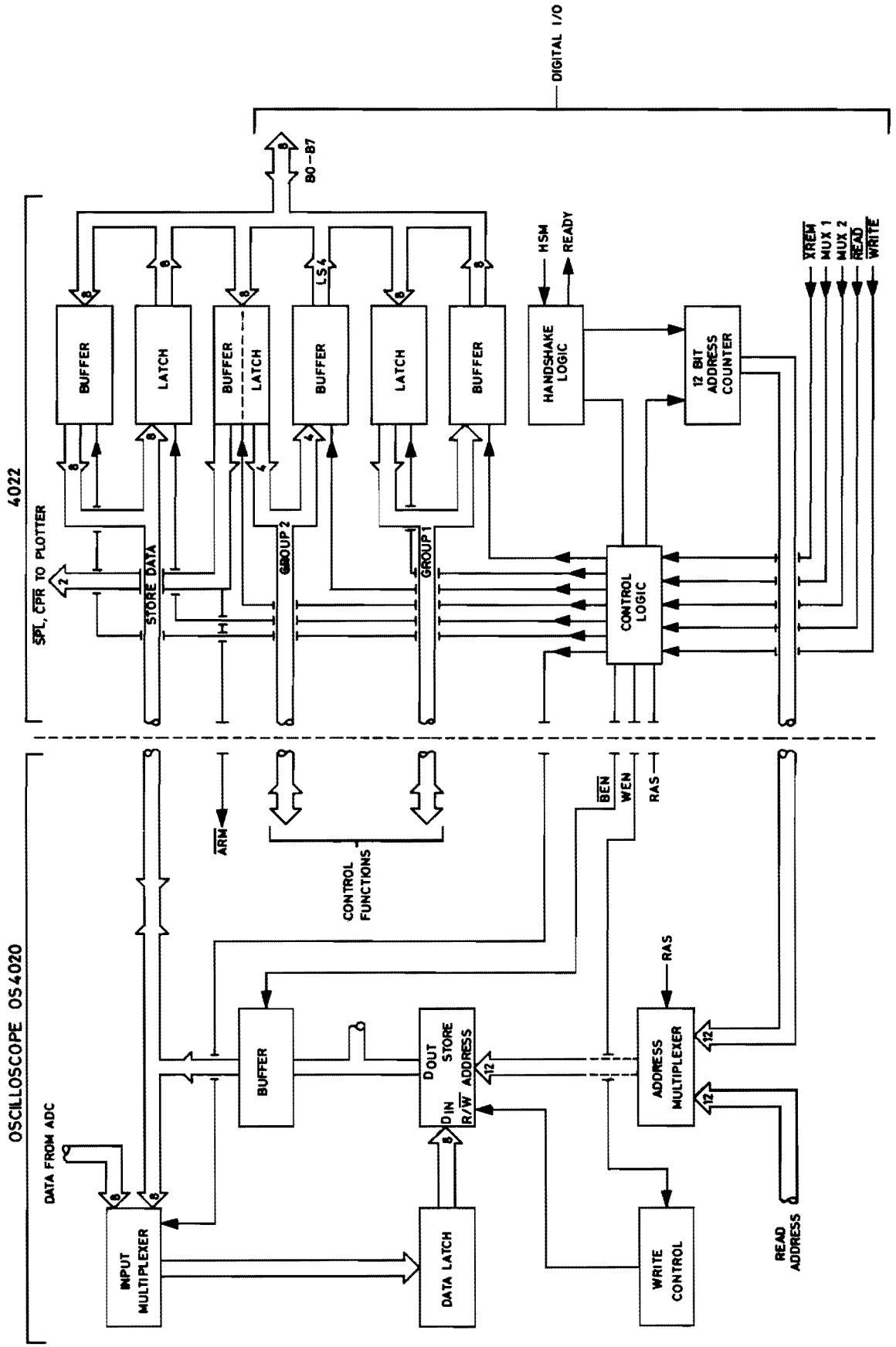


Fig. 4.23 4022 Block Diagram: Digital Mode

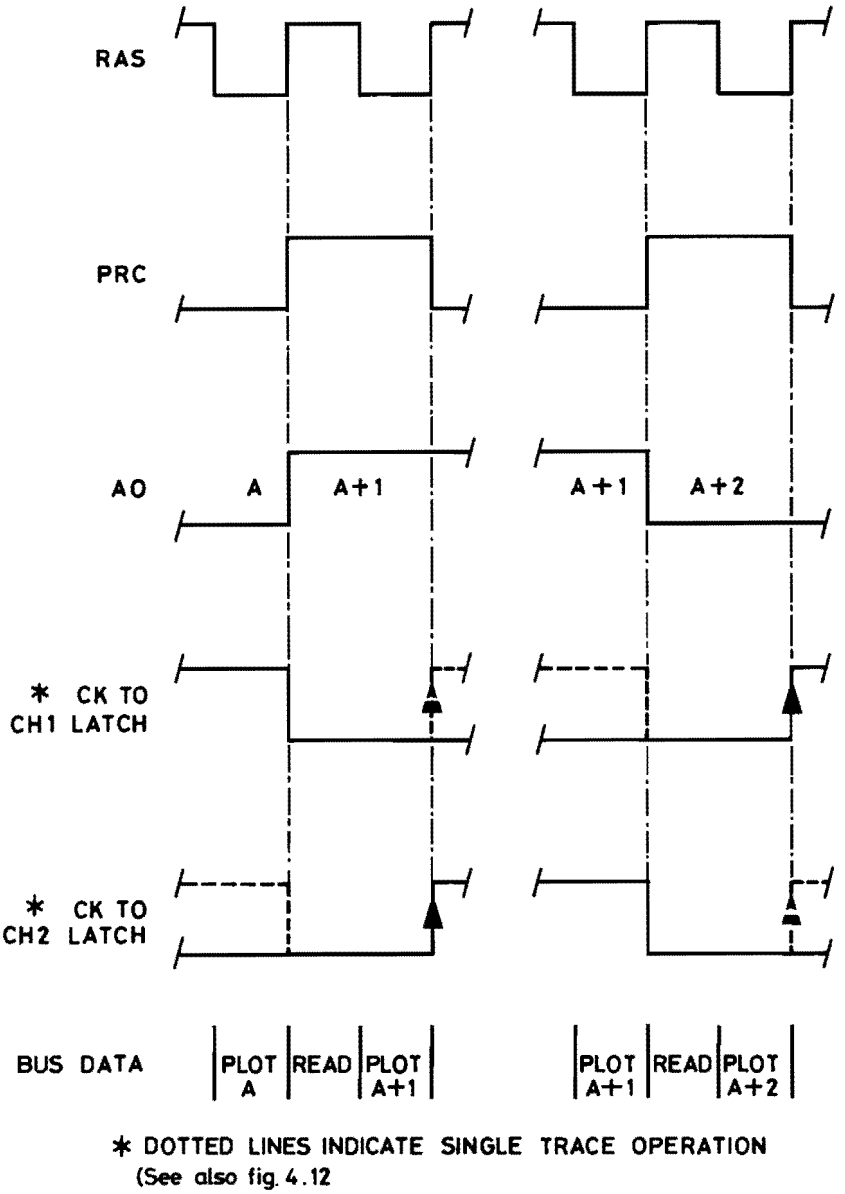


Fig. 4.24 Plot Timing Signals

U804 provides the control of clocks to the latches. When the instrument is in single trace mode, $\overline{DTH}$ is HI, producing a LO at pins 2 & 8 allowing PRC to pass through to both channel latches simultaneously (see Fig. 4.24). In dual trace mode, the latches are clocked alternately as defined by A0. As shown in Fig. 4.24 data from even locations is latched into CH1 and that from odd locations into CH2 as in the main instrument.

4.11.6 PLOT OPERATION: MANUAL MODE

When the front panel PLOT button is pressed, SRO goes LO, which acting through IC833 fires monostable U835(a). The LO level on its $\overline{Q}$ output drives RSQ HI (all other inputs to the R–S bistable are HI) with the following actions:-

a) The clear is removed from U837(a) and the preset from (b)
b) Acting through U836c it turns on Q800 energising relay on RL800
c) Acting through U824b, and U834a & b it drives $\overline{STA}$ LO changing the store multiplexing from READ-WRITE to READ-PLOT (see section 4.5.6) giving the plotter access to the store address bus. When U835(a) times out, the positived edge on $\overline{Q}$ clocks U837a Q HI, which, acting through U825c removes the clear from the address counter.

When the count reaches four, the positive edge clocks U837(b) driving its Q LO. This sets the READOUT MARKER HI while the $\overline{Q}$ going HI takes the clear off the data latches.

The plot continues until the counter overflows to zero, whereupon the negative edge on A11 fires monostable U835(b). The negative edge on the $\overline{Q}$ of the latter drives RDO LO. RDO clears U837(a) which in turn puts a clear on the counter. RDO also presets U837(b) which in turn sets the READOUT MARKER LO and puts a clear on the data latches ending the plot.

4.11.7 PLOT OPERATION: CONTINUOUS MODE

In this mode, $\overline{CNT}$ is LO and U831 pin 3 is LO and thus the clear of U822 is HI. The plot is started as in the manual mode but when U835(a) times out, U822(b) is clocked, driving its $\overline{Q}$ LO. The latter clamps RDO HI. U835(b) is thus unable to terminate the plot. If the PLOT button is pressed again, U822(b), when clocked, will toggle setting its $\overline{Q}$ HI, freeing RDO to be driven LO at the end of the next full count.

4.11.8 PLOT OPERATION: AUTO MODE

In this mode, $\overline{AUT}$ is LO enabling U832(c) and (d). Assume that a plot has been started by the PLOT button. When U835(b) $\overline{Q}$ goes HI at the end of the plot, it acts through U832(c) and U838(b) to drive $\overline{XARM}$ LO, ARMing the oscilloscope. The plot then terminates.

Eventually the $\overline{STO}$ signal goes LO indicating that the oscilloscope has captured a store-full of new data. $\overline{STO}$, acting through U832 d & a will drive U833 pin 12 HI starting another plot. This cycle repeats indefinitely.

4.11.9 WRITE RATE RAMP (Fig. 5.19)

The write rate ramp is enabled by driving $\overline{SAD}$ LO. This enables $\overline{RFQ}$, acting through U838a and U825c to remove the clear from the address counter at the instant the write address counter in the oscilloscope is enabled. The plot clock, having been connected to the write rate clock of the oscilloscope, ensures that the address counter stays in synch. with the write counter. The $\overline{SAD}$ input on U834 pins 4 & 5 clamps $\overline{STA}$ HI ($\overline{STA}$ LO would disable the write chain).

4.11.10 HANDSHAKE CONTROL (Fig. 5.19)

The handshake input, $\overline{HSM}$, is buffered, inverted, and applied to U828(a) clock. U828a & b are connected identically to the clock retiming circuit U821a & b and will produce an 0.5μs wide pulse from a handshake input. If U828a and U821a are presented with the same input (as is the case of Data I/O) they will produce synchronous outputs.

4.11.11 DE-MULTIPLEXER (Fig. 5.19)

The inputs $\overline{READ}$, $\overline{WRITE}$, MUX1 & MUX2 are buffered by U827(a) and applied to U815. Setting $\overline{READ}$ LO enables the 1Y outputs of U815 such that each combination of MUX1 & MUX2 drives one output (only) LO e.g. MUX1 = MUX 2 = 1 drives 1Y3 (pin 4) LO. If $\overline{READ}$ is HI, all four outputs are HI. Setting $\overline{WRITE}$ LO is one enable on the 2Y outputs, however, $\overline{HSQ}$ must also be LO, providing the strobe. Unless both are LO, all outputs are HI.

4.11.12 GROUP 1 I/O (Fig. 5.19)

As previously indicated, if $\overline{READ}$ = 1, MUX1 = 1, MUX2 = 0 then U815 pin 5 is driven LO, enabling three-state buffers U801, which couple the current Group 1 signals directly onto the B0–B7 lines. If $\overline{WRITE}$ is driven LO instead, a handshake input will cause U801 pin 11, and thence U802 clock to pulse LO. The rising edge of this signal causes the current signals on B0–B7 to be latched. Thereafter, U802 will be insensitive to changes on the bus lines. The output enable of U802 has no effect upon this latching action (see also section 4.11.7).

4.11.13 GROUP 2 I/O (Fig. 5.19)

The four least significant bus lines operate as in Group 1, being latched by U803 and coupled onto B0–B3 by U817(a). The three most significant lines are write-only and are handled by U817(b). The enable of the latter will normally be HI forcing the outputs into High–Z mode. The pull-up resistors ensure that $\overline{CPR}$, $\overline{SPL}$, & $\overline{ARM}$ are normally HI. When a handshake causes U817(b) enable to be pulsed LO, B4–B6 are coupled through and a LO on any input will cause the output to pulse LO. This action eliminates the need to reset any of these signals.

4.11.14 DATA I/O (Fig. 5.19)

The data I/O mode is entered when MUX1 is driven LO. This has the following immediate effects:-

a) $\overline{STA}$ is driven LO (unless $\overline{SAD}$ is LO) giving address access to the store and connecting the plotter/oscilloscope lines. D_0–D_7 to the store input.
b) U825(a) will turn off buffer U715 in the main instrument if $\overline{READ}$ is HI, & via selector U841.
c) MUX2 replaces A0 to the store giving specific channel access;
d) HSM replaces the plot clock.
e) The retimed HSM replaces A0 in the counter chain.

4.11.15 DATA I/O – READ (Fig. 5.19)

The sequence of events is shown in Fig. 4.26. The output of data latch U806 is enabled by $\overline{READ}$ = 0 & MUX1 = 0 independently of MUX2 and handshake. The latch is clocked at the end of every plot period by RAS. The handshake input is returned to RAS by U837a & b producing a positive pulse identical to HSQ from U828b. The trailing edge of this pulse increments the address counter during the READ period when the plot address is not being used and the next positive edge on RAS latches valid data from the next-but-one store location.

Plot Rate		Division	W16	W17	W18	W19	W20	W21	W22	U840 pin 9	U840 pin 10	U840 pin 11
1	ms/cm	5	0	1	1	1	1	1	1	0	0	0
2	ms/cm	10	0	0	0	1	1	1	1	0	0	1
5	ms/cm	25	1	0	0	1	1	1	1	0	0	1
10	ms/cm	50	0	1	0	1	1	1	1	0	0	1
20	ms/cm	100	0	0	1	0	1	1	1	0	1	0
50	ms/cm	250	1	0	1	0	1	1	1	0	1	0
.1	sec/cm	500	0	1	1	0	1	1	1	0	1	0
.2	sec/cm	1,000	0	0	1	1	0	1	1	0	1	1
.5	sec/cm	2,500	1	0	1	1	0	1	1	0	1	1
1	sec/cm	5,000	0	1	1	1	0	1	1	0	1	1
2	sec/cm	10,000	0	0	1	1	1	0	1	1	0	0
5	sec/cm	25,000	1	0	1	1	1	0	1	1	0	0
10	sec/cm	50,000	0	1	1	1	1	0	1	1	0	0
20	sec/cm	100,000	0	0	1	1	1	1	0	1	0	1
50	sec/cm	250,000	1	0	1	1	1	1	0	1	0	1
100	sec/cm	500,000	0	1	1	1	1	1	0	1	0	1
EXTERNAL		–	X	X	X	X	X	X	X	1	1	0
HANDSHAKE		–	X	X	X	X	X	X	X	1	1	1

Fig. 4.25 Plot Rate Selection

4.11.16 DATA I/O – WRITE (Fig. 5.19, see also Fig. 4.27)
U715 on the main instrument store board is turned off to allow data to be sent to the instrument by buffer U807. The latter is turned on when $\overline{HSQ}$ goes LO.

When $\overline{WRITE}$ is LO and MUX1 is LO, a pulse on $\overline{HSQ}$ is gated through U825 to WEN. The latter, acting on U623 pin 11 on the main instrument timing logic board gates through one write timing pulse to the store $\overline{WE}$ causing the data on B0–B7 to be written into store. At the end of the plot period the address counter is incremented.

4.11.17 REMOTE/LOCAL (Fig. 5.19)
The remote signal $\overline{XREM}$ is buffered by U827 and applied to the D inputs of U826a & b. The latter are cross-coupled so that both Q outputs cannot be LO simultaneously. This would cause signal line contention between the option and the main instrument.

When $\overline{XREM}$ is HI, both Q's are HI and thus $\overline{REM}$ sent to the main instrument gives it local control and U826 pin 5 drives U802 and U803 into the HI–Z state. U826 pin 6 is LO enabling the PLOT MODE S2 to select AUTO & CONTINUOUS. When $\overline{XREM}$ goes LO, U826(b) is unable to change as it is preset by U826(a) $\overline{Q}$. U826(a) $\overline{Q}$ is free, to be clocked HI by RAS. This sets $\overline{REM}$ LO driving the main instrument into remote. The next positive edge of RAS clocks U826 pin 5 LO turning on U802 & U803 which then provide the remote controlling signals. U826 pin 6 is now HI, forcing the PLOT MODE to MANUAL regardless of setting. U831c and U836b provide control of the main instrument timebase selection such that it may be driven remote either by selecting external clock or by $\overline{XREM}$. When $\overline{XREM}$ goes HI, U826(a) is unable to change as it is cleared by U826(b). The latter is, however clocked by the next positive edge of RAS, which in turn drives U802 & U803 into HI–Z state again. U826(a) changes on the next positive RAS edge.

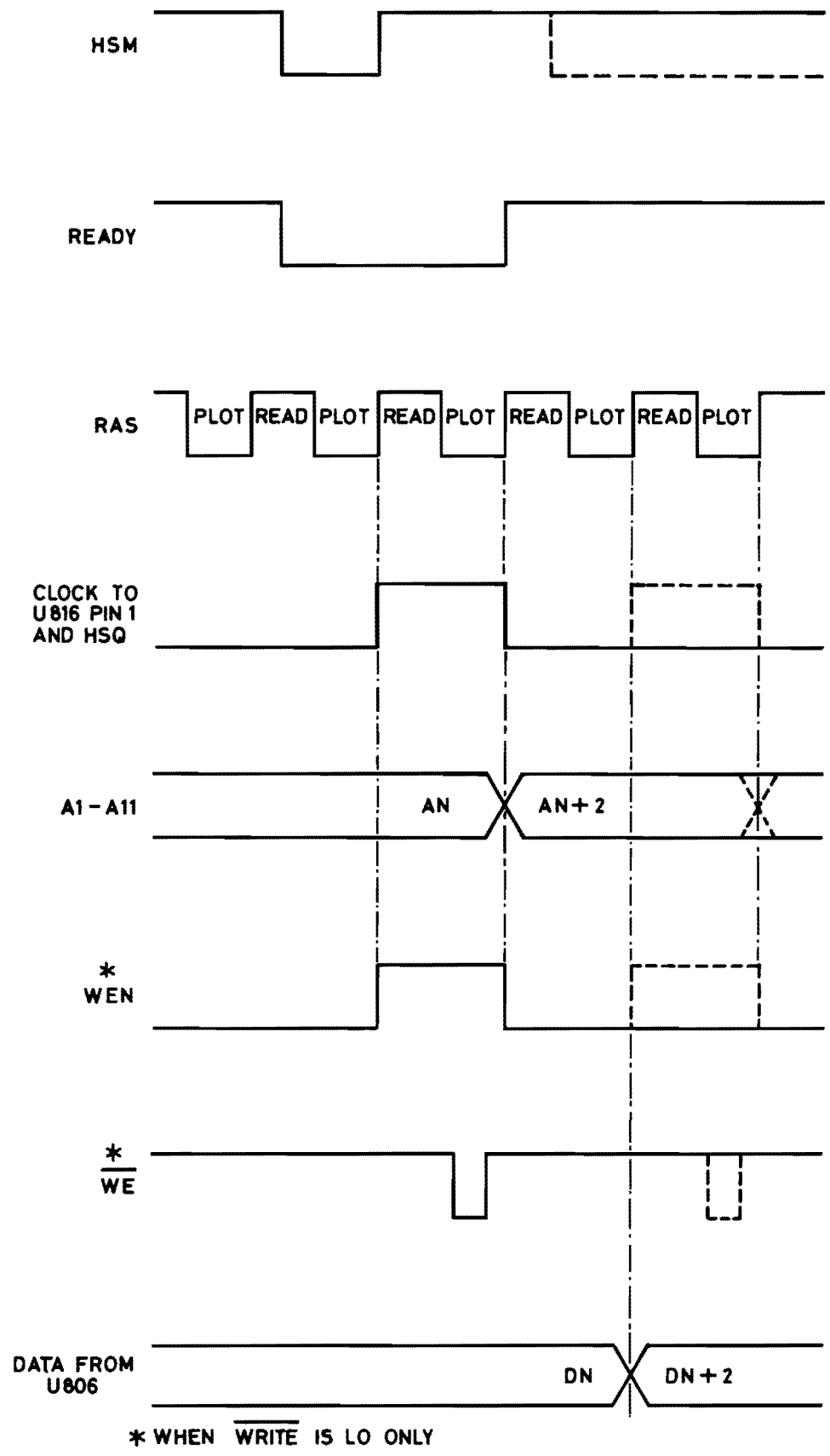


Fig. 4.26 Data I/O Timing

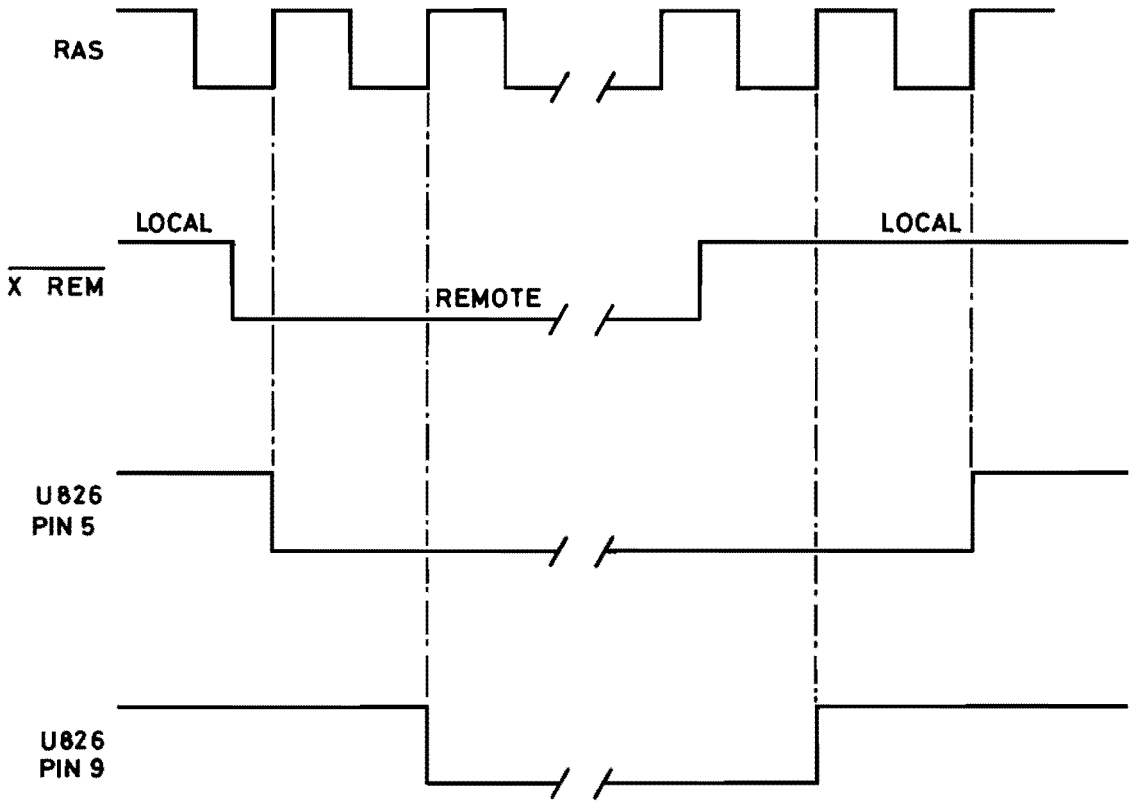


Fig. 4.27 Remote/Local Signals

5.1 GENERAL

The instrument is electrically protected by two fuses as follows:-

1. The supply line fuse, FS51, mounted on the rear panel by the line voltage switch. The rating is 500mA Slo-Blo (Part No. 33685) for 220/240 volt supplies and 1A Slo-Blo (Part No. 34790) for 115 volt supplies.
2. The +170V fuse, FS501, mounted on the Power Supply board at the rear of the instrument. Access is by removing the bottom cover and the fuse rating is 250mA (Part No. 32338).

The following sections give information access to, and removal of, the various printed circuit boards and assemblies as may be found necessary during fault finding procedures.

If, during fault finding, a component needs replacing it may be cut from the printed circuit board as close as possible to the component, leaving the wires protruding through to the component side of the board. The new component can then be soldered into position by attaching it to these protruding wires. This protects the copper track from damage.

If a fault on a printed circuit board cannot be cleared, it is recommended that the instrument is returned to the manufacturer for repair. When faults have been cleared it is recommended that the test procedure be implemented to ensure that the instrument conforms to the specification.

5.2 MECHANICAL ASSEMBLY

5.2.1 LAYOUT

Figures 5.1, 5.2 & 5.3 illustrate the internal layout of the instrument and show the positions of the majority of preset components when the top and bottom covers have been removed. Each cover is retained in position by four latch fasteners. Each fastener is released by turning it one quarter of a turn clockwise or counter clockwise.

WARNING. HIGH VOLTAGES ARE EXPOSED WHEN THE COVERS ARE REMOVED AND THE INSTRUMENT MUST BE WORKED ON ONLY BY SUITABLY QUALIFIED PERSONNEL.

The POWER SUPPLY board contains the low voltage power supplies and also the blanking amplifiers. It is mounted across the rear frame of the instrument behind the c.r.t.

There are two identical Y PRE-AMPLIFIER boards (note that components have identical circuit reference numbers on each of these boards) mounted as 'daughter' boards at the front of the large ANALOGUE TO DIGITAL CONVERTOR (ADC) board. This board is secured underneath the c.r.t. and has two other 'daughter' boards associated with it: the CURRENT SOURCE board which is on the left hand side nearest the frame, and the DECODING LOGIC board on the right hand side.

The E.H.T. board incorporates the high voltage power supplies for the c.r.t. and also the Y OUTPUT AMPLIFIER.

The INTENSITY, SCALE and FOCUS controls are directly mounted on this board, which is adjacent to the c.r.t. and one of four boards mounted vertically. The timing logic is next to the E.H.T. board.

The STORE LOGIC board contains also the DOT JOINER circuit and is the third vertical board.

The TIMEBASE BOARD is mounted on the right hand side of the instrument and includes also the INTERNAL CALIBRATOR circuit.

The circuitry of the 4022 option if fitted is located on a board behind the power supply board. It is covered by the plastic moulded cover. The controls are mounted on a panel recessed in the left side of the instrument.

The construction of the instrument has been arranged so that individual boards and assemblies can be checked and components changed so far as possible without completely removing the assemblies from the mainframe or disconnecting cableforms. In the case of the two logic boards this has been achieved by making them easily withdrawn from inside the mainframe to be mounted on top of the instrument, as shown in Fig. 5.4. The instrument is then still fully functional.

The following description details the method for removing the individual assemblies:-

5.2.2 STORE AND TIMING LOGIC BOARDS

The two logic boards are withdrawn as a unit:-

1. Remove the knobs from the MODE, STORED TRIGGER POINT and DISPLAY MODE lever switches.
2. Remove the 8 screws marked 'A' in Figs. 5.1 & 5.2.
3. Swing the rear fixing bracket upwards to allow it to clear the rear mounting plate as the boards are withdrawn from the front panel. When the unit has been moved far enough to enable the lever switches and pushbuttons to clear the frame, withdraw the assembly from the top of the instrument with the various cableforms still attached.
4. Remove the screens from each board, and also unscrew the screen mounting pillars. This will allow the two boards to be separated. The top bracket should be removed from the top corner of each board. The boards can now be fixed to the top of the instrument supported at the rear, and a single screw through a convenient hole in the frame at the front. Check that all the connectors are firmly in position.

   Refitting is the reverse of the removal procedure.

   Ensure that the 16 way ribbon cable plugs are fully pushed home after fixing the assembly inside the instrument.

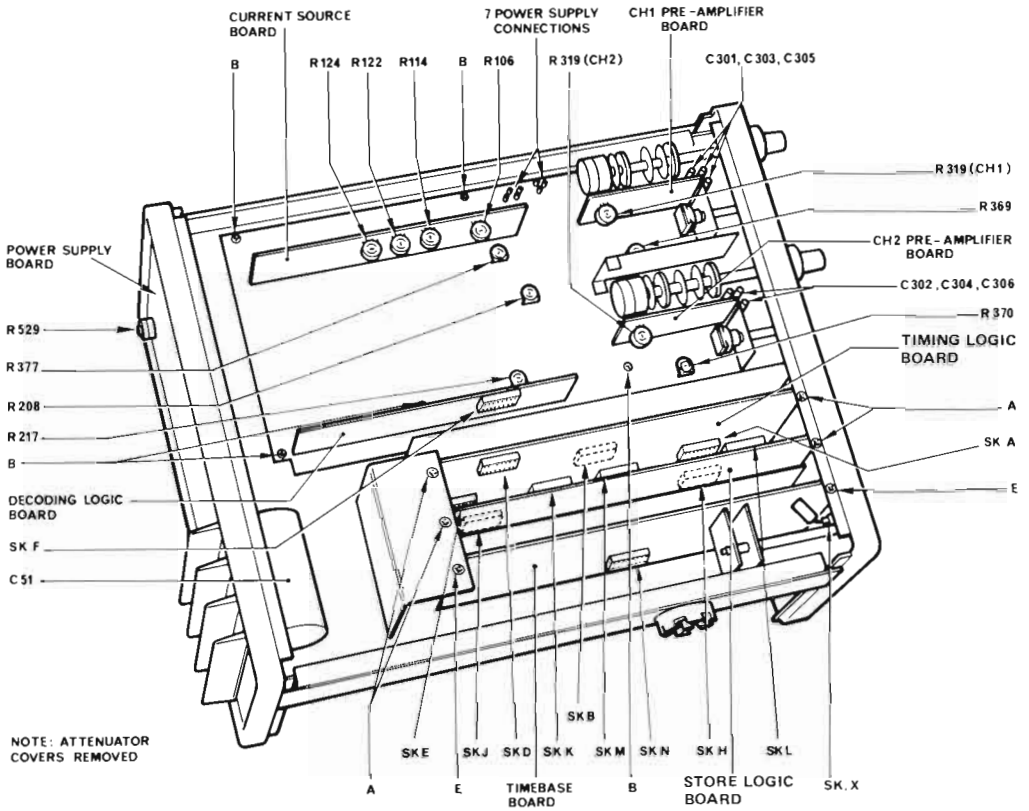


Fig. 5.1 Oscilloscope Bottom View

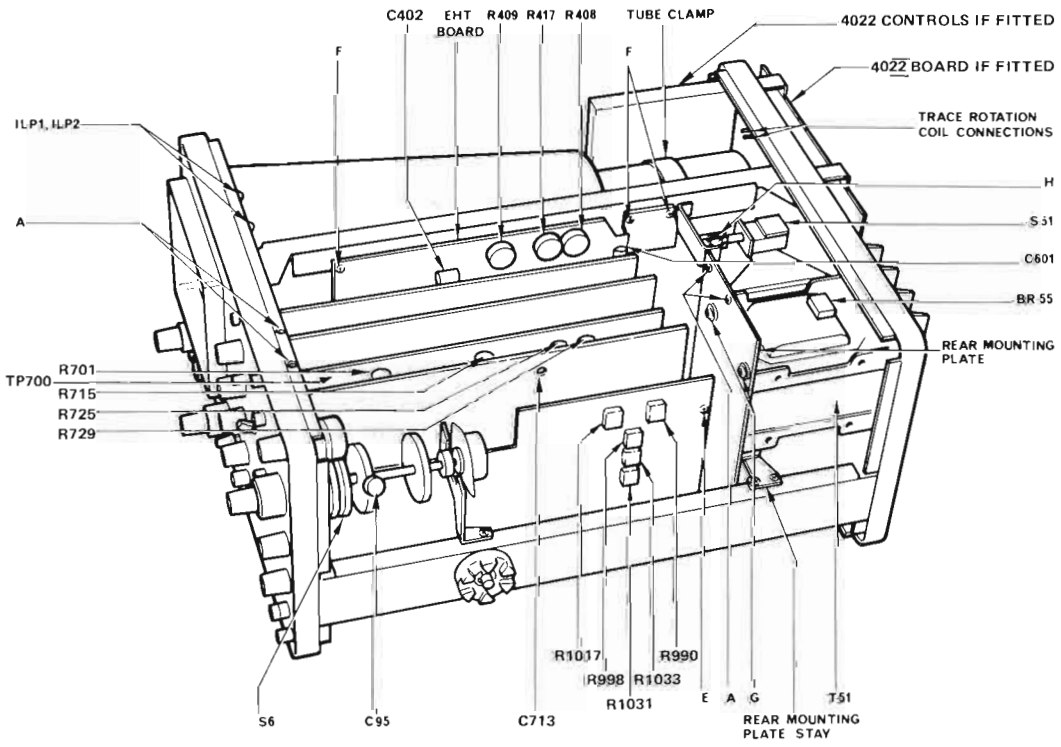


Fig. 5.2 Oscilloscope Right Hand View

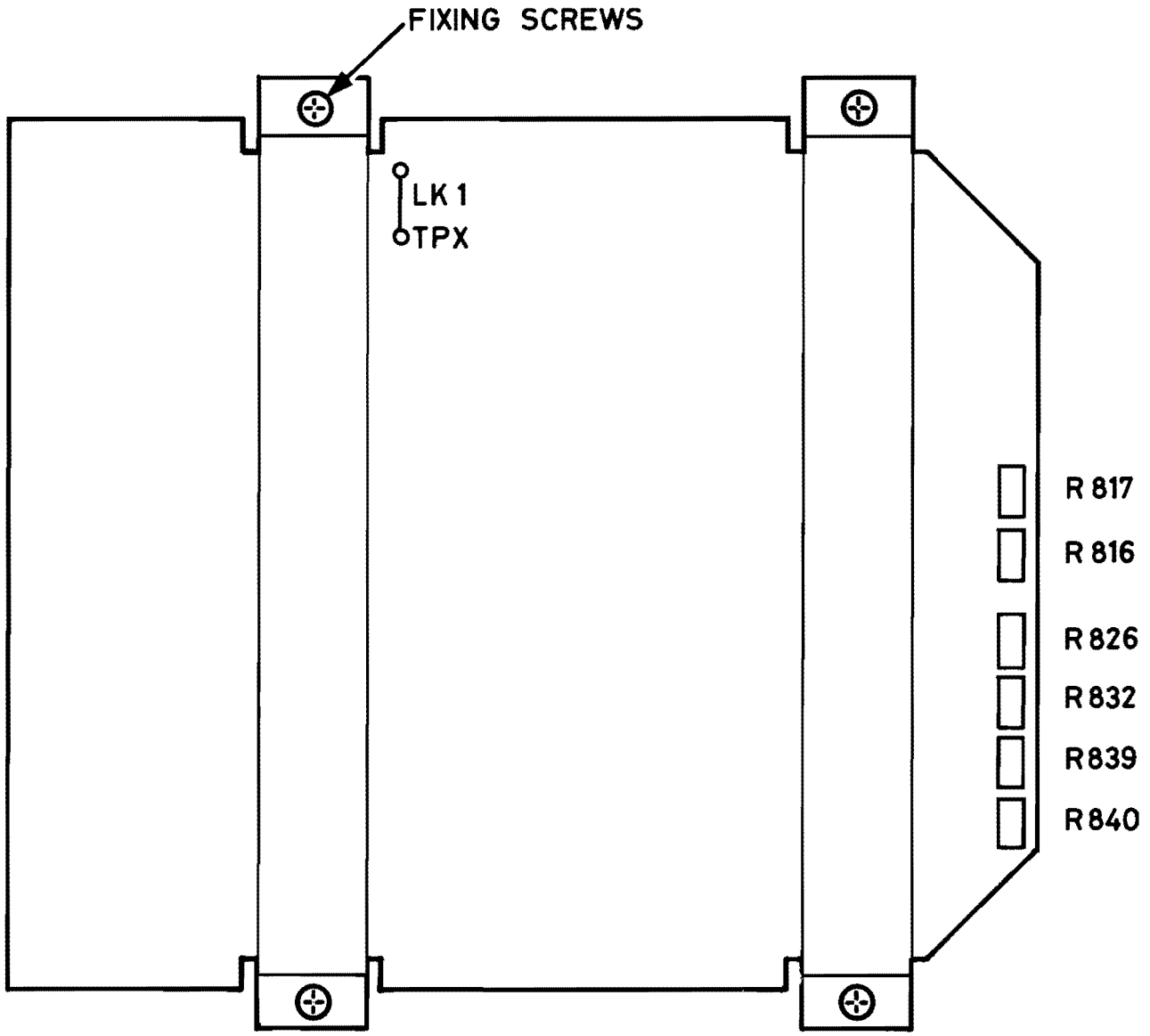


Fig. 5.3 4022 Option

5.2.3 TUBE AND REAR COVER

Removal of the tube is straightforward and provided access to the track side of the Analogue to Digital Converter and E.H.T. boards. Note that access to the rear of the tube may be gained by removing the moulded plastic cover (& 4022 if fitted) which is retained by four fixing screws. The tube is removed together with its magnetic shield in the following manner:-

1. Disconnect the E.H.T. lead at the cavity cap connector at the front of the tube.
2. Disconnect the two trace rotation coil leads at the top of the power supply board. Mark one of these leads so that they may be reconnected in the correct order.
   Disconnect the lead from the tube base to the pin marked GRID on the power supply board.
3. Remove the tube clamp, secured by three screws.
4. The tube may now be pulled back so that the faceplate disengages from the plastic moulding inside the front panel. Lift the front of the tube and remove the connector on the base. Withdraw the tube complete with shield.
5. The tube is a push fit inside the magnetic shield and is removed together with the trace rotation coil, therefore as the tube is withdrawn from the shield the trace rotation coil leads must be fed through the hole in the shield.

5.2.4 ANALOGUE TO DIGITAL CONVERTOR ASSEMBLY

Access to the trackside of the ADC board is best achieved by removing the tube as described in section 5.2.3. If the board must be removed it is taken out together with the Y attenuators, input coupling switches and shift controls as follows:-

1. Remove the Y attenuator cover by removing the five fixing screws and sliding the cover towards the rear of the instrument to clear the edge of the frame. The cover may then be lifted out.
2. Remove the knobs from the Y attenuators, shift controls and input coupling switches. Remove the nut securing the rotary attenuator switches.
3. Disconnect the 7 power supply leads on the left hand edge of the board. Disconnect the 4 minature co-axial plugs across the centre of the board. SK.P, Q, R and S, and the 'BIAS' lead. Remove the 'P' clip securing these leads to the pillar on the right hand side of the board. Disconnect the 16 way flat ribbon cable from SKF on the right hand 'daughter' board.
4. Remove the 5 securing screws marked B in Fig. 5.1. Lift the rear of the board and withdraw it from the instrument.

   Refitting the board is the reverse of the removal procedure, but note that when fitting the securing nut to the attenuator switches, the switch assembly should be held with long-nosed pliers to avoid twisting the switch along its length. The colour code of the power supply leads may be ascertained by inspecting the bottom edge of the power supply board; the two 50 volt supplies marked 'Va' and 'Vb' on the ADC board are interchangeable.

5.2.5 POWER SUPPLY ASSEMBLY

Normal access to the component side of the board is possible by removing the tube, and the trackside of the board is exposed by removing the moulded plastic rear cover (4 fixing screws) and, where appropriate, removing the 4022. The board may be removed by releasing the two screws securing it to the frame and also the two screws securing the heatsink bar at the edge of the board to the finned heatsink assembly. Alternatively the board may be removed as a complete assembly with the finned heatsink, power transformer, ON/OFF switch and C51 in the following manner:-

1. Remove the rear cover.
2. Remove the two screws, marked 'G' in Fig. 5.2, securing the power transformer to the logic assembly mounting plate.
3. Slaken the clamp, marked 'H' in Fig. 5.2, and release the ON/OFF switch actuating rod from the ON/OFF switch.
4. Remove two screws securing the power supply board to the frame on the tube side of the instrument and a further four screws securing the finned heatsink to the frame. Two fixing screws holding the small panel bearing the supply line voltage switch and fuse must also be removed.
5. The rear panel assembly may now be withdrawn sufficiently to replace most of the components: complete separation entails disconnecting the two main cableforms from the power supply board and five leads associated with the c.r.t.
   Refitting is the reverse of removal. Care should be taken to ensure that the insulating shim between the power transformer and the logic assembly mounting plate is correctly positioned and the insulating bushes fitted to the screws 'G' securing these two parts are fitted. The clamp linking supply switch, S51, to the front panel should be carefully aligned so that the switch operates freely without any tendency to stick.

5.2.6 TIMEBASE

Routine access to the timebase board may be gained by removing the logic boards as detailed in section 5.2.2. The timebase range switch may also be removed (see 3. below) and the board itself may be taken out along with the timebase controls (X shift, timebase range, trigger level, source and coupling and external input socket).

Proceed as follows:-

1. Remove the knobs from the 5 rotary controls and the cap from the lever switch.
2. Remove the nit securing the EXT. TRIG. B.N.C. socket and unsolder R91 allowing the socket to be removed.

3. Remove the nut from the bush of the TIME/CM rotary switch. Disconnect the 16 way ribbon cable from the timebase range switch at SKL on the top of the timing logic board. Remove the single fixing screw holding the rear support bracket of the switch to the frame.
4. At the rear of the timebase board, disconnect PLA the twin ribbon cable to the X plates pins 5 and 6, and remove the fixing screw securing the board to the rear mounting plate
5. From underneath the instrument, disconnect and identify the three screened leads to the pins labelled SB, CH1 trig. and CH2 trig. with associate earths, and the single wire to the Line trig. pin. Remove the two bottom fixing screws (marked 'E' in Fig. 5.1). Remove the rear mounting plate stay (see Fig. 5.2). Pull the rear of the board back between the power transformer and the frame side-member until it is possible to disengage the rotary control spindles from their holes in the front panel. The board may now be withdrawn from the instrument, together with the TIME/CM switch.

5.2.7 E.H.T. BOARD

Access to the E.H.T. board is normally obtained by removing the c.r.t. and the two logic boards. If, for some reason, the board itself must be removed, proceed as follows:-

1. Remove the c.r.t. the logic board assemble and the ADC board assembly.
2. Slacken the clamp 'H' (see Fig. 5.2) and withdraw the ON/OFF switch actuating rod through the front panel.
3. Remove the knobs from the SCALE, INTENSITY and FOCUS controls. Remove the small plate in front of the ON/OFF switch. Disconnect all leads.
4. Release the 3 screws marked 'F' in Fig. 5.2 and pull the board towards the rear of the instrument until the control spindles clear the front panel, and remove the board from the instrument.

5.2.8. 4022 OPTION

Access to the component side and adjustments of the 4022 is obtained by removing the four screws securing the rear cover. Access to the track side is obtained by removing the four securing screws shown in Fig. 5.3 whereupon the board may be hinged away from the power supply.

5.3 CALIBRATION PROCEDURE

The calibration procedure is detailed below. Note that any calibration adjustments found necessary must not be made until a 15 minute warm-up period has elapsed. The locations of the various preset components are shown in Figs. 5.1 and 5.2.

5.3.1 TEST EQUIPMENT REQUIRED

1. Multimeter to measure up to 1500 volts with better than 20kΩ per volt impedence, Accuracy to be within ±2%.
2. Variable Autotransformer (Variac, etc.) Output voltage range 200–270 volts at 1A with a.c. r.m.s. voltmeter.
3. Function Generator with frequency range of 0.1Hz to 10kHz, preferably with sawtooth output.
4. Digital Voltmeter with 3½ digit display and 1mV basic resolution. Accuracy to be within ±0.2%.
5. Source of Time and Voltage Calibration signals, to cover the range 0.1μs–0.5s and 25mV – 100V.
6. Square-wave generator to provide 500kHz flat top square wave with amplitude adjustable between 25mV and 1 volt. Risetime to be less than 5ns.
7. Constant amplitude r.f. sine-wave generator to cover the range 500kHz to 15MHz with a 50kHz reference frequency. Output amplitude 25mV to 5 volts pk-pk when terminated with 50Ω load. Amplitude accuracy over the frequency range to be within ±3%.
8. Capacitance standardiser. 1MΩ/28pF with B.N.C. connections.
9. 50Ω B.N.C. through-termination.
10. E.H.T. meter to measure 3kV.
11. Frequency Counter to measure 1kHz at 1 volt.

5.3.2 POWER SUPPLY VOLTAGES

1. Set the INTENSITY control to minimum.
2. Set the SUPPLY VOLTAGE switch on the rear panel to suit the available supply. Using the auto-transformer, set the supply to the instrument to within ±1% of the selected nominal voltage.
3. Check that the POWER LED is lit and that the SCALE control varies the graticule illumination.
4. Check the voltages with respect to the chassis at the pins on the lower edge of the power supply board as follows:-

	voltage limits	
pin	min.	max.
+5	5.0	5.5
–20	–19	–21
–6	–5.5	–6.5
+12	11.4	12.6
+20	19	21
+170	155	185

5. Measure the voltage across C402 (see Fig. 5.2) on the E.H.T. board and adjust R409 (SET E.H.T.) to bring this to 185V with the supply voltage adjusted as in 2. above.
6. Measure the voltage at the –1kV pin on the E.H.T. board (near C403). This voltage should be between –950V and –1050V with respect to the chassis, check that it does not vary by more that 10V when the supply voltage to the instrument is

varied by ±10% of the nominal voltage selected with the SUPPLY VOLTAGE switch.

7. Check that the voltage on the '+3kV' pin at the rear of the E.H.T. board (to which the cable from the c.r.t. cavity cap connector is fitted), is greater than 2.5kV relative to chassis.

5.3.3 GEOMETRY

1. Set the MODE switch to NORMAL, the TIME/CM. switch to 1ms/cm and ensure the TRIGGER LEVEL control is pushed in ('Bright Line' position). With the INTENSITY control advanced approximately half way and the Y MODE switch in the dual trace position, obtain two traces on the screen.
2. Adjust the FOCUS control in conjunction with R417 ('ASTIG') on the E.H.T. board to obtain clear traces.
3. Adjust the TRACE ROTATION control, R529, on the rear panel to align the traces with the horizontal graticule lines.
4. Apply a 1kHz sinewave to one channel and adjust the sensitivity and triggering controls to obtain a stable display with an amplitude of 8cms pk-pk. Adjust R408 (GEOM) on the E.H.T. board for minimum distortion of the display in both X and Y axes. Reset the FOCUS and ASTIG controls to optimise the trace quality.

5.3.4 Y CALIBRATION AND SHIFT TRACE

1. With the input coupling switch in the GND position select CH1 on the Y MODE switch and adjust the front panel BALance control, R373 so that there is no trace shift when changing from the 0.2V/cm range to the 0.5V/cm range. Adjust R369 (VAR BAL) on the ADC board so that there is no shift when the CH1 variable sensitivity control is operated.
2. Repeat the preceding step for CH2 using R374 (BAL) and R370 (VAR BAL).
3. With dual trace selected set the two Y shift pots, R1 and R2, so that the wipers (measured at the pins marked 'SH' on the front of the ADC board) are at +4V with respect to chassis. Adjust R377 (SHIFT CENTRE) so that the two traces are equally spaced each side of the central horizontal graticule lines.
4. Apply a sinewave signal to each channel in turn and set the amplitude for 8cm pk-pk display. Check that the traces can be shifted completely off the screen in each direction.
5. With CH1 only selected, set the attenuator switch to 20mV/cm and apply a 100mV, 1kHz square wave signal from the calibrator. Monitor the signal voltage at the junction of R389 and D316 cathode on the ADC board with an oscilloscope. Adjust R319 on the CH1 pre-amplifier board to set the signal level to 185mV. Repeat the procedure on CH2.
6. With a 100mV signal still applied on the 20mV/cm range, set R438 (in the centre of the E.H.T. board) for 5cms display. Check calibration of other channel.

5.3.5 ATTENUATOR COMPENSATION

1. Check that attenuator cover is fitted.
2. Set CH1 attenuator switch to 0.2V/cm and apply a 2V, 1kHz square wave via a 1MΩ/28pF standardiser. Adjust C301 for a square corner to the display. Repeat procedure with CH2 adjusting C302.
3. Set CH1 attenuator to 0.5V/cm and apply a 2.5V, 1kHz square wave direct. Adjust C305 for a square corner to the display. Repeat step with CH2 adjusting C306.
4. With CH1 attenuator still set at 0.5V/cm, apply a 5V, 1kHz square wave via the standardiser and adjust C303 for a square corner. Repeat step with CH2 adjusting C304.
5. Remove standardiser and check all attenuator ranges applying the appropriate amplitude, to ensure all ranges give a square corner to the applied waveform and are accurate in amplitude to within ±3%.

5.3.6 TIMEBASE CALIBRATION – NORMAL MODE

1. Set TIME/CM control to 1ms/cm and X EXPAND control to X10 (fully clockwise position). Apply 1ms markers to CH1, adjusting Y sensitivity to give approximately 3cm amplitude, triggering with bright line off (TRIGGER LEVEL control pulled out). Adjust R990 (SET x 10) on the timebase board for exactly 10cms between markers.
2. Set X EXPAND to X1 (fully counter clockwise) and adjust R988 (SET X1) on timebase board for 1cm between markers.
3. With 1ms markers still applied, vary the supply voltage to the instrument by ±10% from the nominal value and check that there is less than ±1% change in timebase calibration.
4. Set TIME/CM to 10μs/cm and apply 10μs markers. Adjust the trimmer, C95, on the timebase range switch for 1cm between markers.
5. Set TIME/CM to 1μs/cm and apply 0.1μs markers with the X EXPAND control in the X10 position. Using the X shift control, ensure that the calibration of the first 10cms of trace and the middle 10cms of the trace are within ±4%
6. With the X EXPAND control at X1, check all the timebase ranges from 1μs/cm to 0.5s/cm, with the appropriate markers, to within ±3%. Check that the REFRESHED mode is automatically selected on ranges below 0.5s/cm.
7. Check that the trace length is greater than 12.8cms on all timebase ranges.

5.3.7 TIMEBASE CALIBRATION – DIGITAL MODE

1. Set DISPLAY MODE switch to REFRESHED, TIME/CM switch to 2ms/cm and X EXPAND to X1 (fully anti-clockwise position). DISPLAY SELECT TO FULL STORE. Apply 2ms markers to CH1 as in 5.4.6 (1). Adjust R1033 for exactly 1cm between markers.
2. Switch DISPLAY SELECT to the first quadrant and adjust R1031 for exactly 4cm between markers.
3. Switch TIME/CM switch to 1msec/cm and apply 1ms markers. Check for 5cm between markers ±1mm.

5.3.8 TRIGGER BALANCE

1. With the DISPLAY MODE switch in the NORMAL position and no trigger signal spplied, check that the timebase free runs with the BRIGHT LINE on and does not free run with the BRIGHT LINE off.
2. Apply a 1kHz sine wave and adjust amplitude to give approximately 6cms display. Adjust R1012 on the timebase board (below the timebase range switch, S6) so that there is no vertical shift in the trigger point when moving the TRIGGER SOURCE control between + and –. Check that the TRIGGER LEVEL is midway through its range when the timebase is triggering at the zero crossing point on the displayed waveform.
3. With the signal applied to CH1 input, adjust R1011 on the timebase board so that there is no change in trigger point when the TRIG. COUPLING switch is moved from AC to DC. Repeat this adjustment with R1009 for CH2.
4. Check that the LF and HF REJECT positions of the TRIG. COUPLING switch are functional.
5. Apply a 1kHz square wave input signal and reduce the amplitude to 2mm. Check that stable triggering can be obtained on both + and – slope positions for both input channels.
6. Set the TRIG SOURCE selector to EXT. and apply a 1 volt, 1kHz square wave to the EXT TRIG input. Check that stable triggering can be obtained on both + and – slope settings with the BRIGHT LINE either on or off.
7. Check the LINE trigger facility is functional and that the L.E.D. lamp associated with the TRIGGER LEVEL control is working.

5.3.9 INTERNAL CALIBRATOR

Set the pk-pk amplitude of the 1V calibrator output using R1017 on the timebase board (SET CAL). Check the 0.1V output is accurate within ±2%.

5.3.10 Y PULSE RESPONSE

1. With the CH1 attenuator set at 20mV/cm apply a fast risetime 500kHz flat topped square wave to CH1, using a 50Ω termination to prevent cable reflections. Adjust amplitude for a 5cm display and set C419 and C424 on the E.H.T. board for a square corner with less than 1% undershoot or overshoot. Check CH2 at the same sensitivity.
2. Set the Y attenuators to 5mV/cm and apply a signal from the constant amplitude r.f. generator. Set the signal amplitude at 50kHz to give 5cm display and then increase the input frequency until the display height falls to 3.5cm. This frequency should be greater than 11MHz. Repeat this procedure with CH2.
3. Apply the 500kHz square wave and check the pulse response on all attenuator ranges with 5cms display. Both channels must exhibit less than 2% undershoot or overshoot on any range.

5.3.11 H.F. TRIGGER

Apply a 10MHz sine wave to CH1 and adjust amplitude for 1cm of display on the 20mV/cm attenuator range. Check that steady triggering can be obtained with the BRIGHT LINE switched off. Switch the attenuator to 0.1V/cm to give 2mm display and reduce the input frequency to 2MHz. Check for stable triggering and repeat both tests on CH2.

5.3.12 CLOCK OSCILLATOR FREQUENCY

Set the DISPLAY MODE switch to NORMAL and connect the calibrator output to a frequency counter, adjust C607 on the Timing Logic Board for a frequency of 976Hz ±1%.

5.3.13 ANALOGUE TO DIGITAL CONVERTOR

1. Measure the voltage across the pins of the A.O.T. resistor, R163, on the ADC board with a d.v.m. Adjust R106 on the current source board to bring this voltage to 2.80V.
2. Measure the voltage across the pins of A.O.T. resistor R289. Adjust R124 on the current source board to bring this voltage to 0.817V.
3. With the DISPLAY MODE switch in the REFRESHED position apply a triangle or sine wave input signal and set the amplitude for a display of 8cms. Adjust the timebase and trigger controls so that one half cycle is displayed from the positive peak to the negative peak. Ensure that the l.e.d. associated with the TRIGGER LEVEL control is lit.
4. Adjust R122 to minimise conversion errors (notches) at the ¾ scale point (i.e. at approx. 2cms above the graticule centre line) on the display.
5. Adjust R114 to minimise conversion errors occuring at the ¼ and ½ scale points. Errors at these points will also be affected by R122. If the conversion errors cannot be entirely removed by these two adjustments, it may be necessary to fit a resistor of between 10kΩ and 27kΩ in value, in the position marked R163. Similarly, if there are regular groups of errors occurring in each quarter of the screen, a resistor of value 3k9 to 12kΩ may

be fitted in the position marked R289. It is emphasised that these adjustments should only be used for correcting SMALL conversion errors.

5.3.14 DIGITAL TO ANALOGUE CONVERTOR

The DAC must be set up to 30 samples per cm. Proceed as follows:

1. Set the DISPLAY MODE switch to REFRESHED and GROUND the input. Rotate the Y shift control fully anti-clockwise to deflect the trace to its lower limit. Ground TP700 on the top edge of the store logic board (see Fig. 5.2) and adjust R715 to position the trace 1cm above the centre graticule line.
2. Remove the ground on the test point and adjust R701 to position the trace 3.3cm below the centre graticule line.
3. Adjust R715 and R701 as previously described until both are correct.
4. Ground TP700 and adjust R701 to bring the trace exactly to the centre line. Remove the ground on the test point.

5.3.15 SCALING AMPLIFIER

With a 5cm square wave displayed in the NORMAL mode, set R208 on the ADC board to give no change in amplitude when switching from NORMAL to REFRESHED. Similarly set R217 for no change in vertical position.

5.3.16 DOT JOINER

1. Switch to CH1, REFRESHED mode, TIME/CM to 0.2ms/cm unexpanded 1st quadrant and apply a 10kHz 4cm high square wave. Adjust C713 on the store logic board for 'cleanest' trace.
2. Adjust the X EXPAND control to approximately X5 and adjust R725 for a square corner.
3. Switch to dual trace, GROUND CH2 and adjust R729 for a square corner.

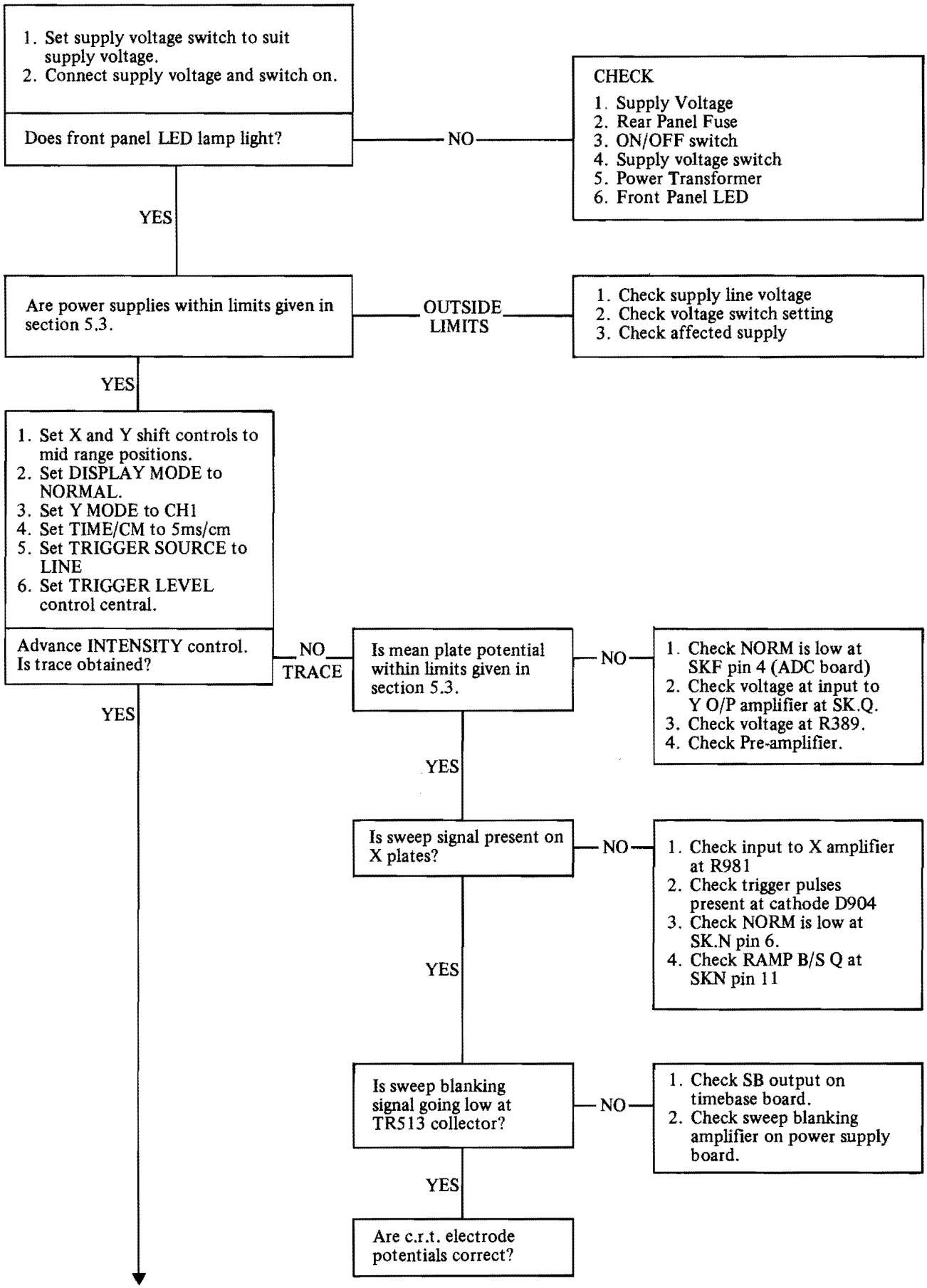
5.4 4022 CALIBRATION PROCEDURE

1. Remove the back cover to obtain access to controls.
2. Select CONTINUOUS plot mode and if necessary press the front panel PLOT button to exit the plot mode. Select CH1 only with grounded input.
3. Connect a d.v.m. to the CH1 output BNC connector. Adjust the zero preset R832 for an output in the range 0 to +3mV.
4. Shift the trace fully off the top of the screen and press PLOT. Adjust the gain preset R826, for an output of 427mV ±1mV. Press PLOT again and shift trace fully off the bottom of the screen. Press PLOT again. Check that the output is in the range −423mV to −431mV, adjusting VR3 if required. Exit the PLOT mode.
5. Connect the d.v.m. to the CH2 output and repeat steps 3 & 4 adjusting R817 and R816 respectively.
6. Connect the d.v.m. to the X output BNC. Unsolder link LK800 and adjust R839 for an output of +512mV ±2mV.
7. Reconnect link LK800 and adjust R840 for zero ±1mV at output.
   Repeat (6) & (7).

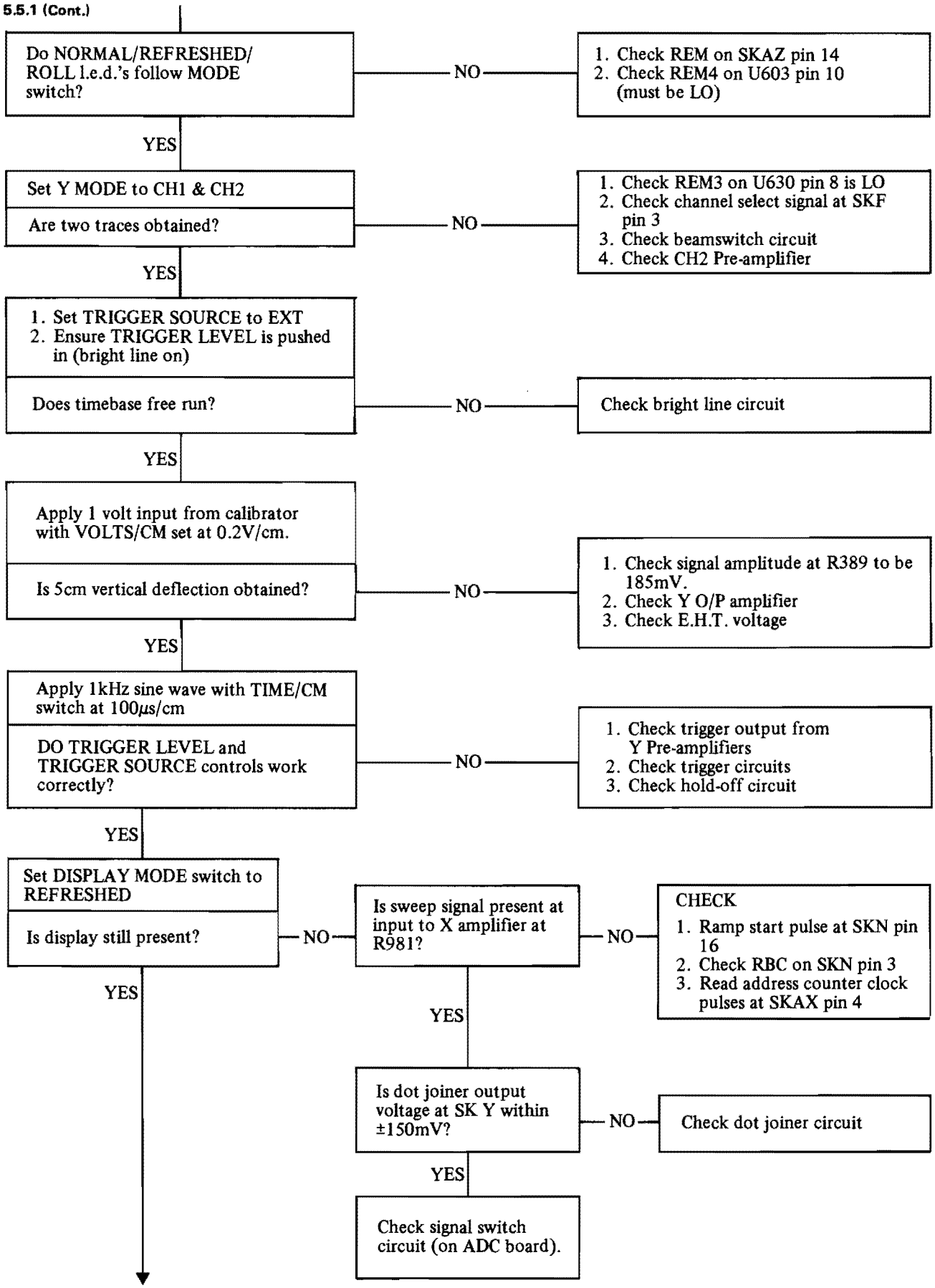
5.5 FAULT FINDING

Faults may be localised by the procedure given in section 5.5.1. Faults in the data path, as opposed to analogue or control logic faults may be localised by following the flow chart in section 5.5.2. More detailed analysis will be aided by the circuit voltages as shown in section 5.6 and reference to the appropriate part of section 4.

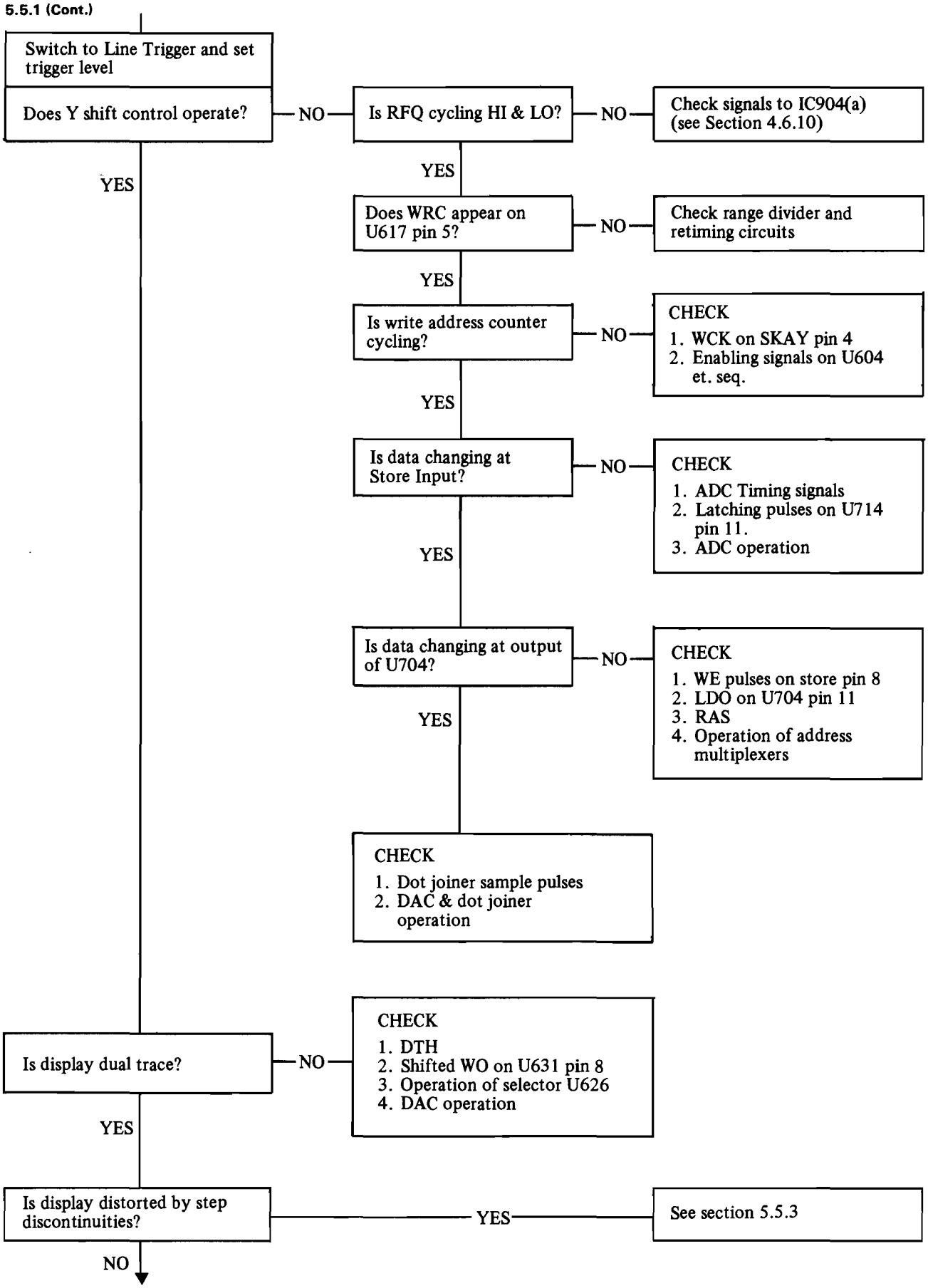
SECTION 5.5.1 FAULT LOCALISATION PROCEDURE



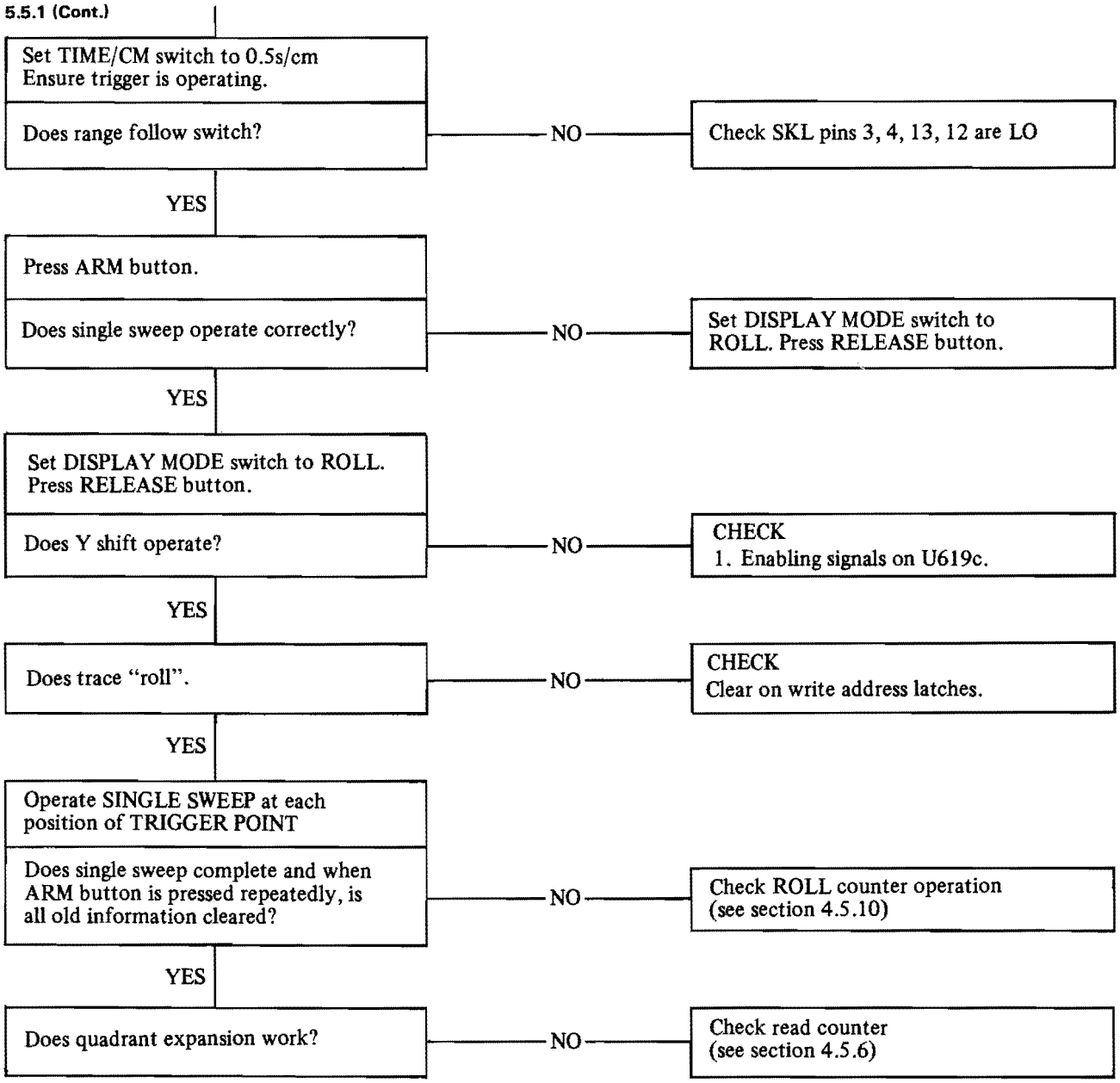
5.5.1 (Cont.)


Do NORMAL/REFRESHED/ ROLL l.e.d.'s follow MODE switch?
NO
1. Check REM on SKAZ pin 14
2. Check REM4 on U603 pin 10 (must be LO)
YES
Set Y MODE to CH1 & CH2
Are two traces obtained?
NO
1. Check REM3 on U630 pin 8 is LO
2. Check channel select signal at SKF pin 3
3. Check beamswitch circuit
4. Check CH2 Pre-amplifier
YES
1. Set TRIGGER SOURCE to EXT
2. Ensure TRIGGER LEVEL is pushed in (bright line on)
Does timebase free run?
NO
Check bright line circuit
YES
Apply 1 volt input from calibrator with VOLTS/CM set at 0.2V/cm.
Is 5cm vertical deflection obtained?
NO
1. Check signal amplitude at R389 to be 185mV.
2. Check Y O/P amplifier
3. Check E.H.T. voltage
YES
Apply 1kHz sine wave with TIME/CM switch at 100μs/cm
DO TRIGGER LEVEL and TRIGGER SOURCE controls work correctly?
NO
1. Check trigger output from Y Pre-amplifiers
2. Check trigger circuits
3. Check hold-off circuit
YES
Set DISPLAY MODE switch to REFRESHED
Is display still present?
NO
Is sweep signal present at input to X amplifier at R981?
NO
CHECK
1. Ramp start pulse at SKN pin 16
2. Check RBC on SKN pin 3
3. Read address counter clock pulses at SKAX pin 4
YES
YES
Is dot joiner output voltage at SK Y within ±150mV?
NO
Check dot joiner circuit
YES
Check signal switch circuit (on ADC board).

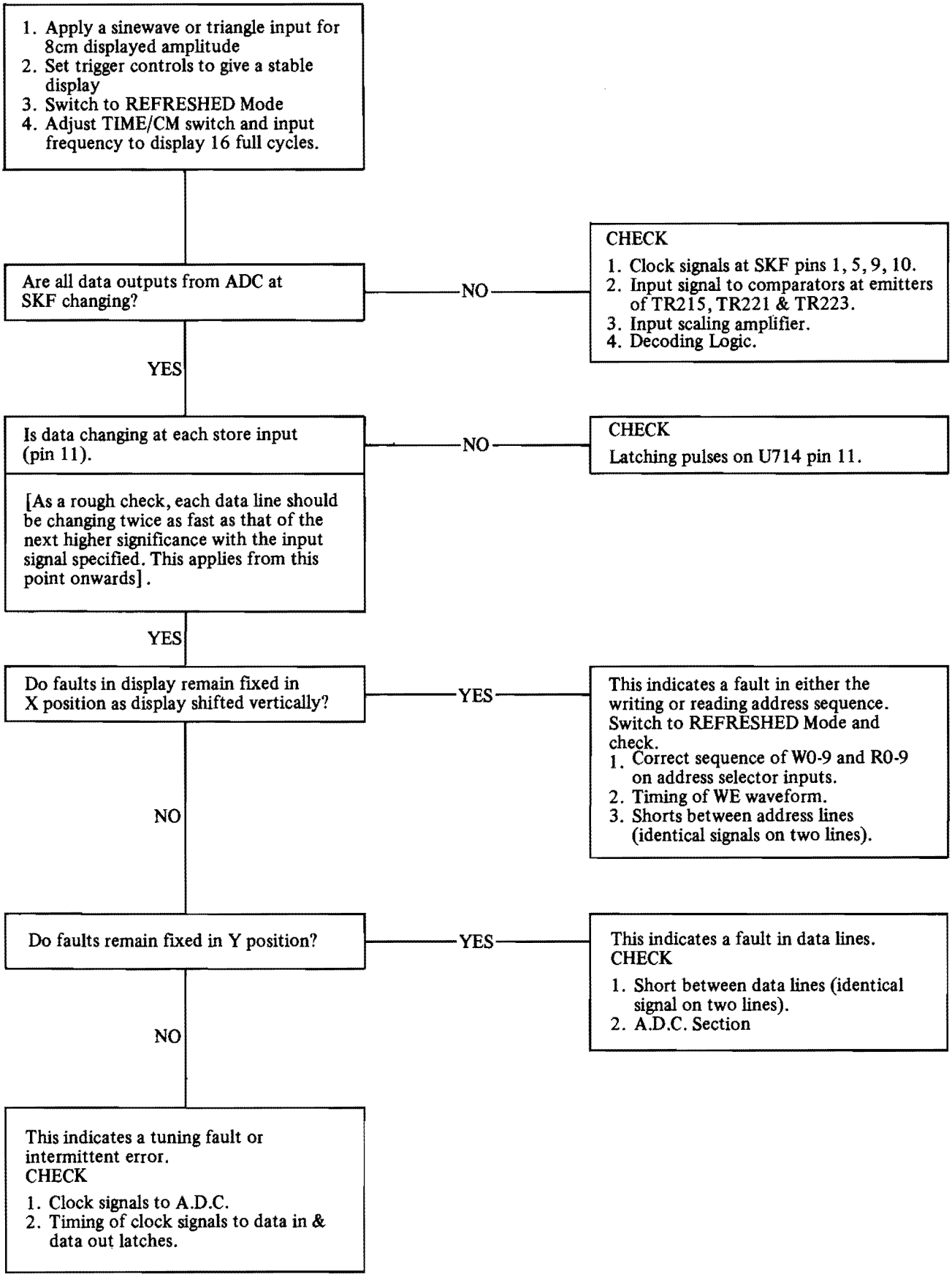
5.5.1 (Cont.)


Switch to Line Trigger and set trigger level
Does Y shift control operate?
NO
Is RFQ cycling HI & LO?
NO
Check signals to IC904(a) (see Section 4.6.10)
YES
YES
Does WRC appear on U617 pin 5?
NO
Check range divider and retiming circuits
YES
Is write address counter cycling?
NO
CHECK
1. WCK on SKAY pin 4
2. Enabling signals on U604 et. seq.
YES
Is data changing at Store Input?
NO
CHECK
1. ADC Timing signals
2. Latching pulses on U714 pin 11.
3. ADC operation
YES
Is data changing at output of U704?
NO
CHECK
1. WE pulses on store pin 8
2. LDO on U704 pin 11
3. RAS
4. Operation of address multiplexers
YES
CHECK
1. Dot joiner sample pulses
2. DAC & dot joiner operation
Is display dual trace?
NO
CHECK
1. DTH
2. Shifted WO on U631 pin 8
3. Operation of selector U626
4. DAC operation
YES
Is display distorted by step discontinuities?
YES
See section 5.5.3
NO

5.5.1 (Cont.)


Set TIME/CM switch to 0.5s/cm
Ensure trigger is operating.
Does range follow switch?
NO
Check SKL pins 3, 4, 13, 12 are LO
YES
Press ARM button.
Does single sweep operate correctly?
NO
Set DISPLAY MODE switch to ROLL. Press RELEASE button.
YES
Set DISPLAY MODE switch to ROLL.
Press RELEASE button.
Does Y shift operate?
NO
CHECK
1. Enabling signals on U619c.
YES
Does trace "roll".
NO
CHECK
Clear on write address latches.
YES
Operate SINGLE SWEEP at each position of TRIGGER POINT
Does single sweep complete and when ARM button is pressed repeatedly, is all old information cleared?
NO
Check ROLL counter operation (see section 4.5.10)
YES
Does quadrant expansion work?
NO
Check read counter (see section 4.5.6)

5.5.2 CHECKING DATA PATH



5.5.3 ANALOGUE TO DIGITAL CONVERTOR FAULTS

With the DISPLAY MODE set to REFRESHED apply a sine wave or triangle input signal. Set the amplitude and trigger controls so that a single half cycle of the input signal is displayed from positive peak to negative peak as in Fig.

Is signal correct at the emitter of TR215? This should be inverted in sense and at approx. 3.7 volts peak amplitude for full screen deflection.

INCORRECT AMPLITUDE OR DISTORTED WAVEFORM

1. Check scaling amplifier circuit and adjustment.
2. Check sample and Hold circuit.

YES

Are first two data bits (D7, D6) changing in correct manner? See Fig.

NO

1. Check comparators.
2. Check reference voltages
3. Check decoding logic.

YES

Is signal waveform at emitter of TR221 correct? (see Fig.

NO

1. Check first two switched current sources, TR136 and TR139.
2. Check first summing amplifier.

YES

Are data bits D5, D4, D3 correct? (see Fig.

NO

1. Check comparators.
2. Check second row reference voltages.
3. Check decoding logic.

YES

Is signal waveform at emitter of TR223 correct? (see Fig.

NO

1. Check remaining three switched current sources, TR144, TR147 and TR150.
2. Check second summing amplifier.

YES

Are data bits D2, D1, D0 changing?

NO

1. Check third row comparators.
2. Check third row reference voltage chain.
3. Check decoding logic.

YES

Are errors (notches) present in the display at fixed Y levels?

YES

Does pattern repeat in each quarter of screen?

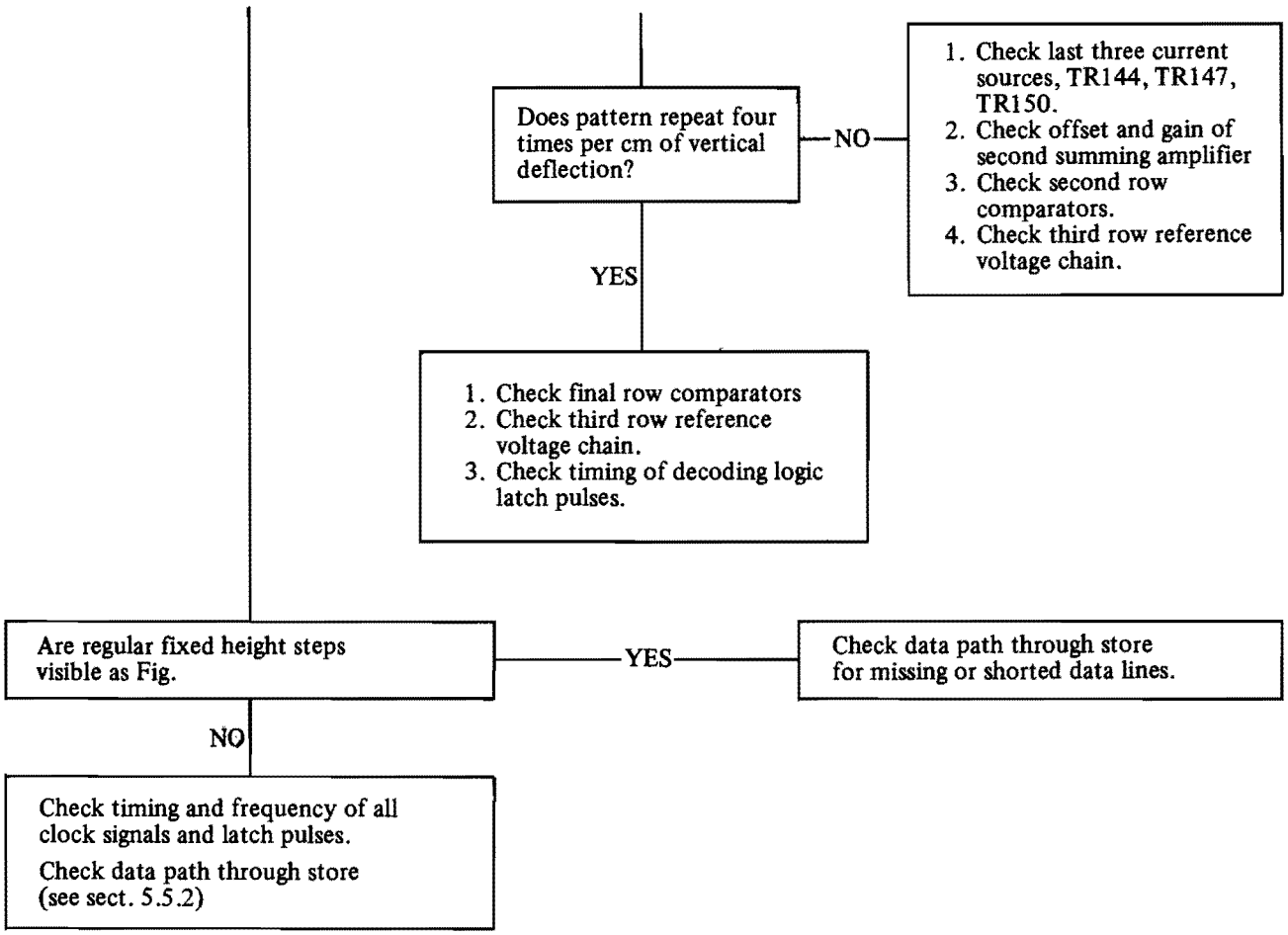
NO

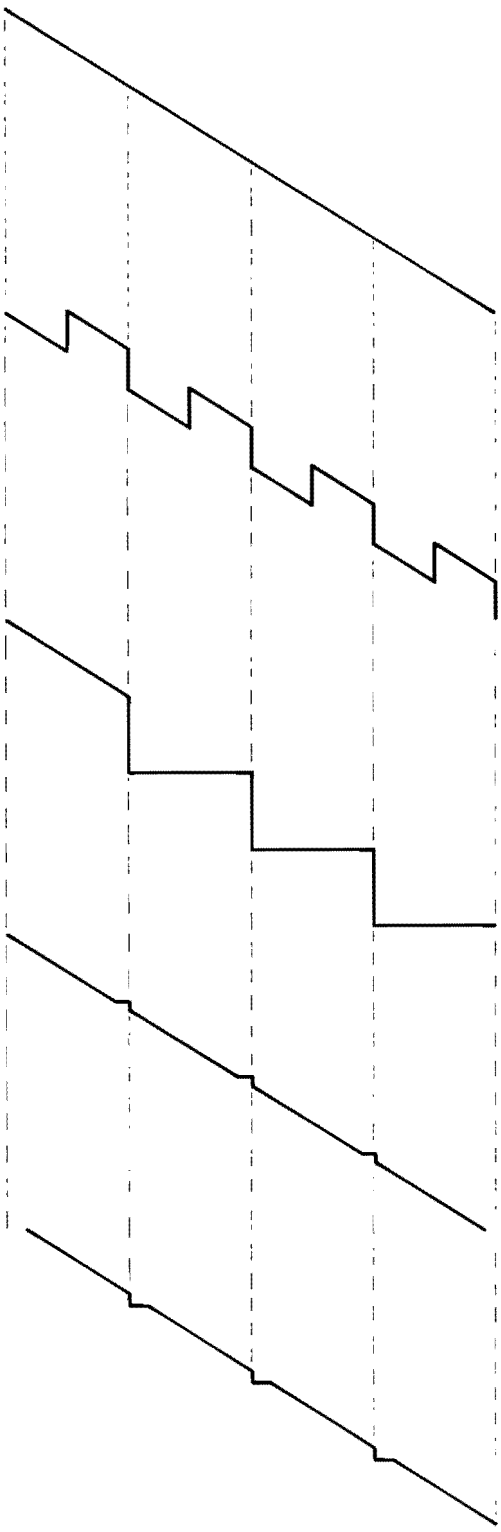
1. Check first two current sources.
2. Check offset and gain of first summing amplifier.
3. Check first row comparators.
4. Check second row reference voltage chain.

NO

YES

5.5.3 (Cont.)


Does pattern repeat four times per cm of vertical deflection?
NO
1. Check last three current sources, TR144, TR147, TR150.
2. Check offset and gain of second summing amplifier
3. Check second row comparators.
4. Check third row reference voltage chain.
YES
1. Check final row comparators
2. Check third row reference voltage chain.
3. Check timing of decoding logic latch pulses.
Are regular fixed height steps visible as Fig.
YES
Check data path through store for missing or shorted data lines.
NO
Check timing and frequency of all clock signals and latch pulses.
Check data path through store (see sect. 5.5.2)



A/ INPUT SIGNAL

B/ DATA BIT MISSING

STEP HEIGHT	DATA LINE
4 cms	D7
2 cms	D6
1 cm	D5
5 mm	D4
2.5 mm	D3
1.2 mm	D2
.6 mm	D1
.3 mm	D0

C/ FIRST TWO SWITCHED CURRENT SOURCES IN ADC NOT WORKING (TR136 AND TR139)
OR
FIRST SUMMING AMPLIFIER FAULTY.

D/ Similar faults for remaining three current sources and second summing amplifier but step height 4 times smaller and pattern repeats over each quarter of the screen.

E/ CONVERSION ERRORS DUE TO

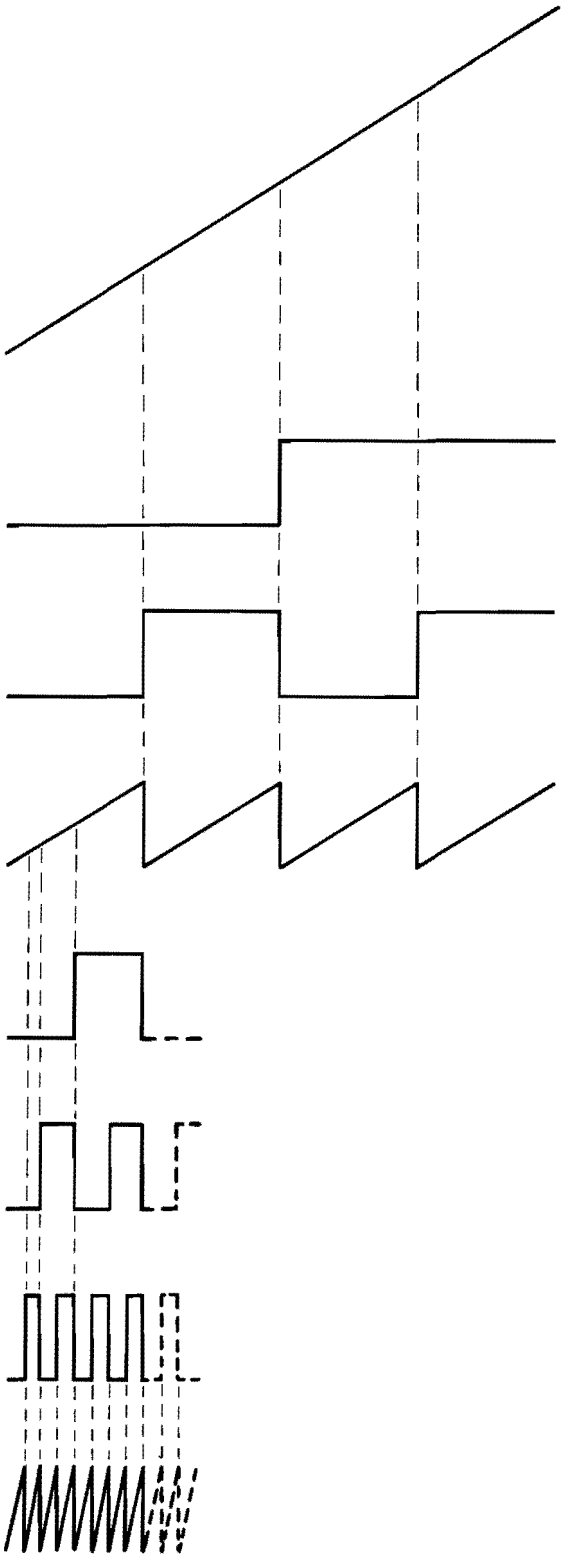
1/ Maladjustment of current sources (R122, R114)

2/ Offsets in first summing amplifiers.

3/ Offsets in first row of comparators.

4/ Timing errors (check clock signal timing)

Fig. 5.4 Data Faults



A/ INPUT SIGNAL AT EMITTER OF TR215

B/ D7 OUTPUT (SK.F PIN. 16)

C/ D6 OUTPUT (SK.F PIN. 15)

D/ WAVEFORM AT EMITTER OF TR221 OUTPUT OF FIRST SUMMING AMPLIFIER

E/ D5 OUTPUT (SK.F PIN 14)

F/ D4 OUTPUT (SK.F PIN 13)

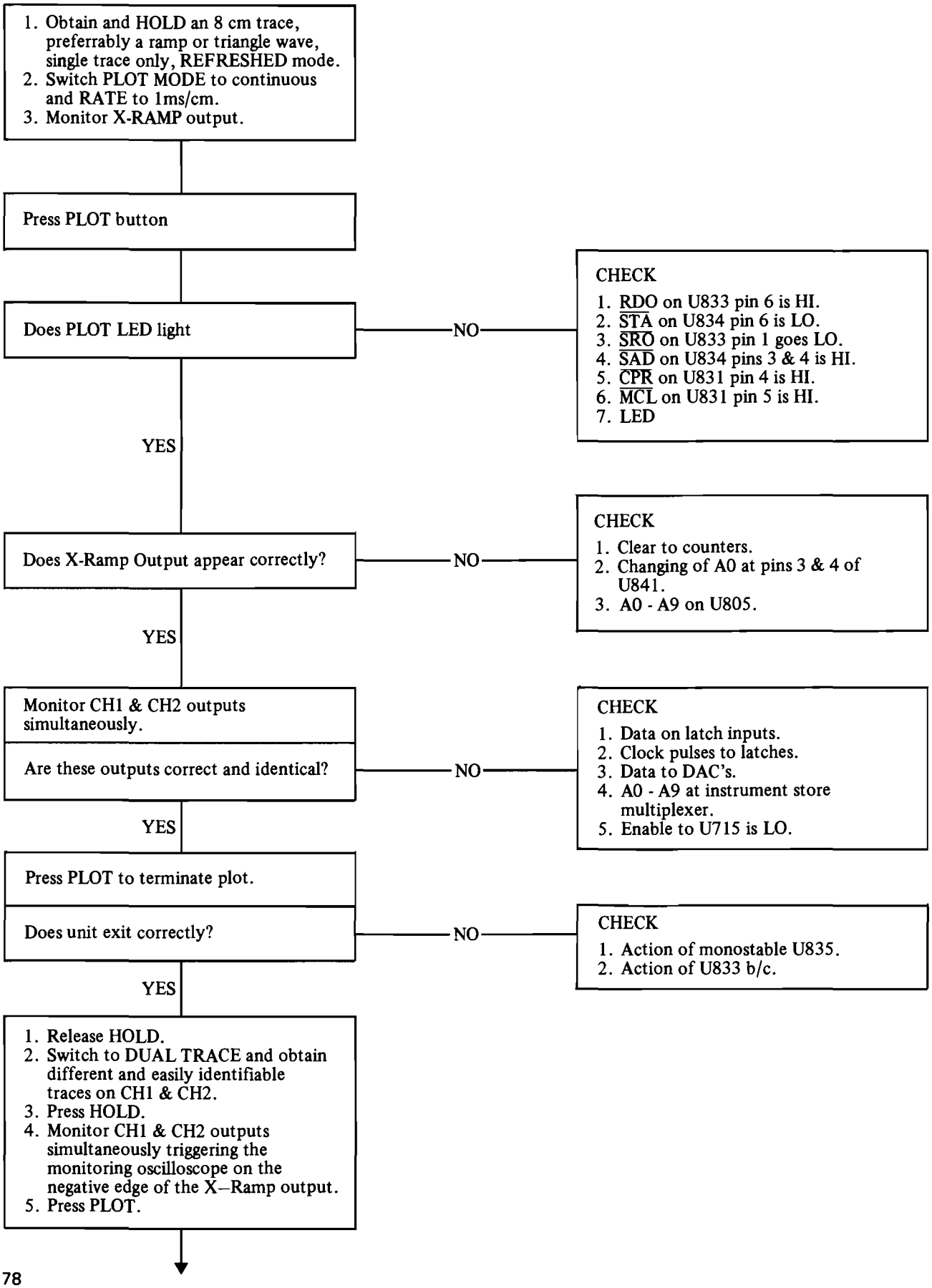
G/ D3 OUTPUT (SK.F PIN 12)

H/ WAVEFORM AT EMITTER OF TR223 OUTPUT OF SECOND SUMMING AMPLIFIER

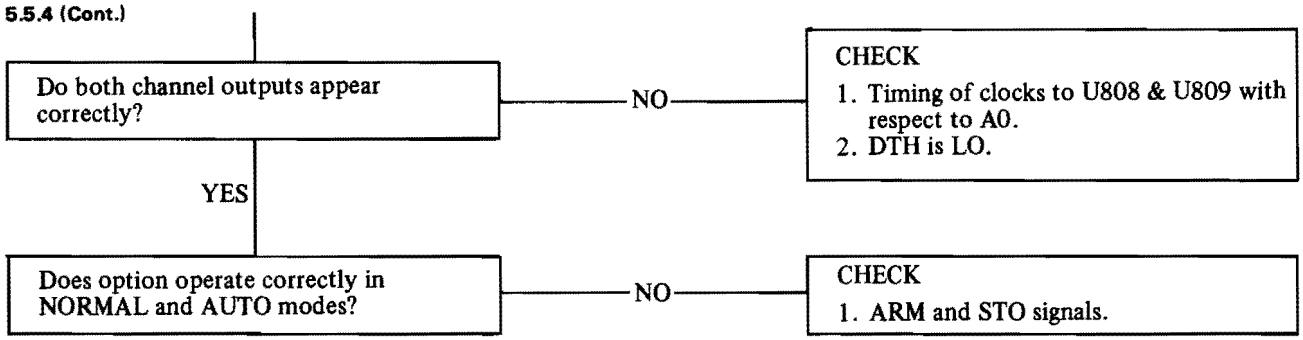
Fig. 5.5 ADC Waveforms

5.5.4 4022 OPTION; FAULT LOCALISATION

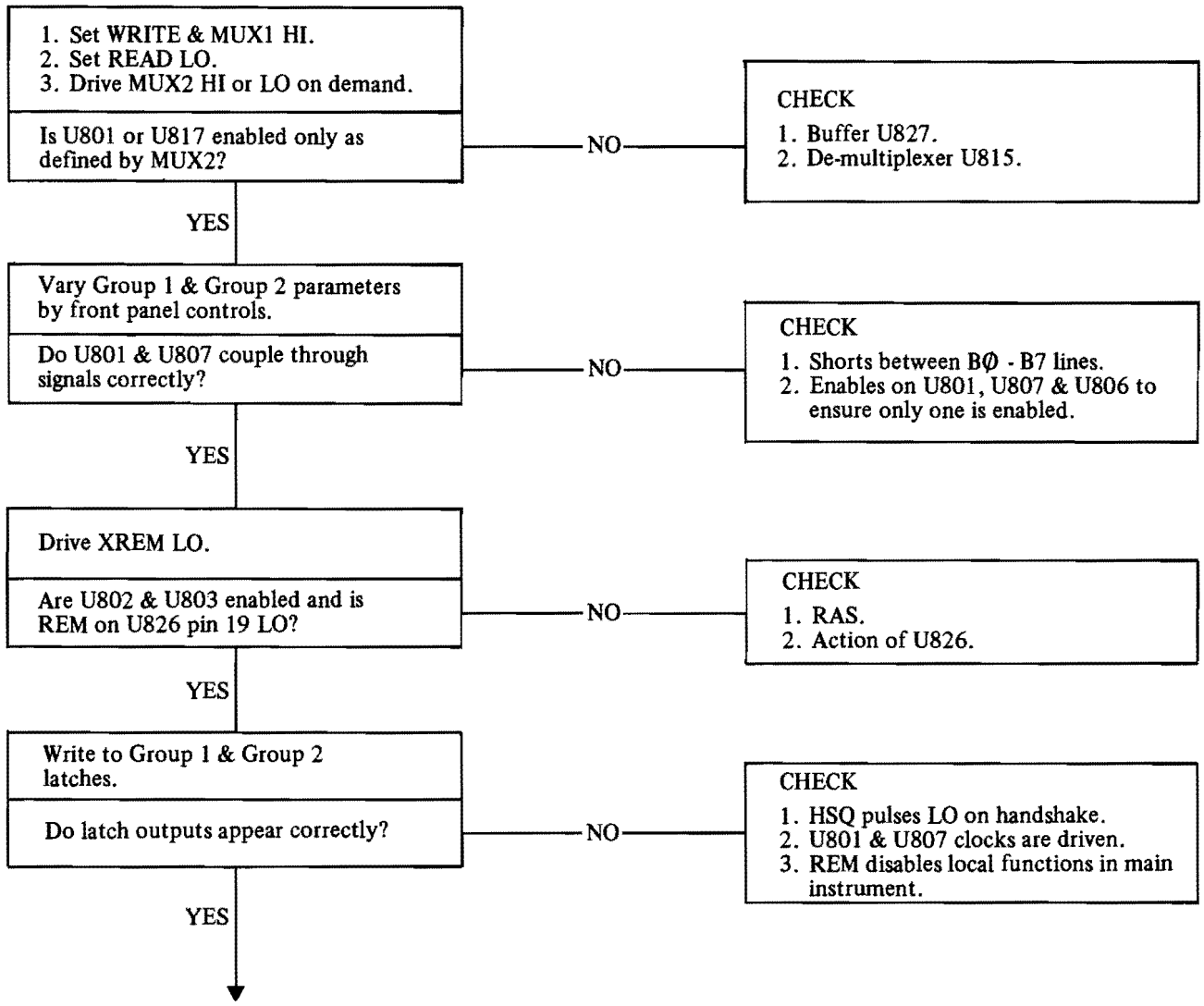
A) ANALOGUE OPTION



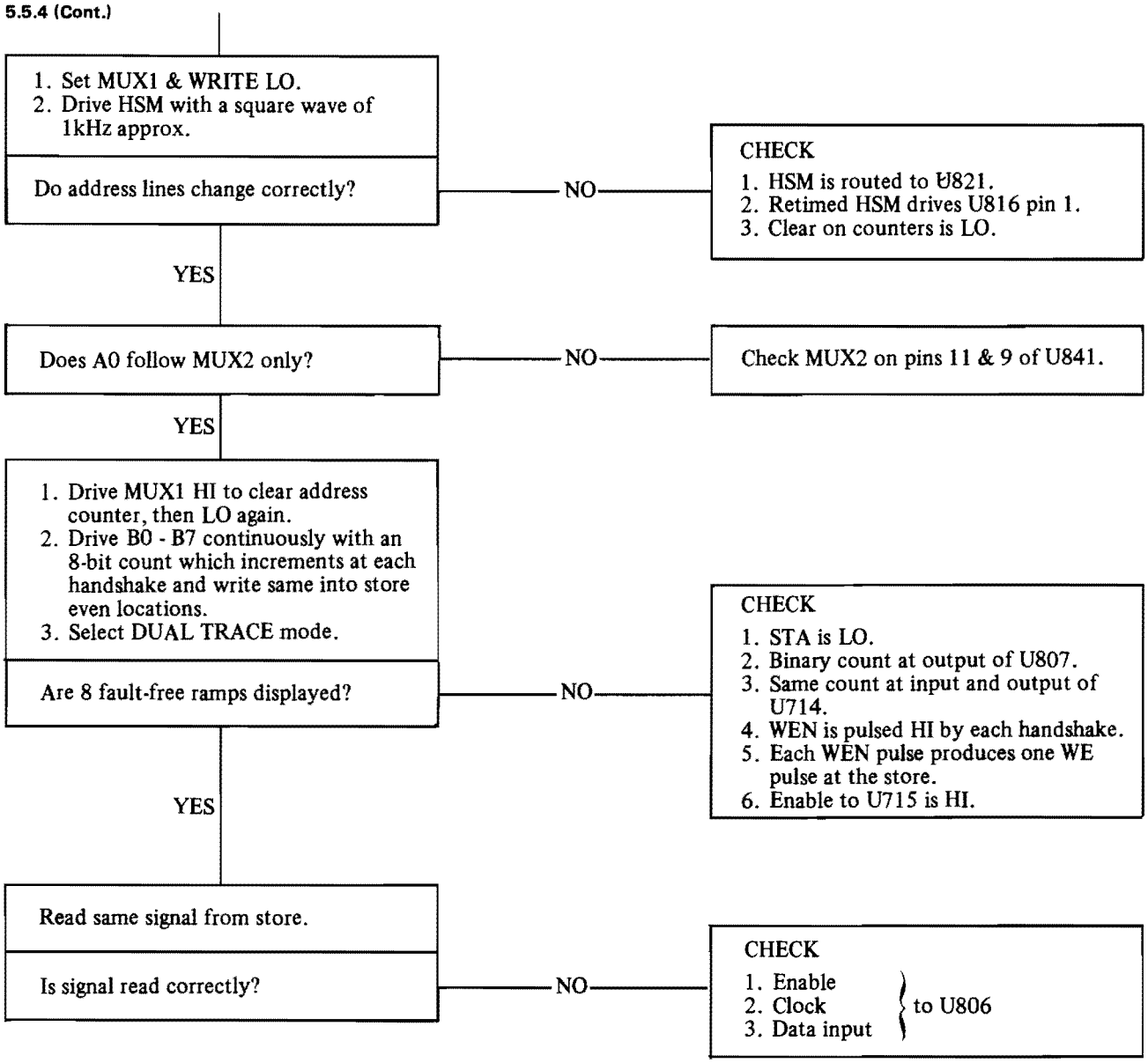
5.5.4 (Cont.)



B) DIGITAL I/O



5.5.4 (Cont.)


1. Set MUX1 & WRITE LO.
2. Drive HSM with a square wave of 1kHz approx.
Do address lines change correctly?
NO
CHECK
1. HSM is routed to U821.
2. Retimed HSM drives U816 pin 1.
3. Clear on counters is LO.
YES
Does A0 follow MUX2 only?
NO
Check MUX2 on pins 11 & 9 of U841.
YES
1. Drive MUX1 HI to clear address counter, then LO again.
2. Drive B0 - B7 continuously with an 8-bit count which increments at each handshake and write same into store even locations.
3. Select DUAL TRACE mode.
Are 8 fault-free ramps displayed?
NO
CHECK
1. STA is LO.
2. Binary count at output of U807.
3. Same count at input and output of U714.
4. WEN is pulsed HI by each handshake.
5. Each WEN pulse produces one WE pulse at the store.
6. Enable to U715 is HI.
YES
Read same signal from store.
Is signal read correctly?
NO
CHECK
1. Enable
2. Clock
3. Data input
to U806

5.6 CIRCUIT VOLTAGES

The following voltages may be used as a general guide during fault finding. All voltages are measured with respect to ground (chassis) with a high input impedence instrument with the supply line voltage at the nominal value set on the SUPPLY VOLTAGE switch. The readings are taken with the front panel controls set as follows unless otherwise indicated:-

INTENSITY, X SHIFT and both Y SHIFT CONTROLS at mid position.
CH1 and CH2 input coupling switches in GND position.
DISPLAY MODE in NORMAL position.
Y MODE in CH1 position.

TIME/CM at 1ms/cm.
X EXPAND in X1 position (fully anti-clockwise).
TRIGGER LEVEL mid position.
BRIGHT LINE OFF.
TRIGGER SOURCE in EXT. position.

Y Pre-Amplifier

D301 Anode	–7.2V
D302 Cathode	+7.2V
TR301 Drain	+10V
TR301 Source	+1.5V
TR303 Collector	0V
TR303 Base	–9.2V
TR302 Drain	–9.8V
TR302 Source	–18.5V
TR305 emitter	–0.7V
TR306	–0.7V
TR307, TR308 collectors	+5.8V
TR309 collector	0V
TR310	+4.2V

Y Output Amplifier

TR408, TR409 bases	+0.7V
TR408 collector	+5.1V
TR409 collector	+4.5V
TR406, TR407 bases	+16V
TR406, TR407 collectors	+17.5V
TR404, TR405 bases	+19.8V
TR404, TR405 collectors (Y plate mean potential)	+109V

Beamswitch and Signal Switch

TR319 collector	+1.9V CH1 selected +0.1V CH2 selected
TR321 base	0V
D317, D318 Anodes	+1.4V (– 0.6V in REFRESHED mode)
D319, D320 Anode	–0.6V (+1.4V in REFRESHED mode)
D323 Anode	–6.4V

ADC: Scaling Amplifier

TR201 base	0V
TR202 collector	+6.5V
TR203 collector	+2.8V
TR204 base	0V
D204 Anode	–6.5V
TR206 base	+2V
TR206 collector	+5.1V

ADC: Sample and Hold

D208 Anode	–12.2V
TR213 Gate	+1.4V
TR213 Source	+2.9V
TR214 Drain	+1.4V
TR214 Source	–4.5V

ADC: Summing Amplifier

IC102 pin 2	+2V
IC102 pin 1	+10.6V
IC102 pin 12	–1.7V

ADC: Current Sources

IC101 pin 3	+3.7V
IC101 pin 4	+7V
IC101 pin 1	+5.3V
TR134 base	+3.9V (D1 high)
or	+0.1V (D1 low)
TR134 collector	+4.7V (D1 high)
or	+6.1V (D1 low)
TR135 collector	+6.0V (D1 high)
or	+5.4V (D1 low)
TR232 emitter	+10.7V

Timebase

TR914 base	0V
TR915, TR916 collectors	+5.5V
TR901, TR902 collectors	+14V
TR903 collector	+18V
TR904 base	+13.7V
TR904 collector	+15.6V
TR905 collector	–19.4V (–20.6 when triggered)
TR909 base	–1.8V (+0.8 when triggered)
TR912 base	+0.8V (–3.4V when triggered)
TR912 collector	+0.2V (+18V when triggered)
TR913 collector	+13.2V (+0.2V when triggered)
TR924 base	+0.6V (plus 11.4V positive going ramp during sweep)
TR924 collector	–4.4V (plus 6V negative going ramp during sweep)
Junction R998/R983	–12.2V
TR927 emitter	+6.4V
TR925, TR926 collectors (X plate mean potential)	+85V

Logic Levels

Inputs: Logic '0' (max.)	+0.8V
Logic '1' (min.)	+2V
Outputs: Logic '0' (max.)	+0.4V
Logic '1' (min.)	+2.4V
Typical Levels: Logic '0'	+0.2V
Logic '1'	+4V

PIN No.	SIGNAL	BOARD SOURCE	MAJOR FUNCTION AT DESTINATION (WHERE APPLICABLE)
1	PTL	TIMING	SELECT SWEEP RATE
2	QTL	TIMING	
3	$\overline{\text{RBC}}$	TIMING	CLEAR RAMP BISTABLE
4	R9	STORE	CALIBRATOR INPUT
5	W11	STORE	TO RESET RFQ
6	$\overline{\text{NORM}}$	TIMING	–
7	N/C	–	–
8	DIG GND	–	–
9	EXC	TIMING	COMMON TO EXPANSION SW.
10	$\overline{\text{BLN}}$	TIMING	BRIGHT LINE INPUT
11	RBQ	TIMEBASE	RAMP BISTABLE OUTPUT
12	RFS	TIMING	REFRESH MODE
13	RFQ	TIMEBASE	HIGH ON TRIG'D SWEEP
14	$\overline{\text{HOC}}$	TIMING	HOLD off BISTABLE CLEAR
15	HOS	TIMING	SET
16	RAMP START	STORE	–

Fig. 5.6 Connections to SKM/N

PIN No.	SIGNAL	BOARD SOURCE (T)IMING (S)TORE	MAJOR FUNCTION AT DESTINATION (WHERE APPLICABLE)
1	R1	(S)	ANALOGUE CHOP
2	WØ	(S)	–
3	W11	(S)	WRITE STOP
4	R1Ø	(S)	TRIG. PT. BRIGHT-UP
5	R11	(S)	TRIG. PT. BRIGHT-UP
6	$\overline{\text{MCL}}$	(S)	ROLL COUNTER CLEAR
7	DHO	(S)	–
8	0V	(S)	–
9	0V	(S)	–
10	+12V	(S)	–
11	Drive to UNCAL LED	(T)	–
12	DTH	(T)	–
13	PON	(S)	PRODUCE $\overline{\text{MCL}}$
14	FLASH	(S)	–
15	+5V	(S)	–
16	+5V	(S)	–

Fig. 5.7 Connections to SKAW

PIN No.	SIGNAL	BOARD SOURCE (S)TORE/(T)IMING	MAJOR FUNCTION AT DESTINATION (WHERE APPLICABLE)
1	RO′	(T)	MODIFIED LEAST SIG. READ ADDRESS BIT
2	RAMP B/S CLEAR	(S)	–
3	R9	(S)	CALIBRATOR DRIVE
4	RCK	(T)	READ COUNTER CLOCK
5	$\overline{R2}$	(S)	START DISPLAY SWEEP
6	0V	(S)	–
7	0V	(S)	–
8	0V	(S)	–
9	$\overline{SWA}$	(T)	DRIVE TO READ/WRITE ADDRESS MULTIPLEXER
10	$\overline{WE}$	(T)	WRITE ENABLE TO STORES
11	$\overline{NORM}$	(T)	DISABLE DIGITAL END SWEEP
12	P3	(T)	–
13	CH2/$\overline{CH1}$	(T)	BEAMSWITCH SIGNAL
14	CK	(T)	
15	P2	(T)	
16	P5	(T)	

Fig. 5.8 Connections to SKAX

PIN No.	SIGNAL	BOARD SOURCE (S)TORE/(T)IMING	MAJOR FUNCTION AT DESTINATION (WHERE APPLICABLE)
1	$\overline{HLD}$	(S)	–
2	$\overline{SRO}$	(S)	START PLOT
3	N/C	–	–
4	WCK	(T)	CLOCK TO WRITE COUNTER
5	WLC	(T)	CLEAR WRITE ADDRESS LATCH
6	Drive to ARM LED	(T)	–
7	Drive to TRIG'D LED	(T)	–
8	Drive to STORED LED	(T)	–
9	$\overline{DTH}$	(T)	MODIFY LATCHED WRITE LSB
10	RØ	(S)	FOR MODIFICATION
11	LDO	(T)	CLOCK TO LATCH DATA FROM STORE OUTPUT
12	L14	–	WIPER OF EXPANSION SWITCH
13	L2	–	
14	L15	(T)	EXPANSION SWITCH
15	L1	–	
16	GATED P4	(T)	DOT JOINER S/H DRIVE

Fig. 5.9 Connections to SKAY

PIN No.	SIGNAL	BOARD SOURCE (S)TORE (T)IMING	MAJOR FUNCTION AT DESTINATION (WHERE APPLICABLE)
1	RES	(T)	GATED FOR $\overline{MCL}$
2	RAS	(T)	DRIVE TO READ/ 4022 ADDRESS MUX
3	–	(S)	SINGLE SHOT RELEASE
4	–	(T)	LOCAL ARM DISABLE
5	ARM	(S)	START SINGLE SHOT
6	0V	–	–
7	0V	–	–
8	0V	–	–
9	$\overline{P1}$	(T)	CK TO STORE I/P LATCH
10	N/C	–	–
11	STA	(T)	DRIVE TO PLOT LED
12	XARM	–	EXTERNAL ARM
13	REM2	(T)	CONVERT ARM TO EXT
14	$\overline{REM}$	–	–
15	HHD	(S)	–
16	WCC	(T)	WRITE COUNTER CLEAR

Fig. 5.10 Connections to SKAZ

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	¼W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potenitometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
CE(3)	Ceramic	50V		unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

0S4020 CH1 & CH2 PRE-AMP

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R301	470	CF		21797
R302	3k3	CF	½W	18556
R303	470	CF		21797
R304	22k	CF		21812
R305	22k	CF		21812
R306	27k	CF		21813
R307	470	CF		21797
R308	470	CF		21797
R309	6k8	CF		21807
R310	6k8	CF		21807
R311	1k8	CF		28725
R312	1k5	CF		21801
R313	1k5	CF		21801
R314	1k8	CF		28725
R315	47	CF		28714
R316	47	CF		28714
R317	2k2	CF		21802
R318	2k2	CF		21802
R319	100	CP		35878
R320	100	CF		21794
R349	47	CF		28714
R350	47	CF		28714
R351	10k1	MF	½	31928
R352	10k1	MF	½	31928
R353	15k	CF		28727
R354	15k	CF		28727
R355	100	CF		21794
R357	10	CF		21793
R358	10	CF		21793
R359	56	CF		28715
R360	2k7	CF		28726
R361	10k	CF		21809
R362	2k7	CF		28726
R363	6k8	CF		21807
R365	5k6	CF		21806
R366	5k6	CF		21806
R367	3k9	CF		21804
R368	3k9	CF		21804
R369	1k	CP		35880
R370	1k	CP		35880
R371	22	CF		28710
R372	22	CF		28710
R373	22k	PCP		A3/35339
R374	22k	PCP		A3/35339
R375	1k	CF		21799
R376	1k	CF		21799
R377	1k	PCP		35880
R378	1k5	CF		21801
R379	47	CF		28714
R380	3k9	CF		21804
R381	47	CF		28714
R382	47	CF		28714
R383	1k5	CF		21801
R384	1k5	CF		21801
R385	5k6	CF		21806
R386	5k6	CF		21806
R387	6k8	CF		21807
R388	6k8	CF		21807
R389	330	CF		28721
R390	1k8	CF		28725
R391	1k3	MO		28792
R392	10k	CF		21809
R393	10k	CF		21809
R394	1k1	MO		28791
R395	1k1	MO		28791
R396	390	CF		28722
R397	390	CF		28722
R398	3k9	CF		21804
R399	100	CF		21794
CAPACITORS				
C301	16pF	TRIMMER		32059
C302	16pF	TRIMMER		32059
C303	16pF	TRIMMER		32059
C304	16pF	TRIMMER		32059
C305	6pF	TRIMMER		29421
C306	6pF	TRIMMER		29421
C307	.01µF	CE(2)	250V	22395
C308	.01µF	CE(2)	250V	22395
C309	47pF	CE(2)		22372
C310	47nF	CE(2)	50V	43497
C311	12pF	CE(2)		22365
C312	22µF	E	25V	32181
C313	15µF	E	63V	32197
C314	15µF	E	63V	32197
C315	120pF	CE(2)		22377
C316	120pF	CE(2)		22377
C317	470pF	PS		11492
C318	470pF	PS		11492
C319	18pF	CE(2)		22367
C320	18pF	CE(2)		22367
C321	1000pF	CE(2)		22387
C323	1000pF	CE(2)		22387
C324	1000pF	CE(2)		22387
C325	.1µF	CE(2)	25V	36709
C326	.1µF	CE(2)	25V	36709
C327	0.01µF	CE(2)	250V	22395
C328				
C329				
C330	27pF	CE(2)		22369
TRANSISTORS				
TR301 } TR302 }		AE31	DUAL FET	A36243
TR303		BC209C		33331
TR304		2N3906		21533
TR305 } TR306 }		AE13	MATCHED PAIR	A31254

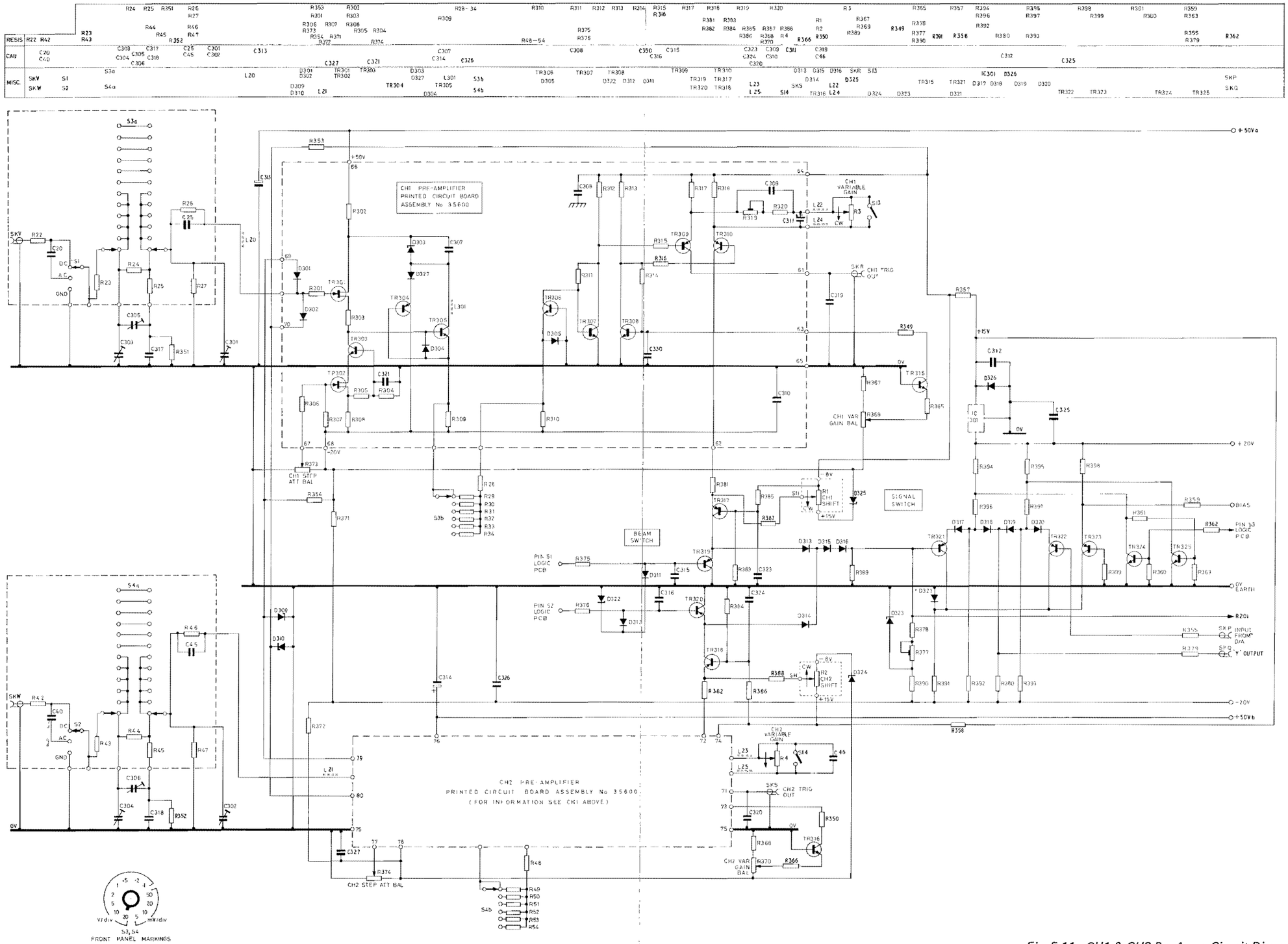


Fig. 5.11 CH1 & CH2 Pre-Amps Circuit Diagram

0S4020 ANALOGUE TO DIGITAL CONVERTER

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R101	10	CF		21793
R102	390	CF		28722
R103	10	CF		21793
R104	1k2	CF		21800
R105	820	CF		28724
R106	1k	CP		35875
R107	47	MO		26748
R108			A.O.T.	
R110	696R5	MF	.25	35874
R111	330	CF		28721
R113	12k	CF		21810
R114	1k	CP		35875
R115	6k8	MF		37007
R116	1k2	CF		21800
R118			A.O.T.	
R119			A.O.T.	
R120	12k	CF		21810
R121	1k2	CF		21800
R122	1k	CP		35875
R123	13k3	MF		37008
R124	220	CP		35877
R125	1k	MF		36032
R126	330	CF		28721
R127	12k	CF		21810
R128	6k96	MF		35867
R129	47	CF		28714
R130	1k2	CF		21800
R131	12k	CF		21810
R133	13k9	MF		35868
R134	1k2	CF		21800
R135	12k	CF		21810
R137	27k8	MF		35871
R138	1k2	CF		21800
R139	8k9	MF		35869
R140	5k6	CF		21806
R141	5k6	CF		21806
R142	5k6	CF		21806
R143	47	CF		28714
R144	47	CF		28714
R145	47	CF		28714
R146	10	MF		27314
R147	10	MF		27314
R148	10	MF		27314
R149	10	MF		27314
R150	10	MF		27314
R151	10	MF		27314
R152	10	MF		27314
R156	47	CF		28714
R157	47	CF		28714
R158	47	CF		28714
R159	47	CF		28714
R160	5k6	CF		21806
R161	5k6	CF		21806
R162	5k6	CF		21806
R163			A.O.T.	
R172	1k	CF		21799
R173	1k	CF		21799
R181	2k2	CF		21802
R183	2k2	CF		21802
R184	1k	CF		21799
R185	1k5	CF		21801
R186	220	CF		21796
R201	47	CF		28714
R202	3k9	CF		21804
R203	1k2	CF		21800
R204	3k9	CF		21804
R205	2k7	CF		28726
R206	4k7	CF		21805
R207	100	CF		21794
R208	220	CP		35881
R209	2k7	CF		28726
R210	1k3	CF	½W	28792
R211	2k2	CF		21802
R212	1k	CF		21799
R213	47	CF		28714
R214	22	CF		28710
R215	22	CF		28710
R216	22	CF		28710
R217	4k7	CP		35879
R218	6k8	CF		21807
R219	5k6	CF		21806
R220	3k9	CF		21804
R221	470	CF		18546
R222	2k2	CF		21802
R223	3k9	CF		21804
R224	10k	CF		21809
R225	3k9	CF		21804
R226	1k	CF		21799
R227	47	CF		28714
R228	22	CF		28710
R229	470	CF		21797
R230	22	CF		28710
R231	470	CF		21797
R232	680	CF		28723
R233	100	CF		21794
R234	1k	CF		21799
R235	2k2	CF		21802
R236	100	CF		21794
R237	68	CF		28716
R239	47	CF		28714
R240	1k	CF		21799
R241	1k8	CF		28725

OS4020 CH1 & CH2 PRE-AMP (Cont.)

Ref	Value	Description	Tol % ±	Part No
TRANSISTORS (Cont.)				
TR307		AE13	MATCHED	A31254
TR308			PAIR	
TR309		2N3640		31781
TR310		2N3640		31781
TR315		2N3904		24146
TR316		2N3904		24146
TR317		BC212		29327
TR318		BC212		29327
TR319		2N3640		31781
TR320		2N3640		31781
TR321		2N3906		21533
TR322		2N3906		21533
TR323		2N3906		21533
TR324		2N3904		24146
TR325		2N3904		24146
DIODES				
D301		IN3595		29330
D302		IN3595		29330
D303		ZENER	10V	33935
D304		IN4148		23802
D305		IN4148		23802
D309		ZENER	7V5	22173
D310		ZENER	7V5	22173
D311		IN4148		23802
D312		IN4148		23802
D313		IN4148		23802
D314		IN4148		23802
D315		IN4148		23802
D316		IN4148		23802
D317		IN4148		34701
D318		IN4148		34701
D319		IN4148		34701
D320		IN4148		34701
D321		IN4148		23802
D322		ZENER	2V7	33921
D323		ZENER	6V2	33930
D324		ZENER	12V	33937
D325		ZENER	12V	33937
D326		IN4148		23802
D327		IN4148		23802
MISCELLANEOUS				
L301		Ferrite Bead		26986
IC301		78L15AWC		36092
SKP				36105
SKQ				36105
SKR				36105
SKS				36105

OS4020 ANALOGUE TO DIGITAL CONVERTER (Cont.)

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont.)				
R242	4k7	CF		21805
R243	22	CF		28710
R244	680	CF		28723
R245	22	CF		28710
R246	330	CF		28721
R247	22	CF		28710
R248	47	CF		28714
R249	1k	MF		36032
R250	1k	CF		21799
R252	270	CF		28720
R253	330	CF		28721
R254	22	CF		28710
R255	47	CF		28714
R256	250	MF		35870
R257	1k	CF		21799
R258	680	CF		28723
R259	22	CF		28710
R260	1k8	CF		28725
R261	4k7	CF		21805
R262	22	CF		28710
R263	27	CF		28711
R264	680	CF	½W	18548
R265	1k	CF		21799
R266	50	MF	.25	35866
R267	50	MF	.25	35866
R268	50	MF	.25	35866
R269	47	CF		28714
R270	47	CF		28714
R271	47	CF		28714
R272	68	CF		28716
R273	2k2	CF		21802
R274	27	CF		28711
R275	5k6	CF		21806
R276	5k6	CF		21806
R277	5k6	CF		21806
R278	10	MF		27314
R279	10	MF		27314
R280	10	MF		27314
R281	10	MF		27314
R282	10	MF		27314
R283	10	MF		27314
R284	10	MF		27314
R285	47	CF		28714
R286	47	CF		28714
R287	47	CF		28714
R288	47	CF		28714
R289			A.O.T.	
R290	100	CF		21794
R291	100	CF		21794
R292	2k7	CF		28726
R293	47	CF		28714
R294	47	CF		28714
R295	47	CF		28714
R296			A.O.T.	
R297			A.O.T.	
R298	100	CF		21794
RN171		Resistor Network		43748
CAPACITORS				
C201	.01μF	CE(2)	250V	22395
C202	22μF	E	25V	32181
C203	.01μF	CE(2)	250V	22395
C204	.1μF	CE(1)	25V	36709
C205	.1μF	CE(1)	25V	36709
C206	12pF	CE(2)	A.O.T.	22365
C207	5.6pF	CE(2)		22361
C208	.1μF	CE(1)	25V	36709
C209	22μF	E	25V	32181
C210	150pF	PC	500V	35913
C211	5.6pF	CE(2)		22361
C212	22pF	CE(2)		22368
C213	10pF	CE(2)		22364
C214	27pF	CE(2)		22369
C215	.1μF	CE(1)	25V	36709
C216	12pF	CE(2)		22365
C218	.1μF	CE(1)	25V	36709
C219	.1μF	CE(1)	25V	36709
C220	.1μF	CE(1)	25V	36709
C221	5.6pF	CE(2)		22361
C222	10pF	CE(2)		22364
C223	39pF	CE(2)		22371
C224	33pF	CE(2)		22370
C225	.1μF	CE(1)	25V	36709
C226	.1μF	CE(1)	25V	36709
C227	5.6pF	CE(2)		22361
C228	39pF	CE(2)		22371
C229	390pF	CE(2)		22382
C230	150pF	CE(2)		22378
C231	150pF	CE(2)		22378
C233	22pF	CE(2)		22368
C234	.01μF	CE(2)	250V	22395
C235	.1μF	CE(1)	25V	36709
C238	.01μF	CE(2)	250V	22395
C239	330pF	CE(2)		22381
C240	22μF	E	25V	32181
C241	4.7μF	E	63V	32195
C242	.01μF	CE(2)	250V	22395
C243	.01μF	CE(2)	250V	22395
C244	.01μF	CE(2)	250V	22395
C245	.1μF	CE(1)	25V	36709
C246	.1μF	CE(1)	25V	36709
C247	1000pF	CE(2)		22387
C248	330pF	CE(2)		22381
C249	.01μF	CE(2)	250V	22395
C250	22pF	CE(2)		22368
C260	.1μF	CE(1)	25V	36709

OS4020 ANALOGUE TO DIGITAL CONVERTER (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont.)				
C261	22µF	E	25V	32181
C262	.1µF	CE(1)	30V	19647
C263	.01µF	CE(2)	250V	22395
C264	.01µF	CE(2)	250V	22395
C265	.1µF	CE(1)	25V	36709
C266	.1µF	CE(1)	25V	36709
C267	.1µF	CE(1)	25V	36709
C268	.1µF	CE(1)	25V	36709
C271	.047µF	CE(3)		43497
C272	.047µF	CE(3)		43497
C273	.047µF	CE(3)		43497
C274	.047µF	CE(3)		43497
C275	22µF	E	25V	32181
C276	120pF	CE(3)		42421
C277	120pF	CE(3)		42421
C278	22pF	CE(3)		42412
C279			A.O.T.	
C280	.047µF	CE(3)		43497
C281	15pF	CE(2)		42410
INTEGRATED CIRCUITS				
IC101		723		31228
IC102		CA3046		36632
IC111		TY38111		36928
IC112		TY38111		36928
IC113		TY38111		36928
IC114		TY38111		36928
IC115		TY38111		36928
IC116		TY38111		36928
IC117		TY38111		36928
IC118		TY38111		36928
IC119		TY38111		36928
IC120		7475		31834
IC121		7400		52038
IC122		7400		52038
IC123		74S74		36005
IC124		74S74		36005
IC125		7420		52039
IC126		7408		53688
IC127		7403	Restricted Manufacturer	37853
IC128		7404		31836
IC129		7400		52038
IC130		74S74		36005
IC131		74S74		36005
IC132		7400		52038
TRANSISTORS				
TR132		BC212		29327
TR133		BC107		26790
TR134		2N2369		23307
TR135		2N2369		23307
TR136		2N3906		21533
TR137		2N2369		23307
TR138		2N2369		23307
TR139		2N3906		21533
TR140		BC107		26790
TR141		2N3906		21533
TR142		2N2369		23307
TR143		2N2369		23307
TR144		2N3906		21533
TR145		2N2369		23307
TR146		2N2369		23307
TR147		2N3906		21533
TR148		2N2369		23307
TR149		2N2369		23307
TR150		2N3906		21533
TR151		2N3906		21533
TR201		2N2369		23307
TR202		2N2369		23307
TR203		2N2369		23307
TR204		2N2369		23307
TR205		2N2369		23307
TR206		2N2369		23307
TR207		2N2369		23307
TR208		E111		36028
TR209		2N2369		23307
TR210		2N2369		23307
TR211		E111		36028
TR212		2N2369		23307
TR213 / TR214		AE23	Matched pair	A32957
TR215		AE16		21533
TR219		2N3640		31781
TR221		BFY 90		26987
TR223		BFY 90		26987
TR224		2N3640		31781
TR225		2N2369		23307
TR226		2N2369		23307
TR227		2N2369		23307
TR231		BC182B		33205
TR232		BFY 51		29329
DIODES				
D101		IN4148		23802
D102		IN4148		23802
D103		IN4148		23802
D104		IN4148		23802
D105		IN4148		23802
D201		IN4148		34701
D202	5V1	ZENER		33928
D203	3V9	ZENER		33925
D204	6V2	ZENER		33930
D205		IN4148		34701
D206		IN4148		34701

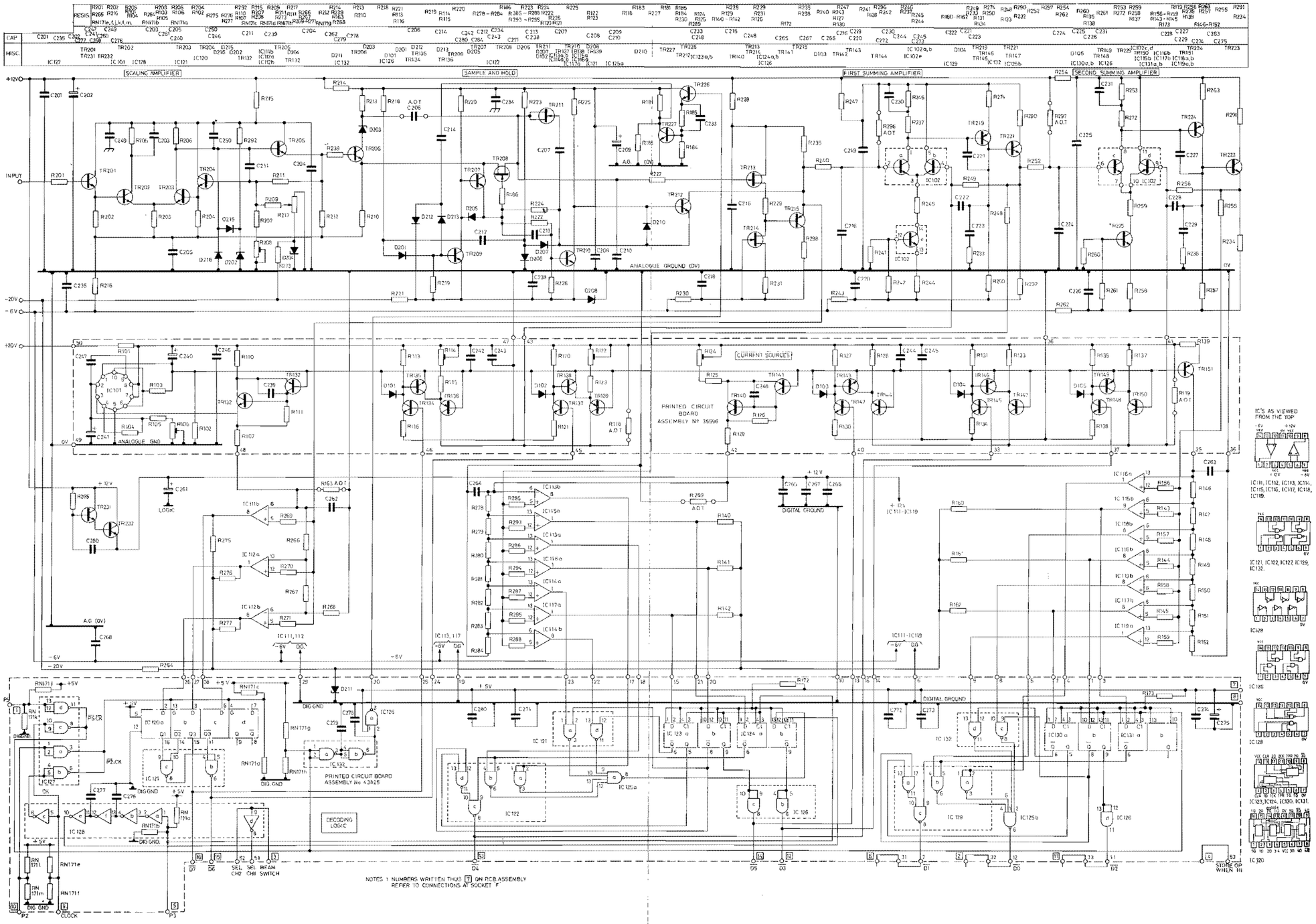


Fig. 5.12 Analogue to Digital Convertor Circuit Diagram

OS4020 TIMING LOGIC

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R601	4k7	CF		21805
R602	4k7	CF		21805
R603	4k7	CF		21805
R604	4k7	CF		21805
R605	4k7	CF		21805
R606	1k	CF		21799
R607	6k8	CF		21807
R608	3k3	CF		21803
R609	470	CF		21797
R610	2k2	CF		21802
R611	3k9	CF		21804
R612	4k7	CF		21805
R613	220	CF		21796
R614	47	CF		28714
R615	390	CF		28722
R616	390	CF		28722
R617	390	CF		28722
R618	4k7	CF		21805
R619	4k7	CF		21805
R620	4k7	CF		21805
R621	4k7	CF		21805
R622	4k7	CF		21805
R623	4k7	CF		21805
R624	4k7	CF		21805
R625	4k7	CF		21805
R626	47k	CF		21815
R627	330	CF		28721
R628	4k7	CF		21805
R629	4k7	CF		21805
R630	4k7	CF		21805
R631	4k7	CF		21805
R632	100k	CF		21819
R633	4k7	CF		21805
RN601	4k7	Resistor Network		40177
CAPACITORS				
C601	.01μF	CE(3)		42444
C602	.01μF	CE(3)		42444
C603	47μF	T	16V	39215
C604	.01μF	CE(3)		42444
C605	.01μF	CE(3)		42444
C606	22pF	PS	63V	35908
C607	15pF	TRIMMER		36227
C608	.10μF	CE(3)		43498
C609	.01μF	CE(3)		42444
C610	.01μF	CE(3)		42444
C611	.01μF	CE(3)		42444
C612	.01μF	CE(3)		42444
C613	.01μF	CE(3)		42444
C614	.01μF	CE(3)		42444
C615	.01μF	CE(3)		42444
C616	.01μF	CE(3)		42444
C617	.01μF	CE(3)		42444
C618	.01μF	CE(3)		42444
C619	100pF	CE(3)		42420
C620	100pF	CE(3)		42420
C621	.01μF	CE(3)		42444
C622	10μF	T	35V	35931
C623	.01μF	CE(3)		42444
C624	47μF	T	16V	39215
C625	2.2μF	T	35V	35930
C626	680pF	CE(3)		42430
Q601		2N3640		31781
Q602		2N3640		31781
Q603		2N2369		23307
DIODES				
D601		0A47		4468
D602		0A47		4468
D603		OA47		4468
D604		OA47		4468
D605		LED		43847
D606		LED		43847
D607		LED		43847
U601		74LS390		43675
U602		74LS151		41085
U603		74LS05		36879
U604		74LS30		41078
U605		74LS10		36867
U606		74LS390		43675
U607		74LS155		43672
U608		74LS03		38307
U609		74LS390		43675
U610		74LS02		41075
U611		74LS04		36731
U612		7407		43674
U613		74LS20		39236
U614		74LS86		38421
U615		74LS74		36732
U616		74LS153		36247
U617		74LS74		36732
U618		74LS175		36728
U619		74LS20		39236
U620		74LS74		36732
U621		74LS02		41075
U622		74LS112		36468
U623		74LS55		43670
U624		74LS00		36730
U625		74LS02		41075
U626		74LS51		43676
U627		74LS04		36731
U628		74LS02		41075
U629		74LS74		36732
U630		7405		53637
U631		74LS74		36732
U632		74LS00		36730

OS4020 ANALOGUE TO DIGITAL CONVERTER (Cont.)

Ref	*Value*	*Description*	*Tol %±*	*Part No*	*Ref*	*Value*	*Description*	*Tol %±*	*Part No*
DIODES (Cont.)									
D207		IN4148		34701	D212		IN4148		34701
D208	12V	ZENER		33937	D213		IN4148		34701
D210		IN4148		34701	D215		IN4148		23802
D211	6V2	ZENER		33930	D216		IN4148		23802

NOTES

1. ASTERISK INDICATES OPEN COLLECTOR DEVICES.

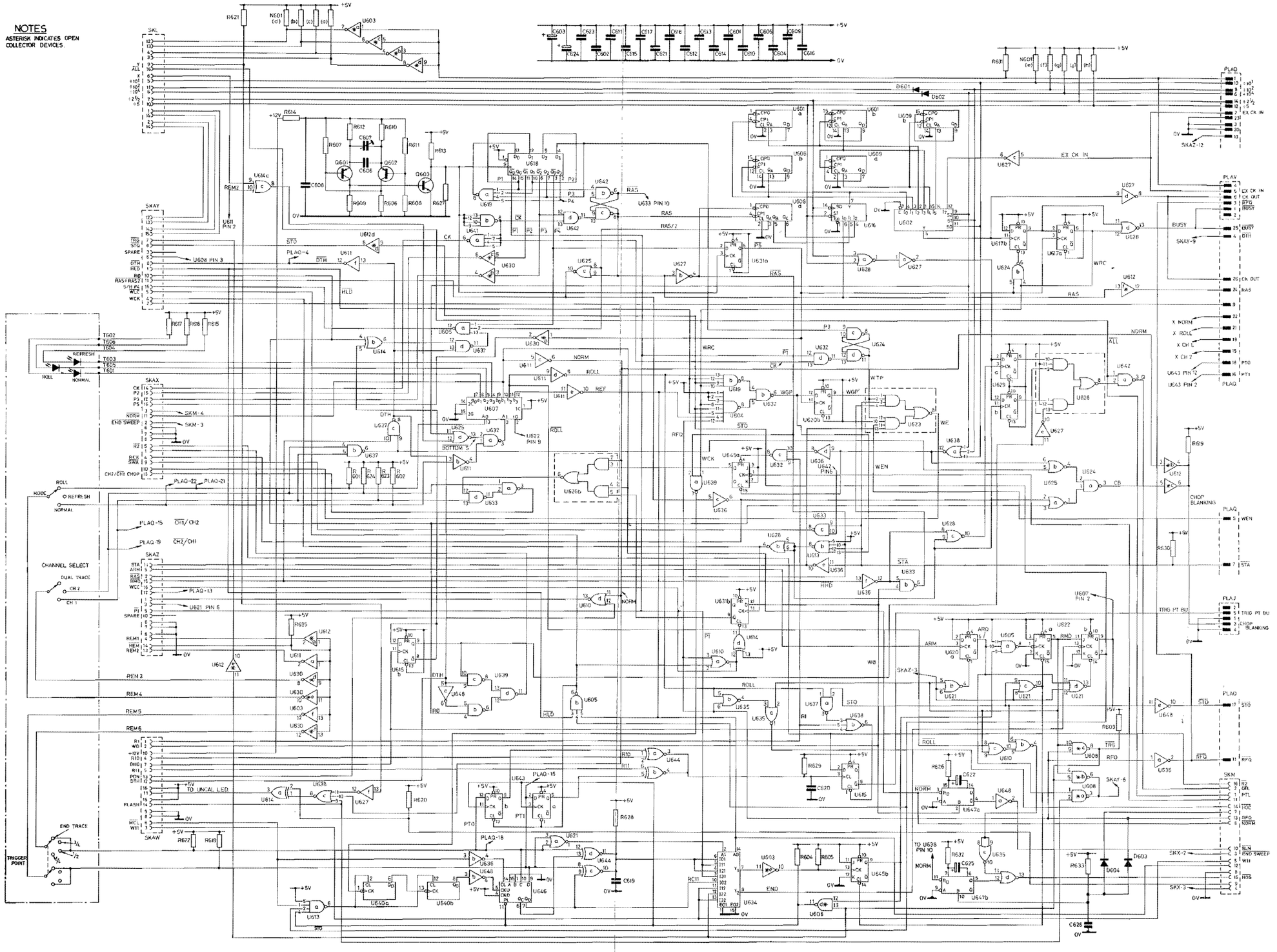


Fig. 5.13 Timing Logic Circuit Diagram

OS4020 TIMING LOGIC (Cont.)

Ref	*Value*	*Description*	*Tol % ±*	*Part No*
U633		74LS00		36730
U634		74LS153		36247
U635		74LS02		41075
U636		74LS04		36731
U637		74LS00		36730
U638		74LS27		41077
U639		74LS00		36730
U640		74LS393		41090
U641		7440		52040
U642		74LS00		36730
U643		74LS74		36732
U644		74LS266		42660
U645		74LS112		36468
U646		74LS193		43668
U647		74LS123		41084
U648		74LS04		36731

MISCELLANEOUS

Ref	*Value*	*Description*	*Tol % ±*	*Part No*
S601				35344
S602				35344
S603				35343
SKJ				41610
SKL				38001
SKV				41607
SKAQ				43832
SKAW				38001
SKAX				38001
SKAY				38001
SKAZ				38001

RESIST.	R706 R702 R703 R704 R701 R705 R775 R710 R715 R707 R711 R708 R709 R712 R777 R722 R713 R720 R716 R717 R714 R718 R719 R723 R730 R726 R721 R727 R725 R724 R740 R728 R729 R731 R732 R741 R734 R776 R736 R737 R735 R742 R739 R733 R738
CAP.	C701 C702 C703 C704 C710 C711 C705 C708 C706 C707 C714 C709 C712 C718 C713 C715 C716 C720 C719 C717 C721
MISC.	U701 D701 D720 D706 U702 D703 Q705 Q701 D704 Q703 Q702 D702 Q706 D705 Q707 D707 Q704 Q708 D709 D708 D711 Q709 U703 D712 D713 D710 L701

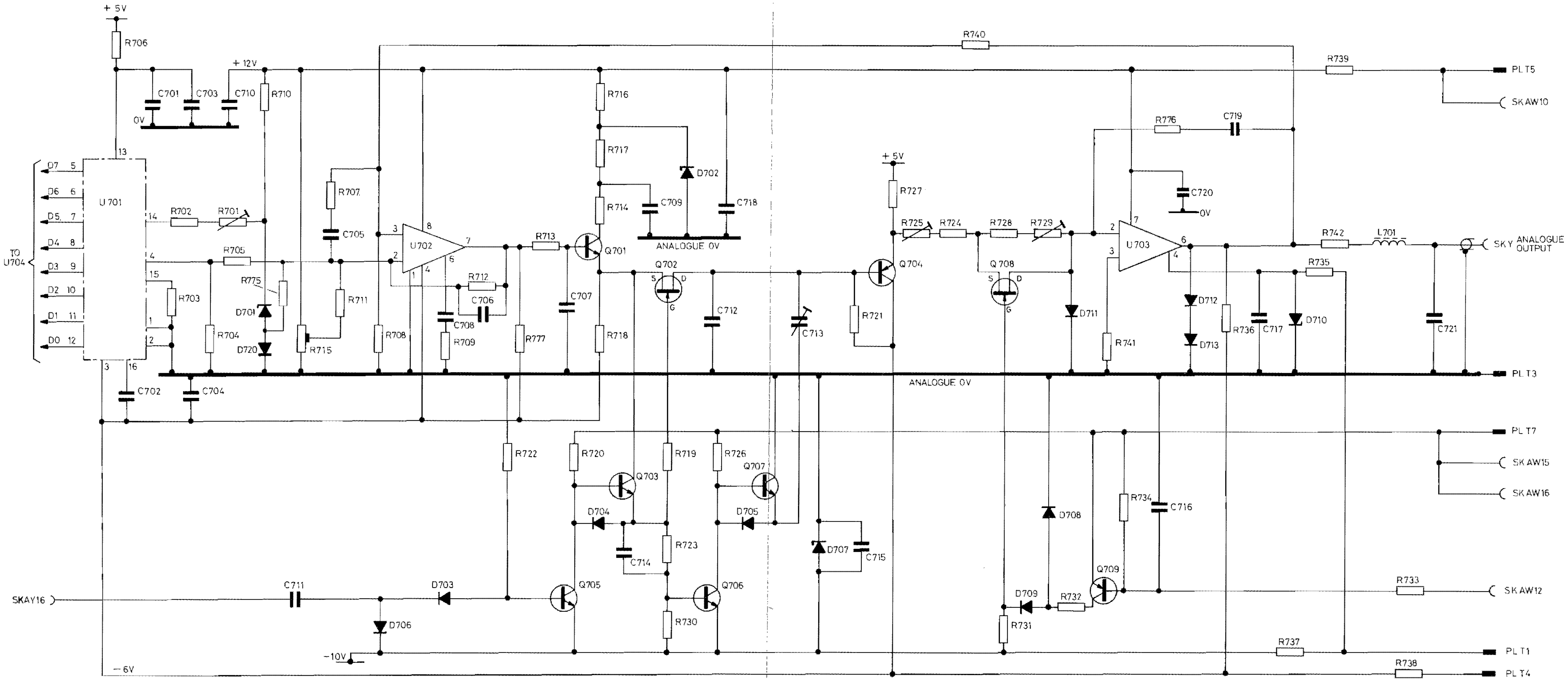
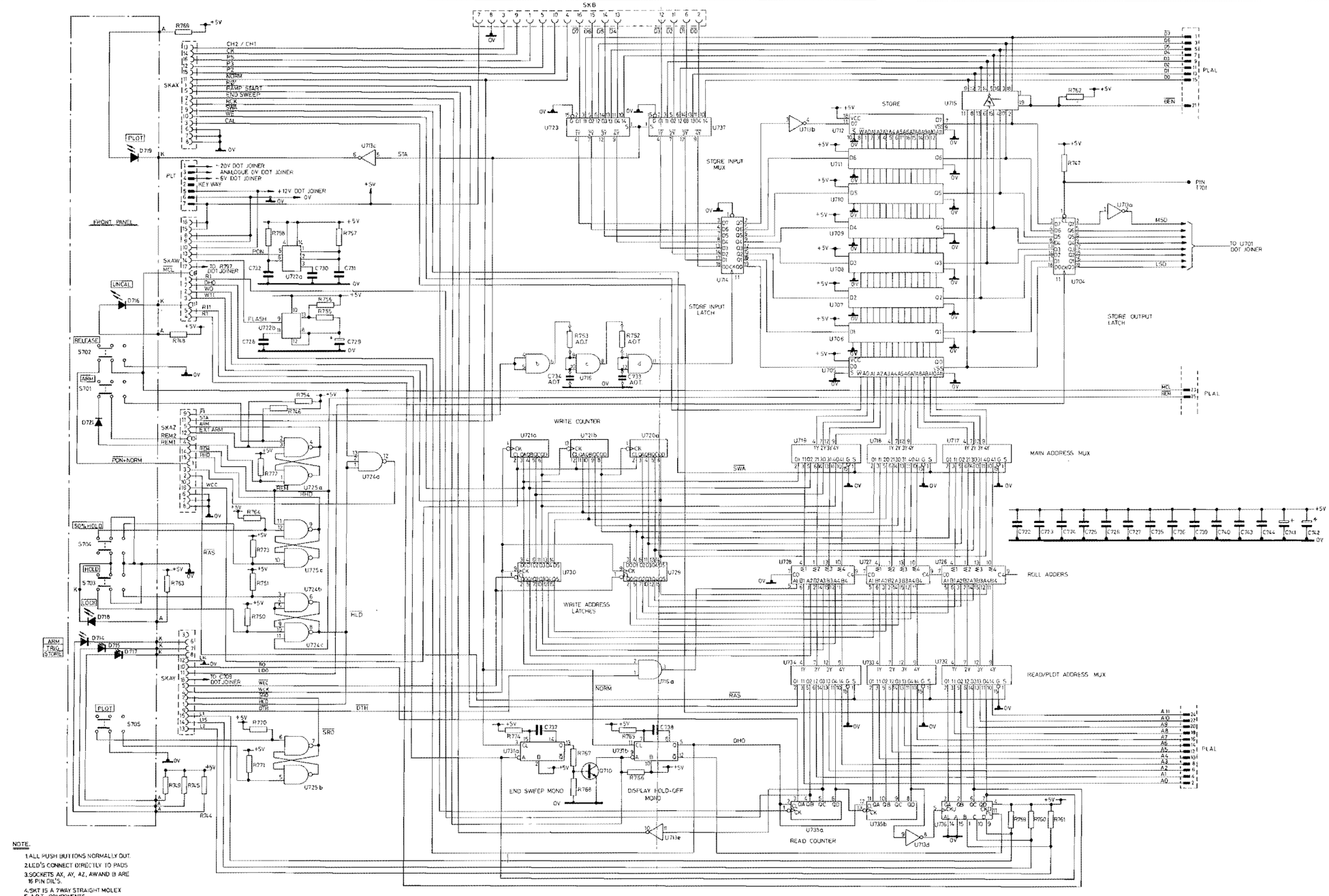


Fig. 5.14 Dot Joiner and Store Logic Circuit Diagram

OS4020 DOT JOINER & STORE LOGIC

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R701	1k	CP		35875
R702	2k2	CF		21802
R703	3k3	CF		21803
R704	82	MF		36033
R705	56	MF		36034
R706	10	CF		21793
R707	220	CF		21796
R708	1k	CF		21799
R709	220	CF		21796
R710	1k	MF		36032
R711	6k8	CF		21807
R712	1k	MF		36032
R713	100	CF		21794
R714	10	CF		21793
R715	10k	PCP		36031
R716	180	CF		21795
R717	47	CF		28714
R718	220	CF		21796
R719	220	CF		21796
R720	5k6	CF		21806
R721	2M2	CC		1180
R722	8k2	CF		21808
R723	4k7	CF		21805
R724	2k7	CF		28726
R725	2k2	MF		36030
R726	5k6	CF		21806
R727	4k7	CF		21805
R728	2k7	CF		28726
R729	2k2	MF		36030
R730	2k2	CF		21802
R731	47k	CF		21815
R732	4k7	CF		21805
R733	1k8	CF		28725
R734	1k	CF		21799
R735	680	CF		28723
R736	1k	CF		21799
R737	820	CF		28724
R738	10	CF		21793
R739	10	CF		21793
R740	1k	MF		36032
R741	10	CF		21793
R742	100	CF		21794
R743			¼W	
R744	330	CF		28721
R745	330	CF		28721
R746	4k7	CF		21805
R747	4k7	CF		21805
R748	330	CF		28721
R749	330	CF		28721
R750	4k7	CF		21805
R751	4k7	CF		21805
R754	4k7	CF		21805
R755	47k	CF		21815
R756	47k	CF		21815
R757	1M	CF		31840
R758	1M	CF		31840
R759	4k7	CF		21805
R760	4k7	CF		21805
R761	4k7	CF		21805
R762	4k7	CF		21805
R763	330	CF		28721
R764	4k7	CF		21805
R765	47k	CF		21815
R766	4k7	CF		21805
R767	4k7	CF		21805
R768	4k7	CF		21805
R769	330	CF		28721
R770	4k7	CF		21805
R771	4k7	CF		21805
R772	4k7	CF		21805
R773	4k7	CF		21805
R774	22k	CF		21812
R775	2k2	CF		21802
R776	47	CF		28714
R777	5k6	CF		21806
CAPACITORS				
C701	22µF	E	25V	32181
C702	1000pF	CE(2)		22387
C703	.01µF	CE(2)	250V	22395
C704	.01µF	CE(2)	250V	22395
C705	330pF	CE(2)		22381
C706	82pF	PS	63V	37685
C707	Not fitted			
C708	56pF	CE(2)		22373
C709	.1µF	CE(2)	25V	36709
C710	.1µF	CE(2)	25V	36709
C711	560pF	CE(2)		22384
C712	220pF	PS	63V	35914
C713	3/10pF	TRIMMER		32669
C714	10pF	CE(2)		22364
C715	.1µF	CE(2)	25V	36709
C716	.01µF	CE(2)	250V	22395
C717	.01µF	CE(2)	250V	22395
C718	.1µF	CE(2)	25V	36709
C719	1000pF	PS	63V	44217
C720	.1µF	CE(2)	25V	36709
C721	820pF	CE(2)		22386
C722	.01µF	CE(3)		42444
C723	.01µF	CE(3)		42444
C724	.01µF	CE(3)	50V	42444
C725	.01µF	CE(3)		42444
C726	.01µF	CE(3)		42444
C727	.01µF	CE(3)		42444
C728	.01µF	CE(3)		42444
C729	2.2µF	T	35V	35930
C730	.1µF	CE(3)		43498
C731	.47µF	CE(3)		43500
C732	.1µF	CE(3)		43498
C733	22pF	CE(3)	A.O.T.	42412
C734	22pF	CE(3)	A.O.T	42412

RESIS	R760 R763 R748 R749 R745 R744 R750 R770 R772 R771 R773 R764 R751 R758 R754 R755 R756 R757 R774 R753 R768 R767 R752 R766 R759 R761 R762 R760 R747
CAP	C732 C728 C730 C731 C729 C737 C734 C733 C738 C723 C724 C725 C726 C727 C735 C736 C739 C740 C743 C744 C741 C742
MISC	D714 D718 S702 D716 D719 D715 D721 S701 D717 S704 S705 S703 U722 U725 U724 U718 U721 U730 U731 U723 U716 U721 Q710 U720 U731 U737 U713 U714 U713 U719 U728 U734 U735 U708 U712 U707 U711 U706 U710 U705 U709 U718 U727 U733 U735 U713 U715 U717 U726 U736 U732 U704 U702



NOTE.

1. ALL PUSH BUTTONS NORMALLY OUT.
2. LED'S CONNECT DIRECTLY TO PADS.
3. SOCKETS AX, AY, AZ, AW AND B ARE 16 PIN DIL'S.
4. SKT 15 A 7WAY STRAIGHT MOLEX
5. A.O.T. COMPONENTS

Fig. 5.15 Dot Joiner and Store Logic Circuit Diagram

OS4020 DOT JOINER & STORE LOGIC (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS (Cont.)				
C735	.01μF	CE(3)		42444
C736	.01μF	CE(3)		42444
C737	1000pF	CE(3)		42432
C738	1000pF	CE(3)		42432
C739	.01μF	CE(3)		42444
C740	.01μF	CE(3)		42444
C741	47μF	T	16V	39125
C742	47μF	T	16V	39125
C743	.01μF	CE(3)		42444
C744	.01μF	CE(3)		42444
Q701		BC182B		26110
Q702		E111		36028
Q703		2N2369		23307
Q704		BC214C		36019
Q705		2N2369		23307
Q706		2N2369		23307
Q707		2N2369		23307
Q708		E111		36028
Q709		BC212		29327
Q710		2N2369		23307
DIODES				
D701	6V1	ZENER		33930
D702	5V6	ZENER		33929
D703		IN4148		23802
D704		IN4148		23802
D705		IN4148		23802
D706		IN4148		23802
D707	11V	ZENER		33936
D708		IN4148		23802
D709		IN4148		23802
D710	12V	ZENER		33937
D711		IN4148		23802
D712		IN4148		23802
D713		IN4148		23802
D714		L.E.D.		43847
D715		L.E.D.		43847
D716		L.E.D.		43847
D717		L.E.D.		43847
D718		L.E.D.		43847
D719		L.E.D.		43847
D720		IN4148		23802
U701		MC1408L8		35683
U702		702C		24789
U703		LF356		39226
U704		74LS273		41089
U705		AM9044EPC		43677
U706		AM9044EPC		43677
U707		AM9044EPC		43677
U708		AM9044EPC		43677
U709		AM9044EPC		43677
U710		AM9044EPC		43677
U711		AM9044EPC		43677
U712				
U713		74LS04		36731
U714		74LS377		42763
U715		74LS244		43384
U716		74LS08		36467
U717		74LS157		36735
U718		74LS157		36735
U719		74LS157		36735
U720		74LS393		41090
U721		74LS393		41090
U722		NE556		43749
U723		74LS158		43740
U724		74LS10		36867
U725		74LS279		43667
U726		74LS283		43741
U727		74LS283		43741
U728		74LS283		43741
U729		74LS174		43669
U730		74LS174		43669
U731		74LS123		41084
U732		74LS157		36735
U733		74LS157		36735
U734		74LS157		36735
U735		74LS393		41090
U736		74LS193		43668
U737		74LS158		43740
MISCELLANEOUS				
S701				35341
S702				35341
S703				35342
S704				35342
S705				A4/44692
PLT				38298
PLAL				43832
SKB				38001
SKY				36105
SKAW				38001
SKAX				38001
SKAY				38001
SKAZ				38001

OS4020 TIMEBASE

Ref	Value	Description	Tol % ±	Part No	Ref	Value	Description	Tol % ±	Part No
RESISTORS									
R901	10	CF		21793	R957	100k	CF		21819
R902	390	CF		28722	R958	100k	CF		21819
R903	1k2	CF		21800	R959	12k	CF		21810
R904	1k2	CF		21800	R960	4k7	CF		21805
R905	47	CF		28714	R961	22k	CF		21812
R906	15	CF		28708	R962	6k8	CF		21807
R907	15	CF		28708	R963	27k	CF		21813
R908	3k3	CF	½W	18556	R964	2k2	CF		21802
R909	82	CF		28717	R965	1k2	CF		21800
R910	10	CF		21793	R966	2k2	CF		21802
R911	47	CF		28714	R967	2k2	CF		21802
R912	560	CF		21798	R968	2k2	CF		21802
R913	220	CF		21796	R969	3k9	CF		21804
R914	220	CF		21796	R970	22k	CF		21812
R915	560	CF		21798					
R916	2k2	CF		21802	R972	4k7	CF		21805
R917	22k	CF		21812	R973	10k	CF	A.O.T.	21809
R918	820k	CF		32360	R974	20k	MO	A.O.T.	28806
R919	330	CF		28721	R975	2M2	CC		1180
R920	120	CF		28718	R976	100	CF		21794
R921	270	CF		28720	R977	56k	CF	1W	19058
R922	22k	CF		21812	R978	68k	CF		21816
R923	22k	CF		21812	R979	100	CF		21794
R924	820k	CF		32360	R980	3k9	CF		21804
R925	330	CF		28721	R981	100	CF		21794
R926	1k8	CF		28725	R982	56k	CF	1W	19058
					R983	1k8	CF		28725
R928	270k	CF		32356	R984	10k	WW	4W	29481
R929	2k2	CF		21802	R985	100	CF		21794
R930	2k7	CF		28726	R986	1.6k	MO		28793
R931	10	CF		21793	R987	3k9	CF		21804
R932	220	CF		21796	R988	10k	PCP		39265
R933	1k5	CF		21801	R989	180	CF		21795
R934	3k3	CF		21803	R990	200	PCP		40355
R935	4k7	CF		21805	R991	180	CF		21795
R936	1k	CF		21799	R992	100	CF		21794
R937	10k	CF		21809	R993	10k	WW	4W	29481
R938	1k	CF		21799	R994	56k	CF	1W	19058
R939	1M	CF		31840	R995	1k8	CF		28725
R940	1k	CF		21799	R996	100k	CF		21819
R941	22k	CF		21812	R997	1.6k	MO		28793
R942	270	CF		28720	R998	1k8	CF		28725
R943	3k3	CF		21803					
R944	2k2	CF		21802	R1000	15k	CF		28727
R945	2k2	CF		21802	R1001	15k	CF		28727
R946	2k2	CF		21802	R1002	27k	CF		21813
R947	4k7	CF		21805	R1003	22k	CF		21812
R948	56k	CF		28729	R1004	4k7	CF		21805
R949	82k	CF		21818	R1005	22k	CF		21812
R950	22k	CF		21812	R1006	27k	CF		21813
R951	12k	CF		21810					
R952	18k	CF		21811	R1008	4k3	MO		26723
R953	3k9	CF		21804	R1009	2k	PCP		40354
R954	3k9	CF		21804	R1010	4.3k	MO		26723
R955	47k	CF		21815	R1011	2k	PCP		40354
R956	56k	CF		28729	R1012	2k	PCP		40354

OS4020 TIMEBASE (Cont.)

Ref	Value	Description	Tol %±	Part No
RESISTORS (Cont.)				
R1015	3k3	CF		21803
R1016	4k7	CF		21805
R1017	2k	PCP		40354
R1018	2k7	CF		28726
R1019	900	MF		35582
R1020	100	MF		35581
R1021	10k	CF		21809
R1022	1k	CF		21799
R1024	10	CF		21793
R1025	1k8	CF		28725
R1026	1k	CF		21799
R1027	4k7	CF		21805
R1028	47k	CF		21815
R1029	100k	CF		21819
R1030	4k7	CF		21805
R1031	20k	PCP		39235
R1032	88k7	MF	1	28305
R1033	50k	PCP		39268
R1034	383k	MF	1	30764
R1035	100k	CF		21819
R1036	4k7	CF		21805
R1037	47k	CF		21815
R1038	4k7	CF		21805
R1039	1k	CF		21799
R1040	1k8	CF		28725
CAPACITORS				
C901	.01µF	CE(3)		42444
C902	33pF	CE(3)		42414
C903	33pF	CE(3)		42414
C904	.01µF	CE(3)		42444
C905	27pF	CE(3)		42413
C906	.47µF	E	100V	36882
C907	.47µF	PE	160V	35604
C908	470pF	CE(3)		42484
C909	4700pF	CE(3)		42440
C910	.01µF	CE(3)		42444
C911	270pF	CE(3)		42425
C912	.01µF	CE(3)		42444
C913	.01µF	CE(3)		42444
C914	27pF	CE(3)		42413
C915	27pF	CE(3)		42413
C916	27pF	CE(3)		42413
C917	.01µF	CE(3)		42444
C918	.047µF	CE(3)		43497
C919	.1µF	CE(3)		43498
C920	220pF	PS		35914
C921	.1µF	CE(3)		43498
C922	.1µF	CE(3)		43498
C923	82pF	CE(3)		42419
C925	.01µF	CE(3)		42444
C926	27pF	CE(3)		42413
C927	.047µF	CE(3)		43497
C928	220pF	CE(3)		42424
C929	.047µF	CE(3)		43497
C930	.01µF	CE(2)		24886
C931	820pF	CE(3)		42431
C932	.01µF	CE(3)		42444
C933	.01µF	CE(3)		42444
C934	33pF	CE(2)	50V	42414
TRANSISTORS				
TR901		2N2369		23307
TR902		2N2369		23307
TR903		2N2369		23307
TR904		2N2369		23307
TR905		BC212		29327
TR906		BC182B		33205
TR907		BC212		29327
TR908		2N2369		23307
TR909		2N2369		23307
TR910		BC212		29327
TR911		2N2369		23307
TR912		2N2369		23307
TR913		2N2369		23307
TR914		BC108		26110
TR915		AE13		A31254
TR916		AE13		A31254
TR917		BC108		26110
TR918		2N2369		23307
TR919		2N2369		23307
TR920		2N2369		23307
TR921		BC214C		36019
TR922		BC212		29327
TR923		BC182B		33205
TR924		BC212		29327
TR925		BF258		31490
TR926		BF258		31490
TR927		BC212		29327
TR928		J111		36208
TR929		J111		36208
TR930		2N2369		23307
TR931		2N2369		23307
TR932		BC212		29327
TR933		BC212		29327
TR934		BC212		29327
TR935		BC212		29327
TR936		2N2369		23307
TR937		J111		36028
TR938		J111		36028
TR939		2N2369		23307
TR940		BC212		29327
DIODES				
D901		IN3595		29330
D902		IN4148		23802
D903		IN4148		23802
D904		IN4148		23802
D905	8V2	ZENER		33933
D906		IN4148		23802
D907		IN4148		23802

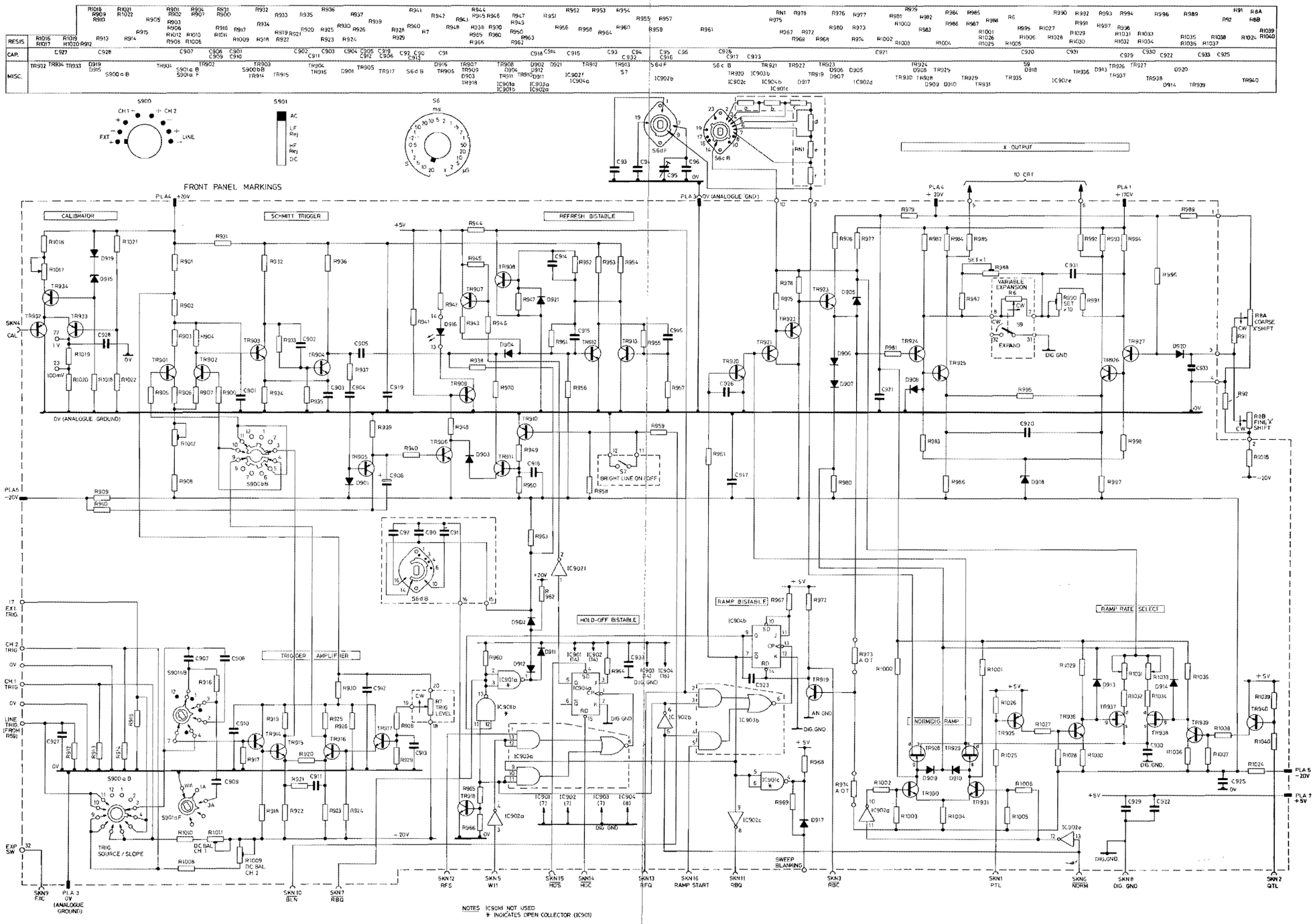


Fig. 5.16 Timebase Circuit Diagram

OS4020 POWER SUPPLIES Y O/P AMPLIFIER AND BLANKING AMPLIFIERS

Ref	Value	Description	Tol % ±		Part No
RESISTORS					
R401	3M3	MF		½W	36002
R402	500	CP			A4/35335
R403	100	CF			21794
R404	100	CF			21794
R405	2M2	CC			1180
R406	4k7	CC			3427
R407	1M5	CC			7016
R408	200k	PCP			39264
R409	10k	PCP		½W	39265
R410	51k	MO			28815
R411	3M3	MF			36002
R412	15k	CF			28727
R413	47k	CF			21815
R414	220k	CF			21823
R415	1M	CC			1171
R416	1M	CP			A4/35337
R417	200k	PCP			39264
R418	2/0k	CF			32356
R419	220k	CP			A4/35336
R420	560k	CF			32359
R421	10k	CF			21809
R422	2M2	CC			1180
R423	3k	WW			33212
R424	91	MO			28782
R425	47	CF			28714
R426	68	CF			28716
R427	33k	CF			21814
R428	390	CF			19038
R429	91	MO			28782
R430	47	CF			28714
R431	10	CF			21793
R432	3k	MO	5	6W	33212
R433	100	CF			21794
R434	100	CF			21794
R435	68	CF			28716
R436	100	CF			21794
R437	100	CF			21794
R438	220	CP			35877
R439	2k7	CF			28726
R440	2k7	CF			28726
R441	470	CF			21797
R442	470	CF			21797
R443	22	CF			28710
R444	10	CF			21793
R447	150	CF			28719
R448	680	CF			28723
R450	100	CF			21794
R451	10	CF			21793
R501	100k	CF			18574
R502	3k3	CF			21803
R503	3k3	CF			21803
R504	5k6	CF			21806
R505	5k6	CF			21806
R506	5k6	CF			21806
R507	6k8	CF			21807
R508	5k6	CF			21806
R509	3k3	CF			21803
R510	1k	CF			21799
R511	3k9	MO			26724
R512	3k3	CF			21803
R513	2k2	CF			21802
R515	100	CF			21794
R516	3k3	CF			21803
R517	10k	CF			21809
R518	470	CF			21797
R519	820	CF			28724
R520	56	CF			28715
R521	47	CF			28714
R522	OR22	WW	10	2½W	36159
R523	220	CF			21796
R524	12k	WW			21141
R525	12k	WW			21141
R526	15k	CF		½W	18564
R527	18k	CF		2W	29491
R528	22k	CF		½W	18566
R529	1k	PCP			36080
R530	560	CF		1W	19040
R532	8k2	CF		½W	18561
R533	1M	CF			31840
R534	2k7	CF			28726
R535	4k7	CF			21805
R538	100	CF			21794
R539	100	CF			21794
R540	47	CF		1W	4038
CAPACITORS					
C401	.01µF	CE(2)		250V	22395
C402	1µF	E		350V	29494
C403	4.7µF	E		63V	32195
C404	4µF	E		450V	23599
C405	4µF	E		450V	23599
C406	4µF	E		450V	23599
C407	4µF	E		450V	23599
C408	4µF	E		450V	23599
C409	4µF	E		450V	23599
C410	5.6nF	CE(2)		4kV	43117
C411	5.6nF	CE(2)		4kV	43117
C412	5.6nF	CE(2)		4kV	43117
C413	5.6nF	CE(2)		4kV	43117
C414	.047µF	CE(2)		1k5V	36633
C415	.01µF	PE		5kV	37854
C417	100pF	CE(2)			22376
C418	100pF	CE(2)			22376
C419	12/75pF	TRIMMER			36091
C420	150pF	SM			4514

OS4020 TIMEBASE (Cont.)

Ref	*Value*	*Description*	*Tol %±*	*Part No*
DIODES (Cont.)				
D908		IN4148		23802
D909		IN4148		23802
D910		IN4148		23802
D911		IN4148		23802
D912		IN4148		23802
D913		IN4148		23802
D914		IN4148		23802
D915	5V6	ZENER		33929
D916		LED MV5153		43847
D917		OA47		4468
D918	6V8	ZENER		4666
D919		IN4148		23802
D920		IN4148		23802
D921		IN4148		23802

Ref	*Value*	*Description*	*Tol %±*	*Part No*
INTEGRATED CIRCUITS				
IC901		74LS01		41074
IC902		74LS04		36731
IC903		74LS51		43676
IC904		74LS112		36468
MISCELLANEOUS				
S900		Switch - Trig. Source		35999
S901		Switch - Trig. Coupling		35343
SKN				38001
PLA				37877

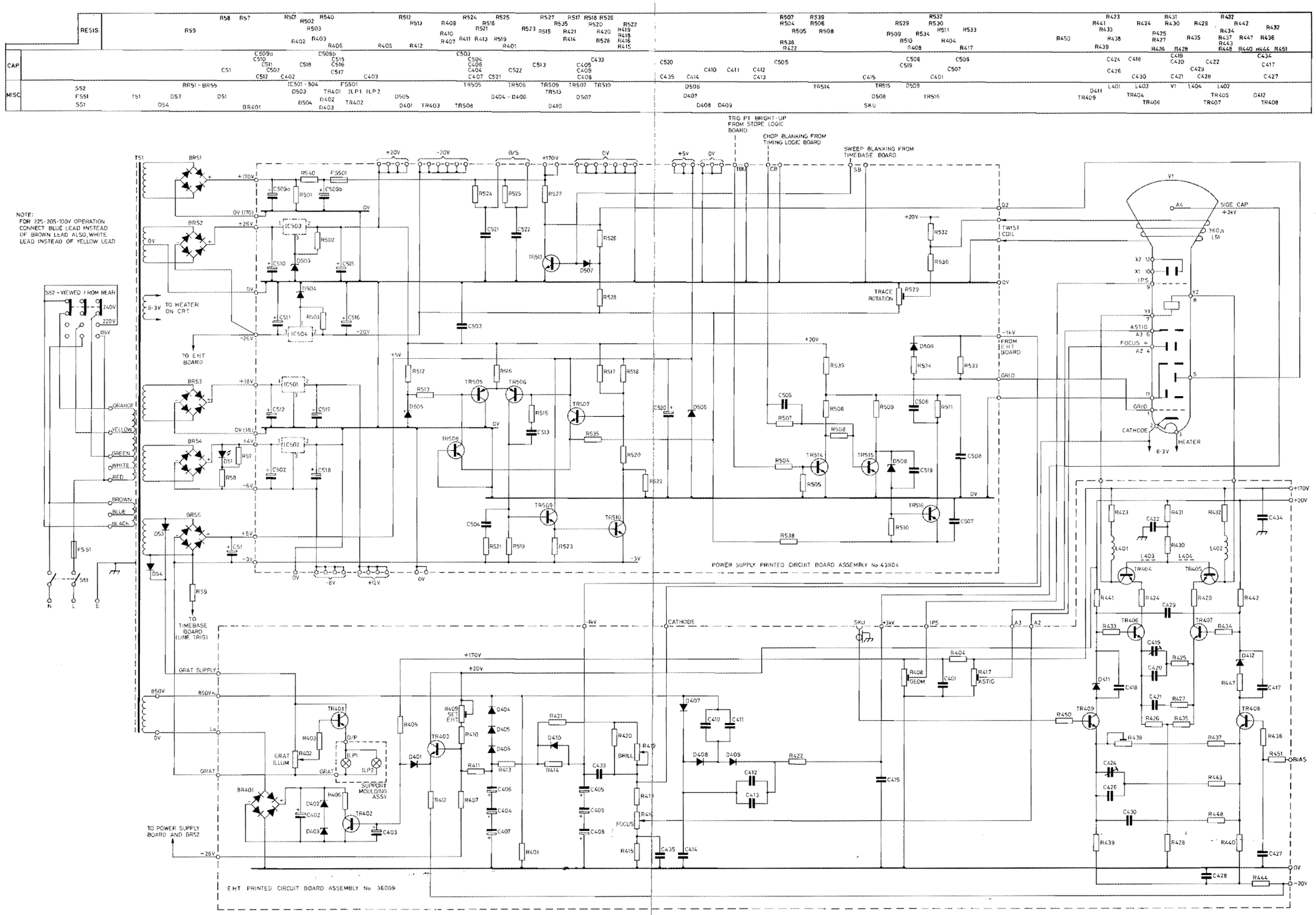


Fig. 5.17 Power Supplies Circuit Diagram

0S4020 INTERCONNECTIONS

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R1	22k	CP		A4/35986
R2	22k	CP		A4/35986
R3	470	CP WITH S13		A4/36070
R4	470	CP WITH S14		A4/36070
R6	5k	CP Part of S8/S9		43683
R7	22k	CP		A4/35338
R8		CP R8a + R8b		A3/43681
R22	22	CF		28710
R23	22	CF		28710
R24	990k	MF	0.5	31927
R25	27	CF		28711
R26	470k	CC		4906
R27	1M	MF		26346
R28	18	CF		28709
R29	16k	MF		29361
R30	15k8	MF		33291
R31	5k23	MF		33290
R32	1k72	MF		33289
R33	787	MF		33288
R34	360	MF		33287
R42	22	CF		28710
R43	22	CF		28710
R44	990k	MF		31927
R45	27	CF		28711
R46	470k	CC		4906
R47	1M	MF		26346
R48	18	CF		28709
R49	16k	MF		29361
R50	15k8	MF		33291
R51	5k23	MF		33290
R52	1k72	MF		33289
R53	787	MF		33288
R54	360	MF		33287
R57	270	CF		28720
R58	560	CC	5	9236
R59	150k	CF		21821
R90	100k	CC	5 1W	19061
R91	470	CF		21797
R92	4k7	CF		21805
RN1		Resistor Network		A3/36455
CAPACITORS				
C20	.1μF	CE(2)	400V	29495
C25	.01μF	CE(2)		31388
C40	.1μF	CE(2)		29495
C45	.01μF	CE(2)		31388
C51	47000μF	CE(2)	10V	36024
C90	5600pF	CE(3)		42441
C91	4.7μF	E	63V	32195
C92	.047μF	CE(3)		43497
C93	1μF	PC	1 63V	24888
C94	.01μF	PC	1 160V	24886
C95	6/25pF	TRIMMER		23593
C96	47pF	S/M		685
MISCELLANEOUS				
BR51		W04		29367
BR52		W04		29367
BR53		W04		29367
BR54		W04		29367
BR55		VJ148		43198
S1		Lever, 3 Position		37045
S2		Lever, 3 Position		37045
S3		ATTENUATOR		35998
S4		ATTENUATOR		35998
S6		TIMEBASE WITH R8		43681
S7		S.P. Push-pull WITH R7 + CP		A4/35338
S8		EXPANSION WITH R6		43683
S13		FINE GAIN WITH R3		A4/36070
S14		FINE GAIN WITH R4		A4/36070
S51		DP, DT PUSH ON		A4/36232
S52		SLIDER		36815
L20		FERRITE FX1242		26986
L21		FERRITE FX1242		26986
L22		FERRITE FX1242		26986
L23		FERRITE FX1242		26986
L24		FERRITE FX1242		26986
L25		FERRITE FX1242		26986
T51				A1/36171
D51				40105
D53		IN4003 MOTOROLA		32771
D54		IN4003 MOTOROLA		32771
V1		THORN D14-G181GH		32380
1LP1				35471
1LP2				35471
FS51	500mA	SLO-BLO 230V supply		33685
	1A	SLO-BLO 115V supply		34790

OS4020 POWER SUPPLIES Y O/P AMPLIFIER AND BLANKING AMPLIFIERS (Cont.)

Ref	Value	Description		Tol %±	Part No
CAPACITORS (Cont.)					
C421	.15µF	CE(2)		250V	35601
C422	.1µF	CE(2)		25V	36709
C424	10/40pF	TRIMMER			35506
C426	39pF	CE(2)			22371
C427	.047µF	CE(2)		12V	19657
C428	.01µF	CE(2)		250V	22395
C429	5.6pF	CE(2)			22361
C430	75pF	PS		63V	42365
C433	1µF	PE		250V	35606
C434	.01µF	CE(2)		250V	22395
C435	4700pF	CE(2)		4kV	26863
C502	4700µF	E		16V	36020
C503	.1µF	CE(3)			43498
C504	.1µF	CE(3)			43498
C505	15pF	CE(3)			42410
C506	.02µF	CE(2)		2kV	42367
C507	.1µF	CE(3)			43498
C508	.1µF	CE(3)			43498
C509	100µF + 100µF	E	C509a + C509b	300V	36023
C510	2200µF	E		40V	36022
C511	2200µF	E		40V	36022
C512	3300µF	E		25V	36021
C513	560pF	CE(3)			42429
C515	10µF	E		25V	32180
C516	10µF	E		25V	32180
C517	10µF	E		25V	32180
C518	10µF	E		25V	32180
C519	.01µF	CE(3)			42444
C520	10µF	E		25V	32180
C521	.01µF	CE(3)			42444
C522	.01µF	CE(3)			42444
TRANSISTORS					
TR401		2N3053			4039
TR402		BD159			34652
TR403		BC182B			33205
TR404		BF380			32902
TR405		BF380			32902
TR406		AE13	PAIR		31254
TR407		AE13			
TR408		2N2369			23307
TR409		2N2369			23307
TR505		BC212			29327
TR506		BC212			29327
TR507		BC182			33205
TR508		BC182			33205
TR509		2N3053			4039
TR510		2SC1173			36188
TR513		2N5831			33209
TR514		2N2369			23307
TR515		2N2369			23307
TR516		BC182			33205
DIODES					
D401		IN4007			52337
D402	180V	ZENER			40632
D403	180V	ZENER			40632
D404		IN4007			52337
D405		IN4007			52337
D406		IN4007			52337
D407		1AV12OTR			44550
D408		1AV12OTR			44550
D409		1AV12OTR			44550
D410		IN4007			52337
D411	11V	ZENER			33936
D412	10V	ZENER			33935
D503	5V1	ZENER			33928
D504	5V1	ZENER			33928
D505	5V1	ZENER			33928
D506	6V2	ZENER			28764
D507		IN4148			23802
D508	24V	ZENER			33944
D509		IN4148			23802
INTEGRATED CIRCUITS					
IC501				12V	36178
IC502				6V	36177
IC503				15V	36179
IC504				15V	36185
MISCELLANEOUS					
BR401		W04			29367
L401	33uH				33204
L402	33uH				33204
L403		Ferrite Bead			4442
L404		Ferrite Bead			4442
FS501				250mA	32338
SKU					36105

NOTES

1. FOR 225–205–100V OPERATION CONNECT TO 100V TAPS INSTEAD OF 115V ON BOTH PRIMARIES.
2. S6, S8, S3 & S4 ARE SHOWN IN THEIR FULLY ANTICLOCKWISE POSITION

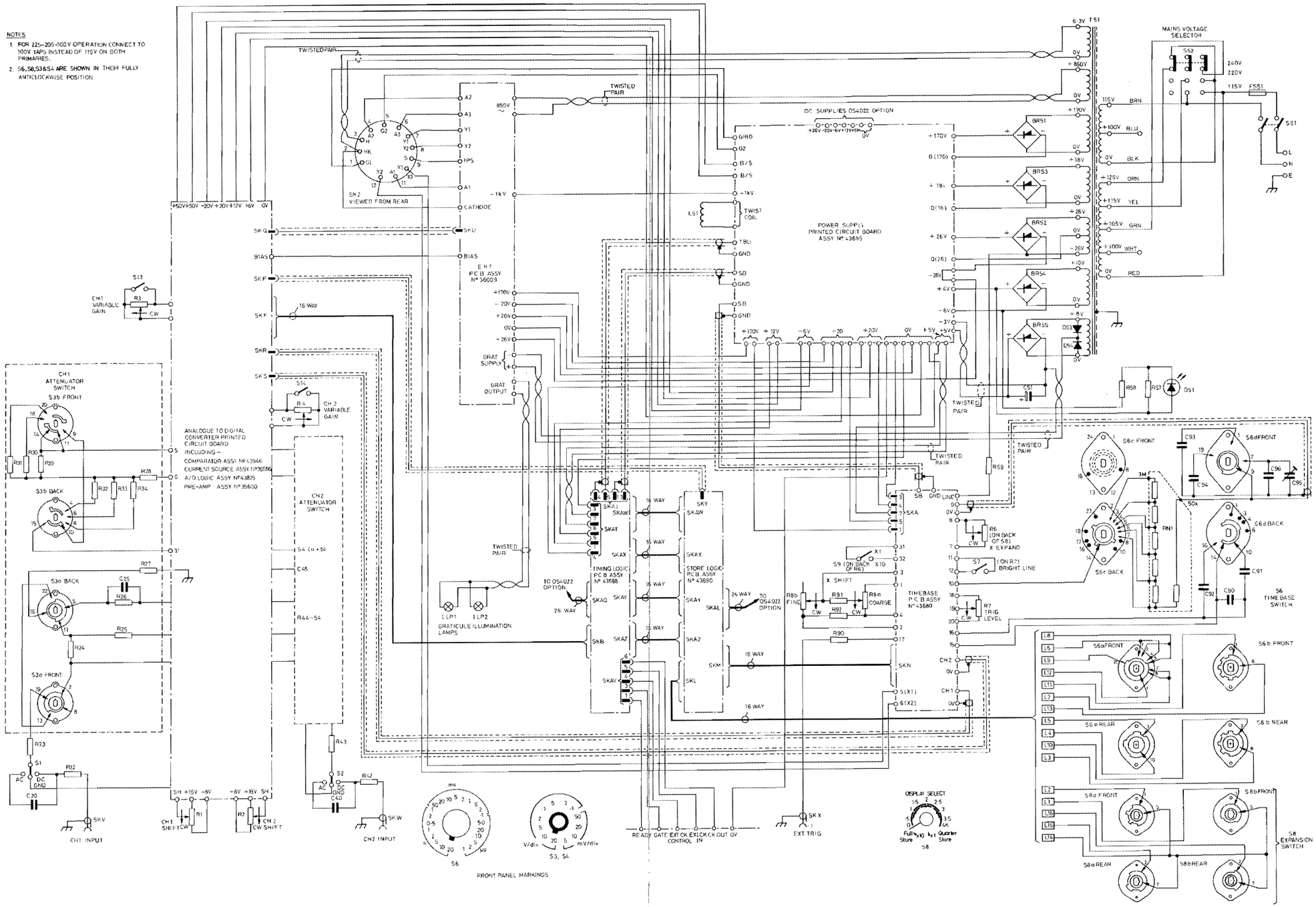


Fig. 5.18 Interconnections Circuit Diagram

OS4022 O/P OPTION FOR OS4020

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R1	100k	CP		A4/44570
R801	4k7	CF		21805
R802	4k7	CF		21805
R803	470	CF		21797
R804	330	CF		28721
R805	4k7	CF		21805
R806	4k7	CF		21805
R807	4k7	CF		21805
R809	4k7	CF		21805
R810	12k	MF	2	38620
R811	4k7	CF		21805
R812	430	MF	2	38585
R813	2k7	MF	2	38604
R814	2k7	MF	2	38604
R815	2k7	MF	2	38604
R816	2k	PCP		40178
R817	500	PCP		39262
R818	2k2	CF		21802
R819	2k2	CF		21802
R820	430	MF	2	38585
R821	100	CF		21794
R822	430	MF	2	38585
R823	430	MF	2	38585
R824	4k7	MF	2	38610
R825	100	CF		21794
R826	500	PCP		39262
R827	330	CF		28721
R828	100	CF		21794
R829	2k7	MF	2	38604
R830	4k7	MF	2	38610
R831	30k	MF	2	38629
R832	2k	PCP		40178
R833	18k	CF		21811
R834	4k7	CF		21805
R835	180	CF		21795
R836	3k9	CF		21804
R837	560	MF	2	38588
R838	1k8	MF	2	38600
R839	1k	PCP		39261
R840	100	PCP		39263
N801	4k7	Resistor Network		39225
N802	4k7	Resistor Network		39225
N803	4k7	Resistor Network		39225
CAPACITORS				
C1	.1µF	CE(2)	25V	36709
C2	.1µF	CE(2)	25V	36709
C3	.1µF	CE(2)	25V	36709
C801	.01µF	CE(3)		42444
C802	.01µF	CE(3)		42444
C803	.01µF	CE(3)		42444
C804	.01µF	CE(3)		42444
C805	.01µF	CE(3)		42444
C806				
C807	1µF	T	35V	54221
C809	1µF	T	35V	54221
C810	47µF	T	16V	39215
C811	.01µF	CE(3)		42444
C812	.01µF	CE(3)		42444
C813	.01µF	CE(3)		42444
C814	.01µF	CE(3)		42444
C815	.01µF	CE(3)		42444
C816	.01µF	CE(3)		42444
C817	2.2µF	T	35V	35930
C818	.01µF	CE(3)		42444
C819	.01µF	CE(3)		42444
C820	.01µF	CE(3)		42444
C821	47µF	T	16V	39215
C822	47µF	T	16V	39215
C823	47µF	T	16V	39215
C824	22µF	T	6V3	54230
C825	.01µF	CE(3)		42444
C826	47µF	T	35V	35933
C827	47µF	T	35V	35933
C828	.01µF	CE(3)		42444
C829	.01µF	CE(3)		42444
C830	.01µF	CE(3)		42444
C831	.01µF	CE(3)		42444
Q801		BC212		29327
DIODES				
D801	15V	ZENER		4669
D802	15V	ZENER		4669
U801		74LS244		43384
U802		74LS374		43386
U803		74LS374		43386
U804		74LS02		41075
U805		DAC 9356		43953
U806		74LS374		43386
U807		74LS240		43382
U808		74LS273		41089
U809		74LS273		41089
U810		74LS04		36731
U811		74LS390		43675
U812		74LS390		43675
U813		74LS390		43675
U814		74LS293		39241
U815		74LS156		39237
U816		74LS393		41090
U817		74LS244		43384
U818		MC1408LS		35683
U819		MC1408LS		35683
U820		74L06		36959

OS4020 INTERCONNECTIONS (Cont.)

Ref	*Value*	*Description*	*Tol %±*	*Part No*
MISCELLANEOUS (Cont.)				
FS501	250mA			32338
L51		TWIST COIL C.R.T.		A3/32495
SKV				1222
SKW				1222
SKX				1164
SKZ				24913

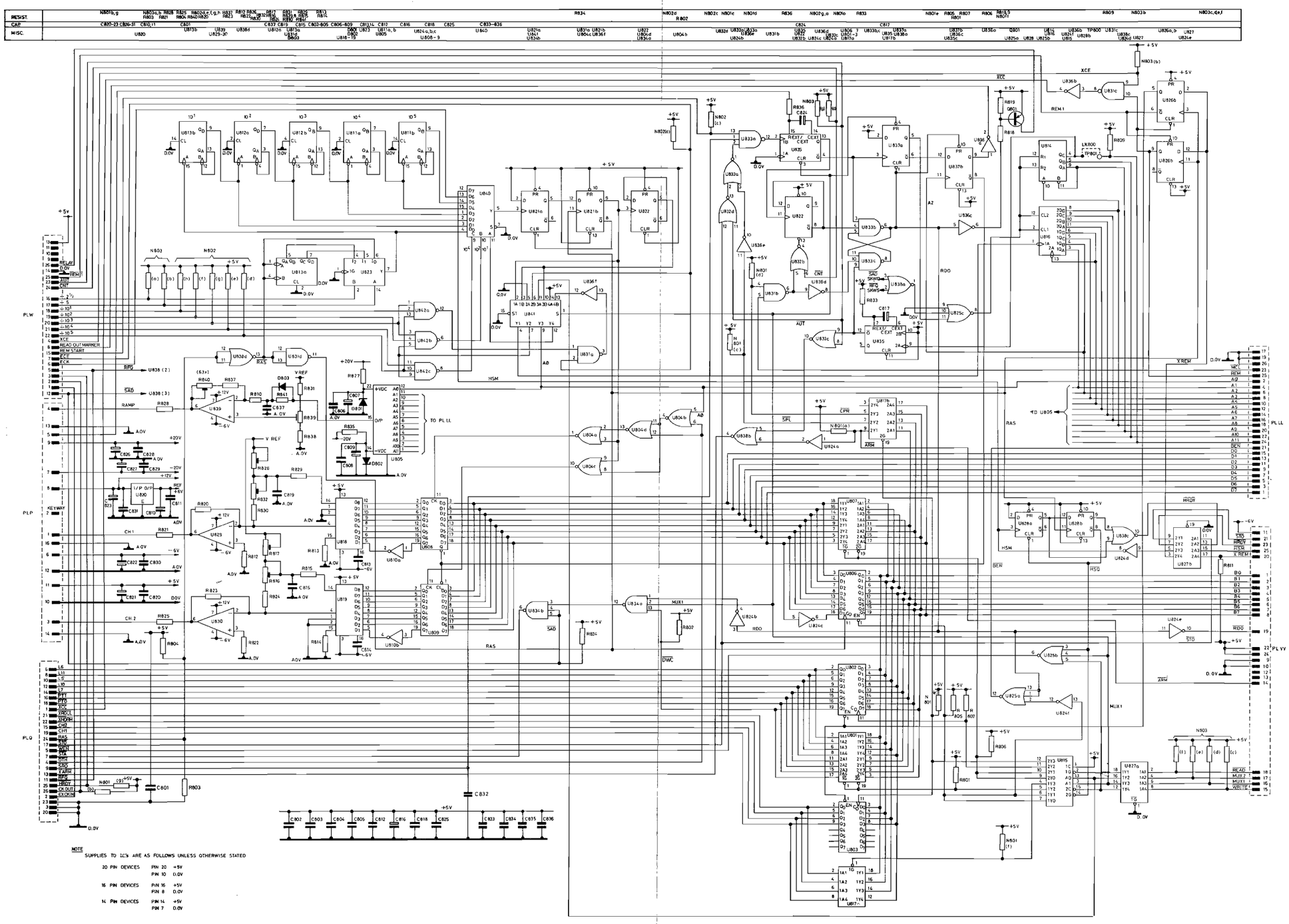


Fig. 5.19 4022 Plotter Circuit Diagram

OS4020 O/P OPTION FOR OS4020

Ref	Value	Description	Tol %±	Part No
U817		74LS244		43384
U818		MC1408LS		35683
U819		MC1408LS		35683
U820		74L06		36959
U821		74LS74		36732
U822		74LS74		36732
U823		74LS153		36247
U824		74LS04		36731
U825		74LS27		41077
U826		74LS74		36732
U827		74LS244		43384
U828		74LS74		36732
U829		741		36736
U830		741		36736
U831		74LS00		36730
U832		74LS02		41075
U833		74LS10		36867
U834		74LS10		36867
U835		74LS221		39239
U836		74LS04		36731
U837		74LS74		36732
U838		74LS02		41075
U839		741		36736
U840		74LS151		41085
U841		74157		36007
U842		74LS10		36867
MISCELLANEOUS				
S1				43962
S2				37614
RLA				43961
PLQ				43952
PLW				43952
PLLL				43952
PLVV				43952

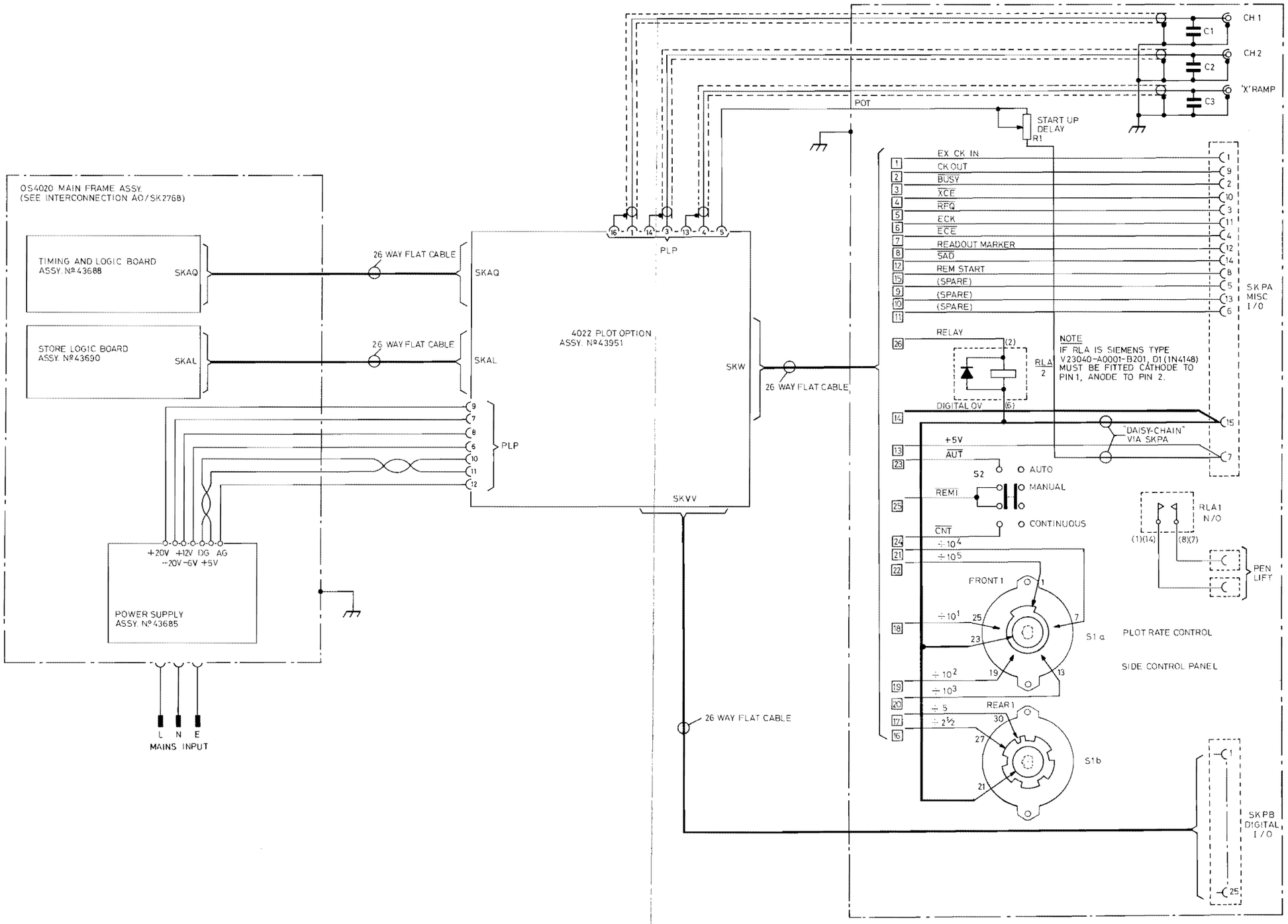


Fig. 5.20 4022 Interconnections Circuit Diagram

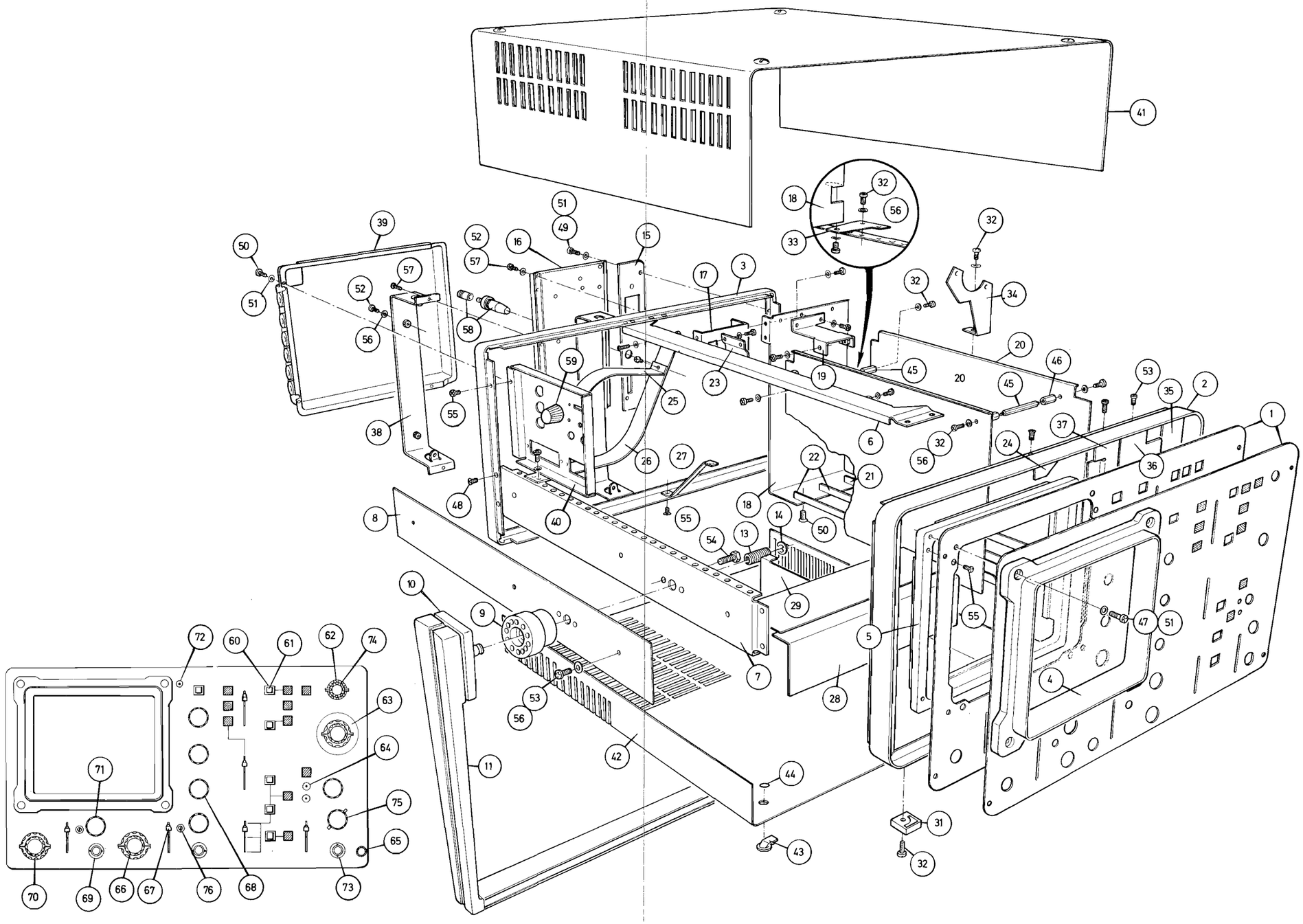


Fig. 5.21 Mechanical View Circuit Diagram

Ref. No.	Part No.	Description	No. Off	Ref No.	Part No.	Description	No. Off
1	43834	Front Panel Composite	1	39	44028	Cover rear Assy.	1
2	44580	Frame Front	1	40	44085	Control Support Bracket (OS4022)	1
3	43694	Frame Rear	1	41	36915	Cover Top (OS4022 Pt. No. OS4022)	1
4	36351	Escutcheon on (DN AZ-31117)	1	42	36055	Cover Bottom	1
5	35298	Moulded Tube Support	1	43	37864	Latch	8
6	36049	Bracket Top Support	1	44	37915	'O' Ring	8
7	43965	Bracket Support (RH)	2	45	36073	Spacer Male	3
8	43966	Trim Side Strip	2	46	36074	Nylon Spacer	7
9	43969	Block Indexing	2	47	22816	Screw 6-32 x 3/8 Pan Head	
10	44576	Handle Skirt	2	48	22772	Screw 6-32 x 3/8 C'sk Head	
11	43757	Handle Assembly on (DN A1-40805)	1	49	26403	Screw 6-32 x 1/4 Pan Head T T	
12	44945	Title Strip	1	50	22815	Screw 6-32 x 1/2 Pan Head TT	
13	42645	Compression Spring	2	51	1199	Washer 6-32 Plain	
14	10016	Circlip	2	52	22842	Screw 4-40 x 1/4 Pan Head	
15	44663	Panel Rear	1	53	22844	Screw 4-40 x 3/8 Pan Head	
16	36047	Heatsink	1	54	41764	Screw M4 x 10mm. Hexagon Headed	4
17	39260	Mounting Plate	1	55	22780	Screw 4-40 x 1/4 C'sk Head	
18	36050	Rear Mounting Plate P.C.B.	1	56	1200	Washer 4-40 Plain	
19	38800	Bracket Support P.C.B.	1	57	22698	Screw 4-40 x 1/4 Pan Head TT	
20	44173	Screen Store, Logic Timing P.C.B.	2	58	32210	Fuse Holder	
21	36046	Bracket Support P.C.B.	1	59	40794	Knob R4-354	2
22	36689	Bracket Support P.C.B.	2	60	44442	Bezel-Pushbutton	6
23	36066	Heatsink	1	61	38407	Knob-Pushbutton	6
24	36321	Bearing Plate	1	62		Knob	1
25	36052	Tube Clamp	1	63	44849	Skirt Printed	1
26	36051	Bracket Tube Rear Mtg.	1	64	24159	Terminal Lead Through	2
27	36078	Braket Beam Switch P.C.B.	1	65	32310	Terminal Earth	1
28	36043	Attenuator. Front Panel Inner	1	66	40922	Knob R2-324	3
29	36042	Screen Attenuator	1	67	36324	Knob Lever Switch	5
30	36063	Screen C.R.T.	1	68	40923	Knob R2-354	4
31	36329	Foot Moulded	4	69	1222	Socket BNC	2
32	22695	Screw 4-4D x 5/16 Pan Head		70	40410	Knob R4-454	3
33	36079	Bracket Mtg. P.C.B. Support	1	71	40924	Knob R2-334	2
34	35348	Bracket	1	72	40105	Indicator L.E.D.	1
35	43693	Switch Mounting Plate	1	73	1164	Socket BNC	1
36	43746	Front Panel Inner. Timing	1	74	40580	Knob R2-224	1
37	43745	Front Panel Inner. Store Logic P.C.B.	1	75	40794	Knob R4-354	1
38	44566	Cover Bracket	2	76	34651	Bush P.T.F.E.	2

Guarantee and Service Facilities

Section 7

This instrument is guaranteed for a period of two years from its delivery to the purchaser, covering faulty workmanship and replacement of defective parts other than cathode ray tubes and batteries (where fitted). Cathode ray tubes are subject to the manufacturers guarantee. This assumes fair wear and tear and usage in the specified environment and does not cover routine recalibrations and mechanical adjustments.

We maintain comprehensive after sales facilities and the instrument should be returned to our factory for servicing if this is necessary. The type and serial number of the instrument should always be quoted, together with full details of any fault and service required.

Equipment returned for servicing must be adequately packed, preferably in the box in which the instrument was supplied and shipped with transportation charges prepaid. We accept no responsibility for instruments arriving damaged. Should the cause of failure during the guarantee period be due to misuse or abuse of the instrument, or if the guarantee has expired the repair will be put in hand without delay and charged unless other instructions are received.

Our Sales, Service and Engineering Departments are ready to assist you at all times.

The Service Department can provide maintenance and repair information by telephone or letter, if required.

Note: Please check fuses before returning instruments for service and ensure that any 13 Amp mains plugs fitted are removed. To prevent possible transit damage, we regret that mains plugs cannot be returned.

Service Dept.,
Roebuck Road,
Hainault,
Essex,
IG6 3UE

Tel: 01-500 1000
Telex: 263785
Telegrams: Attenuate Ilford