Tillhör
AM 55

part number 97100041R1

9440
Service Manual

Navtel

STATEMENT OF WARRANTY

NAVTEL products are warranted in their entirety against any defects of material or workmanship which develop for any reason whatsoever, except abuse, within a period of one (1) year following the date of purchase of the NAVTEL product. This warranty is extended by NAVTEL only to the original purchaser or user of the NAVTEL product.

In the event a defect develops during the warranty period, NAVTEL will, at NAVTEL's election, repair or replace the product with a new or reconditioned model of equivalent quality. In order to obtain performance of any obligation under the warranty, the purchaser must return the product to the designated service depot. NAVTEL will incur transportation expenses one way.

NAVTEL shall not be liable for loss of the use of the NAVTEL product or other incidentals or consequential damages, expenses, economical loss, or for any claim or claims for such damages, expenses or economical loss.

Navtel

TABLE OF CONTENTS

FIGURES

SECTION 1

INTRODUCTION

1.0 SCOPE

This manual is a maintenance guide for NAVTEL 9440 Protocol Analyzer. The manual is organized in the following manner :

Section 2	lists other documents that should be used in conjunction with this manual.
Section 3	covers the theory of operation for the internal circuitry down to the component level. The exceptions are OEM components. In those instances only a system level description is provided.
Section 4	provides a system verification procedure.
Section 5	includes a troubleshooting guide presented in a flowchart type format. The aim of the guide is to isolate any faults on the 9440 to subsystem level.
Section 6	is a list of bill of materials.
Section 7	are assembly drawings and schematics for the 9440 unit.

SECTION 2
REFERENCE

2.1 REFERENCE DOCUMENT

The following documents should be used in conjunction with this service manual :

1) 9440 Operators Manual

2) SONY Micro Floppy Disk Drive Service Manual for model number MP-F17W-50L

3) INTEL data sheets for the following list of IC's :

- 80188 Mircoprocessor chip
- 82072 Floppy Disk Controller
- 82716 CRT Controller

4) Zilog data sheets for 80C30 Serial Communication Controller.

2.2 SERVICE SUPPORT

Any service support request or question regarding the content of this manual should be directed to:

Quality Engineering
NAVTEL Canada Inc,
55 Renfrew Drive
Markham, Ontario
Canada L3R 8H3
Telephone : 416-479-8090
Telex : 06-986189
Fax: 416-475-6524

SECTION 3

THEORY OF OPERATION

3.1 GENERAL SYSTEM DESCRIPTION

This section of the manual will provide a description of the major subsystems shown in the 9440 System Block Diagram (drawing # 04-100041B). All drawings referenced in this section are included in section 7 of this service manual.

The 9440 is a multiprocessor system. There are two internal processor boards in the basic system. Both are based on the Intel 80188 CPU. The first processor board, which is referred to as the MAIN PROCESSOR CARD or MPC, is a general purpose card for controlling all of the major subsystems in the unit such as the disk drive, CRT, and keyboard interface. The second card, which is the DATA LINK CONTROLLER or DLC, is a dedicated processor card for controlling the testing of the data communication circuitry.

Other major subsystems in the 9440 are :

- Status Indicator Board.
- Power supply.
- 3.5 inch high density disk drive.
- 5 inch CRT display.
- Keyboard.

The disk drive used in the 9440 is a 3.5 inch high density drive with a formatted storage capacity of 1.44 M. The drive serves two purposes : first, the disk drive is needed because a disk operating system is implemented for the 9440 and second, the disk drive allows for the storage of captured test data on diskette.

The power supply is a triple output OEM unit from Computer Product. It is capable of operating from an input voltages of 85 to 264 VAC and a frequency of 47 to 440 Hz. The DC outputs provided by this unit are : 7.0A @ 5V, 2.5A @ 12V and 0.7A @ - 12V.

A 5 inch CRT display is used in the 9440 for operator interface and test status display. Normal mode of operation is 40 columns by 20 rows. In the VT100 terminal emulation mode the screen is set up for 80 columns by 25 rows.

The Status Indicator Board or SIB provides the standard Navtel breakout on the RS232 interface. It uses the same breakout method implemented on other Navtel products such as the Datacheck 2 and the Datatest 2+.

3.2 MAIN PROCESSOR PCB

The 9440 MPC can be classified into six main functional blocks as illustrated in figure 3.1. These functional blocks are :

- microprocessor
- memory
- CRT controller (CRTC)
- floppy disk controller
- support logic
- shared RAM bus and keyboard & serial
- port controller.

Each of these blocks are described in the following sections.

3.2.1 Microprocessor

The microprocessor is an Intel, 12 MHz 80C188 microprocessor, operating with zero wait-state memory. The device contains two DMA channels, three timers, an interrupt controller and programmable memory & peripheral chip-select generators. A DMA request can be initiated by either the floppy disk controller or a device on the backplane. One of the timers is used as a waveform generator for an audio speaker. Four external interrupt lines are available to external devices. Interrupt 0 is dedicated to MPC based devices. Interrupts 1 to 3 are reserved for backplane cards. The non-maskable interrupt (NMI) is not used.

There are 768 Kbytes of available, on-board RAM and a maximum of 128k of EPROM space for the user. The EPROM that is actually used has a 32k capacity, but they are packaged in 28-pin DIPs therefore, they cannot be randomly inserted in the 32-pin EPROM socket. As a general rule, all EPROMs must be inserted into the socket with their ground pin matching pin 16 of the socket. Also note that the capacity of the EPROM is jumper configurable. The I/O and memory maps of the MPC are shown on figures. 3.2 and 3.3, respectively.

On power up, the processor accesses the EPROM and executes the disk-loader code which moves all the application software from disk to RAM. The EPROM is accessed only on power up. After all the software has been loaded, the EPROM is bank switched with the CRTC and its configuration code is executed. A similar switching operation is used to control the flow of /CTS to the MUART. One mode allows /CTS to be passed in its entirety, and the other mode enables it always to the MUART. This is done when it is necessary to fool the MUART into believing it is always Clear To Send.

Figure 3.1 MPC Block Diagram

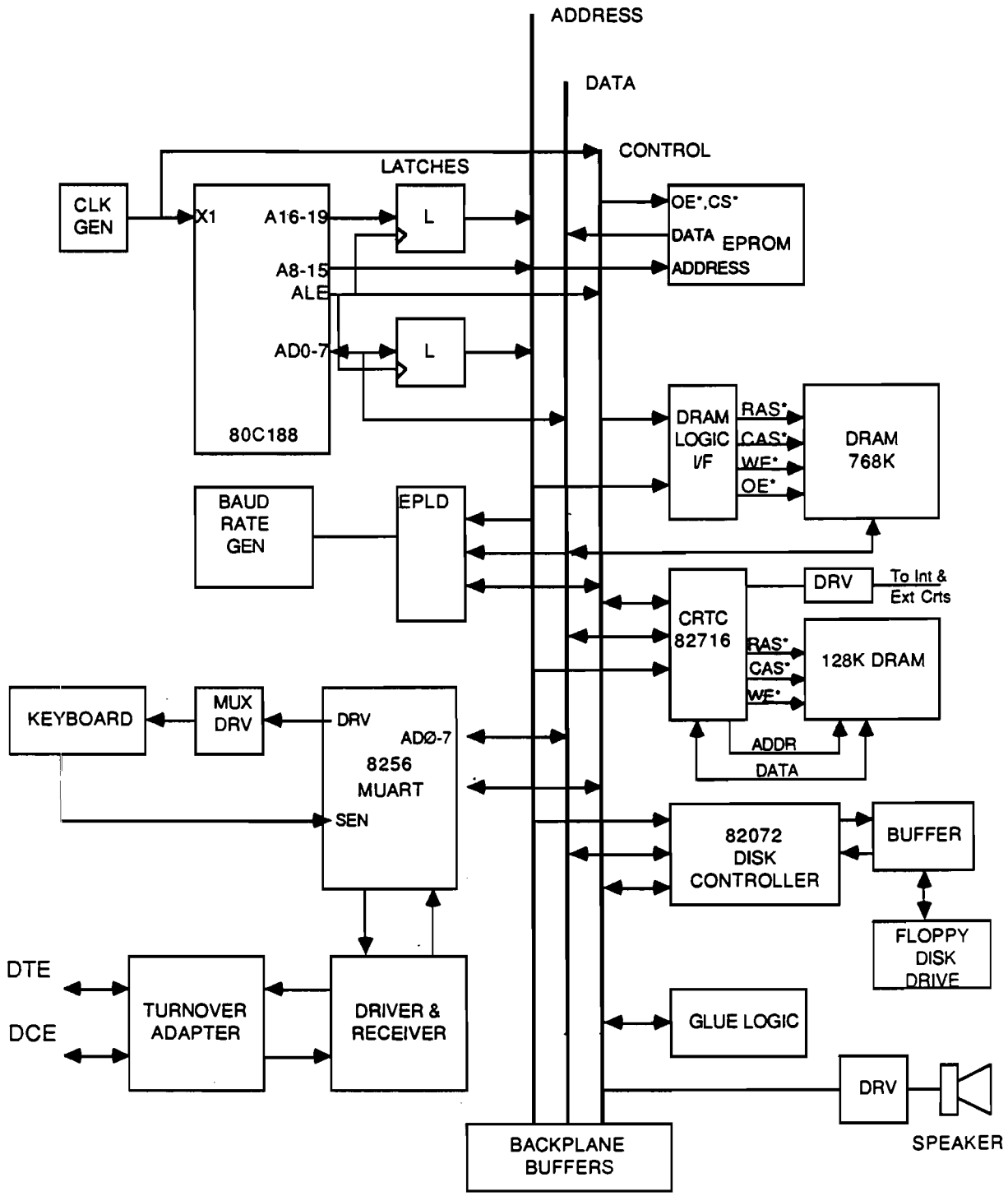


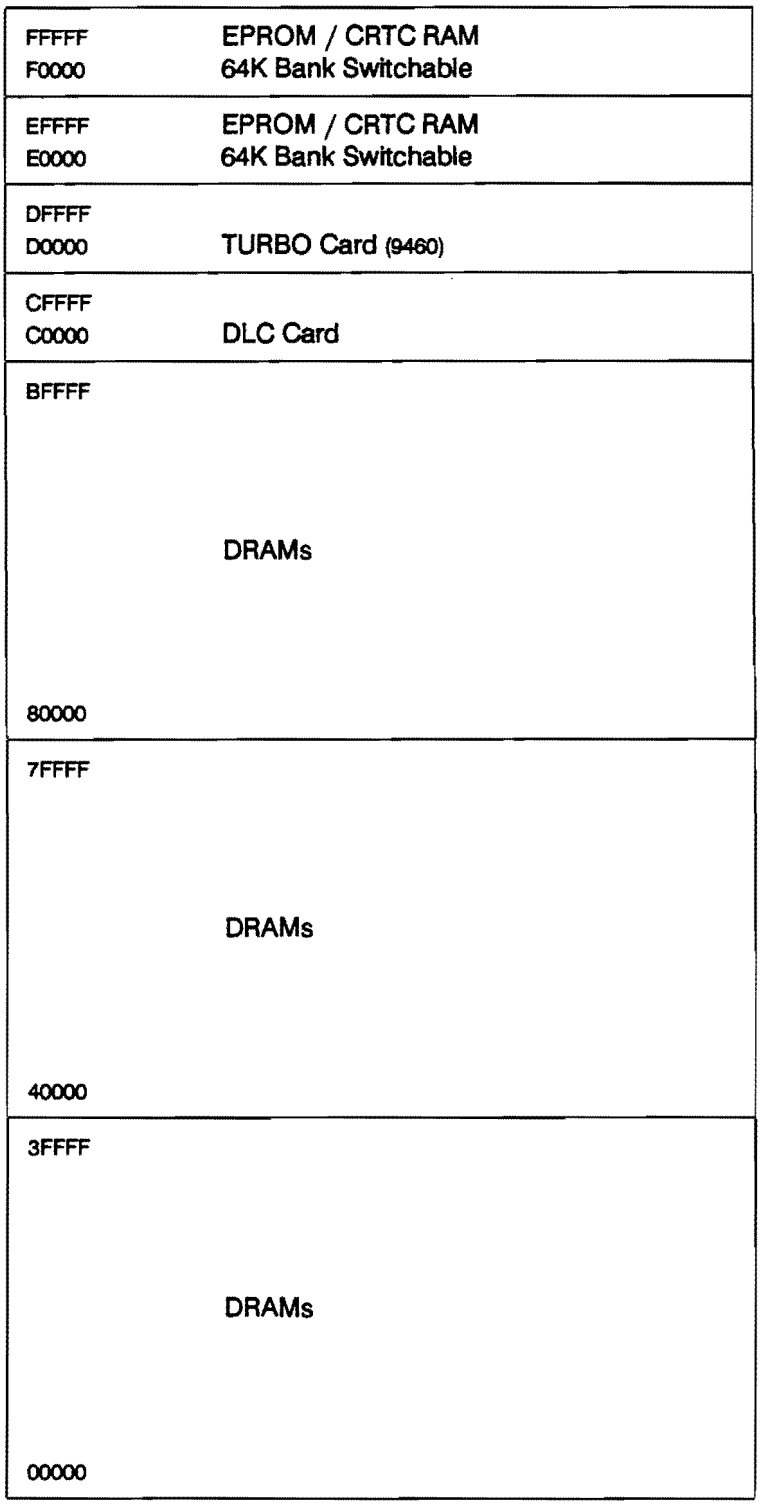
Figure 3.2 MPC I/O Map

FF00 -> FFFF	STAND ALONE DEBUG BOARD
8400 -> FEFF	RESERVED
8000 -> 83FF	CHANNEL ATTENTION TO DLC
7400 -> 7FFF	RESERVED
7000 -> 73FF	HARDWARE RESET TO DLC
4500 -> 6FFF	RESERVED
4400 -> 44FF	PARALLEL PORT 82C55 REG
4300 -> 43FF	TURBO CARD DEBUG BOARD
4200 -> 42FF	REAL TIME CLOCK REGISTER
4100 -> 41FF	SCSI DMA PORT
4000 -> 40FF	SCSI REGISTERS (NOTE 5)
3000 -> 3FFF	RESERVED
1000 -> 2FFF	BATTERY BACKUP SRAM
0300 -> 0FFF	RESERVED (PCS6)
0280 -> 02FF	SEE NOTE 4 (PCS5)
0200 -> 027F	SEE NOTE 3 (PCS4)
0180 -> 01FF	SEE NOTE 2 (PCS3)
0100 -> 017F	82072 FLOPPY DISK CTRL (PCS2)
0080 -> 00FF	SEE NOTE 1 (PCS1)
0000 -> 007F	8256 MUART (PCS0)

NOTE :

1) Write 1 to this port enables CRTC accesses, write 0 to enable EPROM accesses.
2) On reset, /CTS is passed to MUART, write 1 to this port to keep /CTS active, write 0 to this port to pass /CTS to MUART.
3) Reserved for bank switching backplane boards.
4) Read at this port determines which board is on the backplane, 0 = DLC, 1 = TURBO.
5) SCSI stands for Small Computer System Interface, the SCSI DMA ports and registers are for future options such as the Hard Disk in the 9460 Turbo unit.

Figure 3.3 MPC Memory Map



3.2.2 CRT Controller

The CRT controller is a memory-mapped device with a maximum address space of 128k. This private RAM space is only accessible through the CRTC. The MPC can support the simultaneous use of both an internal CRT and an external IBM-compatible TTL monitor. The CRT drive circuitry can operate either an internal TTL or composite CRT. Please note that the components needed to drive a composite CRT are not stuffed and are left only as an option.

3.2.3 Floppy Disk Controller

The 3.5" micro-floppy drive in the unit satisfies two purposes. Firstly, all software and software up-dates become easy and expedient by being disk-based. Secondly, quick data-capture by a fast disk drive makes the data conveniently portable. With a formatted disk capacity of 1.44Mb, the system is capable of both large and high speed data capture. The 82072 floppy disk controller has the ability to transfer data to disk at a rate of 500 Kbits/sec. The MPC can easily support a two drive system should the need ever arise.

The 82072 is a highly integrated floppy disk controller with an on-chip data separator, a precompensation delay write circuit, a crystal oscillator and a 16-byte FIFO. The FIFO is filled or emptied via DMA transfers for disk write or read operations, respectively. DRQ0 is reserved for 82072 DMA requests and the DMA acknowledge is done by accessing port 101H. The external terminal count (TC) input is not used to end DMA transfers. Rather, it is implicitly supported through the use of the underrun/overrun and end-of-track functions. The only difference between the two methods is the latter will return an "abnormal termination" message, which can be ignored.

A description of the interface signals between the controller and the disk drive is given in section 3.8.3. The presence of the 100 ohm series resistors in the vicinity of the floppy disk controller and the CRTC is to dampen out destructive voltage undershoots.

Jumpers are used in the vicinity of the disk-signal connector to allow for the interchangable use of both Sony and Epson drives. The default configuration is set to accommodate the Sony drive.

3.2.4 Support Logic

Erasable programmable logic devices (EPLD) were used to confine and, thereby, reduce the overall board area. Simple operations such as generating chip selects to EPROM, DRAM, disk drive selects, SRDY, and the baud rate clock for the 8256 MUART were easily implemented. Thus, a single EPLD replaced five 14-pin I.C.s in performing the same functions. Because the operational speed of EPLD's are still relatively slow, as compared to discrete 74HCXX's, only non-speed critical logic were replaced. It is for this reason that the DRAM RAS and CAS signals were implemented by fast, discrete 74ACXX series of CMOS logic and not by an EPLD. Rigid timing constraints imposed by the processor and the memory chips forced the migration to advanced CMOS logic.

3.2.5 Shared RAM Bus

All the necessary processor signals for the backplane cards are made available on the backplane. These cards are memory-mapped with reference to the 80C188 and communication can be done through a shared memory area or by interrupts. The address decoding is the responsibility of the backplane cards. The data bus buffer-enabling is handled simply by an eight-input AND gate and a straight-forward concept. That is, the data buffer should be enabled when the processor's /DEN signal is active AND the processor is not accessing any of the MPC-based devices. PCS5 on the backplane is used for board ID, specifically DLC-type identification (DLC = 0, Turbo = 1). PCS4 is used for bank-switching. That is, by writing a code to a particular board, its interface can be enabled for communication with the MPC. There can be many boards at the same address range and their activity is mutually-exclusive, as indicated in the memory map. The general voltage level for the backplane drivers and receivers are the following : Vih(min) = 2.1 V, Vil(max) = 0.9 V @3 V Voh(min) = 3.8 V, Vol(max) = 0.44 V @4.5 V.

3.2.6 Keyboard And Serial Port Control

The keyboard and serial port controls were implemented by using a 8256 MUART. The MUAR contains two parallel ports, a UART, five counter/timers, and an interrupt controller. The UART ca perform the dual function of either emulating a terminal port or a printer port, but not both. This i due to the fact that both ports share the same control lines but have different external connector Basically, a turn-over adapter is implemented here. These two ports are located on the transitio board along with the speaker and the reset button. The line driver is a standard 1488 but the lin receiver is a 74HC14 with a resistor network to step down the voltage and to current limit the inpu signal. The two parallel ports are used for the keyboard interface. As nine keyboard lines ar driven by one port on the MUART, the other eight lines are ready to sense the response of th keyboard on the other port. The keyboard consists of a simple, X-Y grid matrix in which eac intersection represents a keyboard key. As one axis of the matrix is driven by the MUART, a ke depression would result in a row and column connection and be detected by the MUART's "sense lines. A simple translation table can determine the ASCII value of the depressed key. Electrostati discharge (ESD) protection has also been added to guard against potentially harmful electri shocks from the user through the keyboard. This protection takes the form of buffers an clamping diodes. Since the MUART can also perform the function of an external interru controller, all MPC-based interrupts are channelled into it and a global interrupt can be raised t the processor on interrupt 0. The floppy disk controller interrupt and the "disk change" signals ar the only signals funnelled into the MUART.

3.3 DATA LINK CONTROLLER

The Data Link Controller (DLC) is a data acquisition card which resides on the backplane at its address on the memory map. It is a slave processing card just like any other non-MPC card on the backplane. The core of the DLC consist of the processor, the share RAM interface, the Serial Communication Controller (SCC), the Transparent Synchronous Receivers (TSR), and the Test Port Interface Controller (TPIC). Figure 3.4 is a block diagram of the DLC board and detail description of these various function blocks are described in the following sections.

3.3.1 Shared RAM Interface Bus

The DLC is a slave processor card which communicates with the MPC through 32k shared static RAM, int 1 to the MPC and a Channel Attention (CA) signal to the DLC processor which is an 8 Mhz 80188. The arbitration between the DLC and the MPC for use of shared RAM is accomplished by a Gate Array Logic (GAL). Should simultaneous requests for the shared RAM occur, the DLC is given priority. The LOCK signals from the two processors are also used in the arbitration scheme. The reason it is used is not because the bus arbiter is not sound but because the two processors are operating at two different speeds (one being 50% faster than the other). There is the possible scenario where the DLC is attempting a word read from the shared RAM and the MPC sneaks in between the byte reads and accomplishes a word write to that same address. In this case, the DLC will incorrectly read the word. This LOCK signal should be active at the same time as any shared RAM accesses. Using LOCK with any memory accesses guarantees exclusive use of the shared RAM. The address decoding of the DLC's address is done by a GAL16V8-15. A GAL was chosen for the purpose of using a fast, re-programmable part in case the address range needs to be changed. At the time of implementation, EPLDs were not fast enough to do the job. Channel Attention (CA) is also generated by the GAL from a particular I/O access. The DLC also contains a board ID. This ID can be read by reading PCS5 which should return a zero.

3.3.2 Microprocessor

The CPU chip on the DLC is an 8 Mhz 80188 which has 32k of private CMOS static RAM and 32k of EPROM code (see figure 3.5 DLC memory map). The processor can be driven by either a 24 MHz or 16.128 MHz clock. The default frequency is 16.128 MHz. It was made jumper selectable in the event that the processor can be up-graded to 12 MHz in the future. If the processor speed is increased then the 16.128 MHz clock must be jumpered to the TPIC and the Serial Communication Controller SCC must operate based on the external clock.

Figure 3.4 DLC Block Diagram

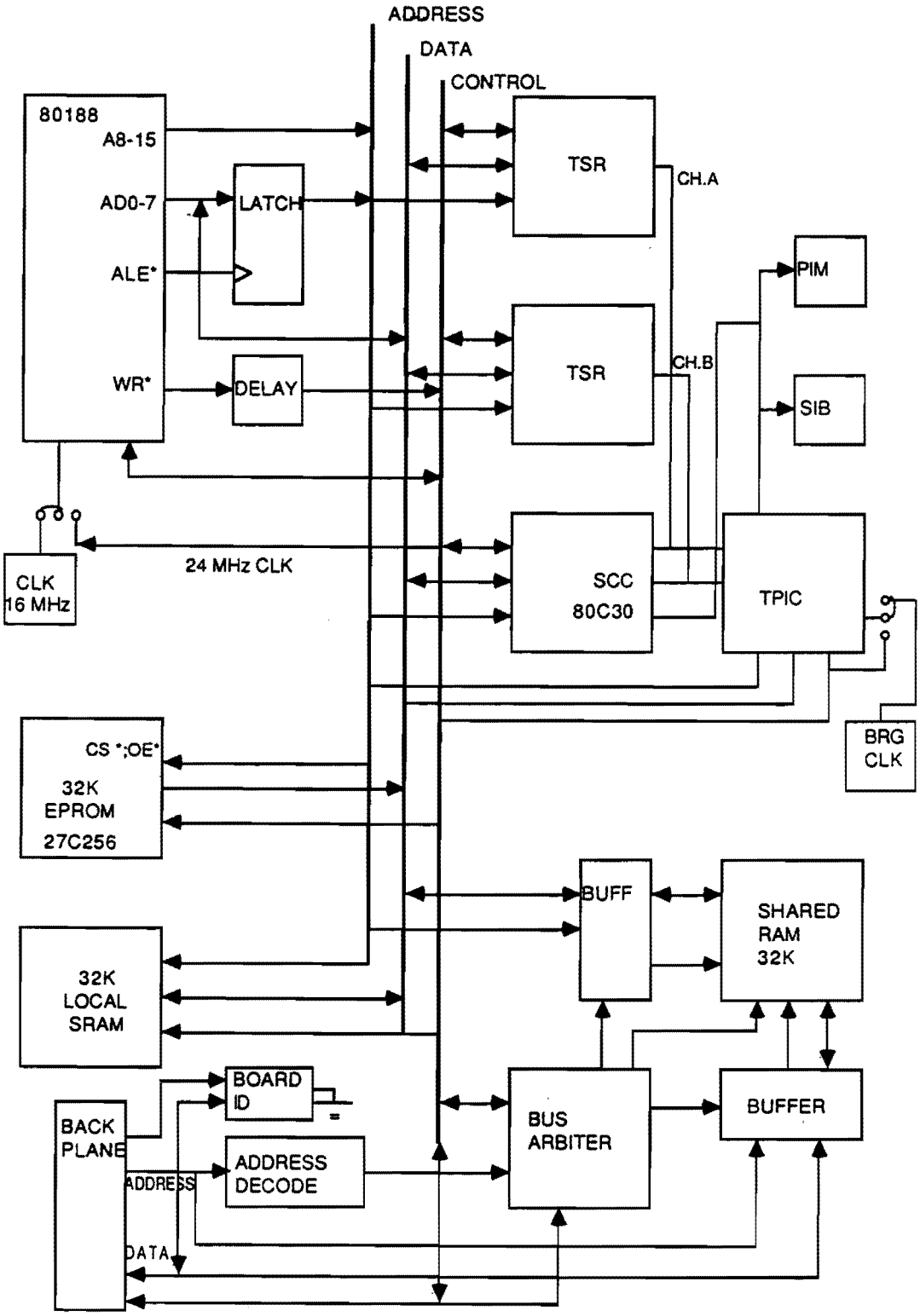
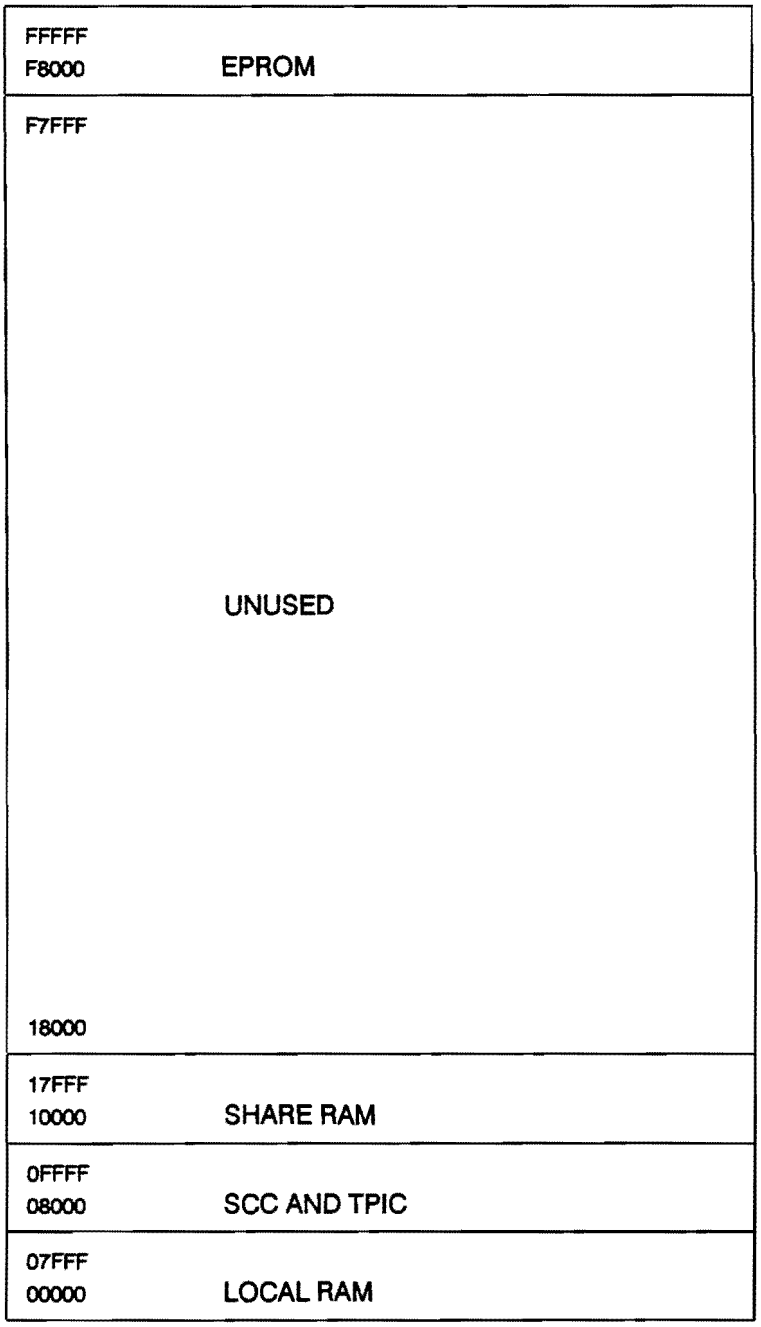


Figure 3.5 DLC Memory Map



3.3.3 PIM/SIB Interface

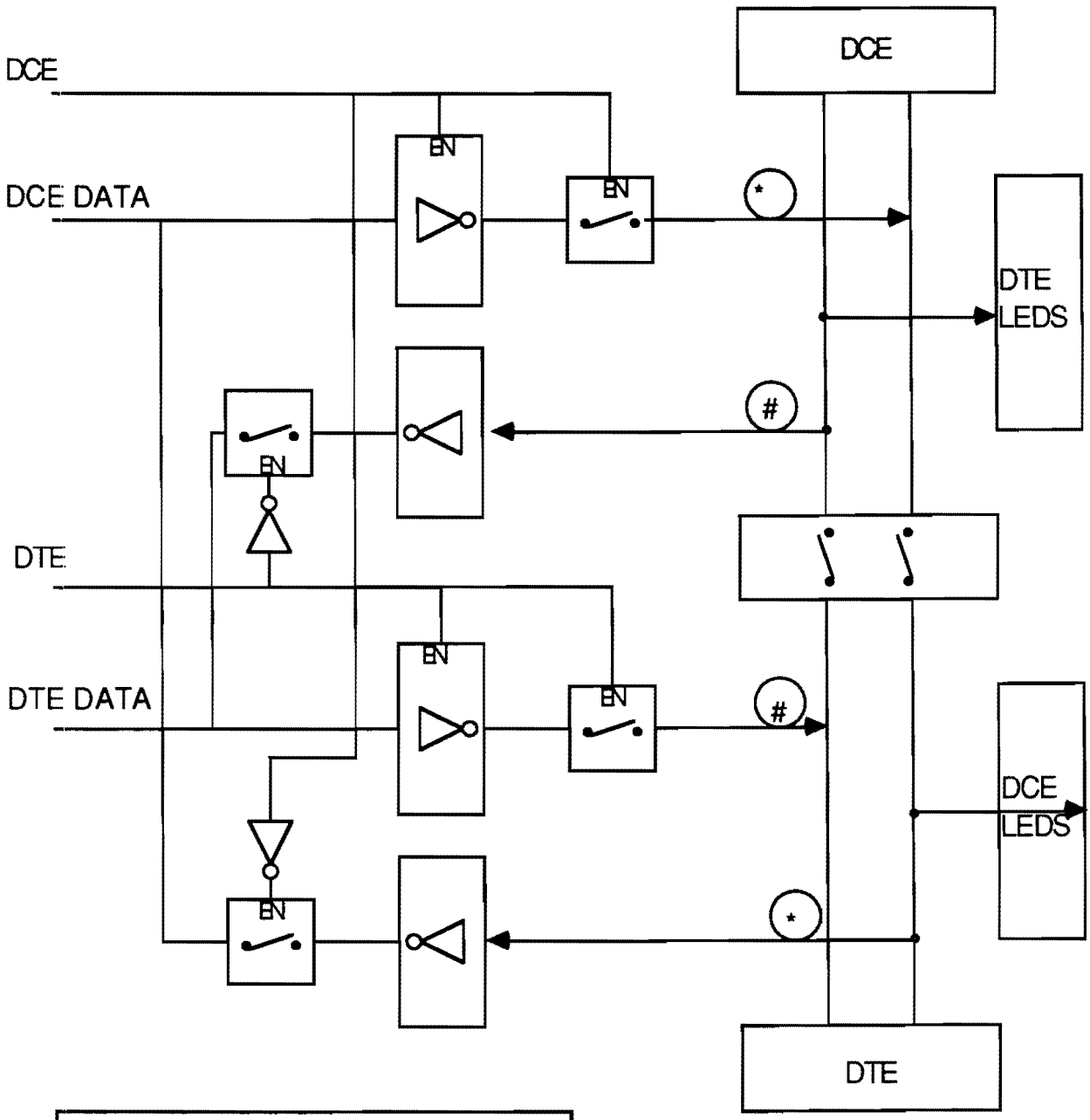
Any NAVTEL PHYSICAL INTERFACE MODULE (PIM) for the NAVTEL DT5B can be attached to the PIM port. If a PIM is not attached then the SIB is used. The line drivers for the SIB port includes reed relays for physical separation from the lines (see figure 3.6). This is required to avoid electrostatic damage to the switches as was the case in using analog gates. The line receivers were implemented with 74C914s and resistor networks in the same way as in the MPC. The DLC/SIB interface and the SIB block diagram must be examined at the same time rather than separately schematic-wise. The entire SIB section is controlled by two signal lines from the TPIC, that is DCE and DTE. When emulating either DCE or DTE, that signal line must be active and the other line must be inactive. That is, when emulating a DCE, DCE = 1 and DTE = 0. When line-monitoring is required, both DCE and DTE must be inactive. The case of both DCE and DTE being active represents a total inactive state. In summary, the unit will drive the appropriate signals lines when emulating the respective data equipment type and also properly receive the conjugate signal lines. The line-monitoring condition is a non-intrusive surveillance of the lines.

3.3.4 Test Port Selection

On power up, the DLC reads the PIM ID bits (N.B. 111b = no PIM). If no PIM is attached, then the built-in RS-232C test port is used, otherwise the attached PIM is used.

Whenever an attached PIM is used the entire PIM bus is driven onto the built-in test port. In this way the local LED indicators always reflect the state of the test interface in actual use. All breakout switches on the built-in test port must be closed and all customer equipment must be attached to the PIM rather than the built-in test port. Note that this mode of operation is the conjugate of MON. The modes of operation for the built-in test port may be summarized as DCE, DTE, MON & PBD (ie.PIM Bus Display). (N.B. the SIB has been designed to decode PBD mode as the equivalent of MON except that the SIB PIM bus drivers are all disabled.)

Figure 3.6 DLC INTERFACE AND SIB BLOCK DIAGRAM



* RD,CTS,DSR,CD,RC,TC,RI,SQ

TD,RTS.DTR,XTC

3.3.5 Test Port Interface Controller

The TPIC (Test Port Interface Controller) is the interface controller chip developed by NAVTEL to control the signal flows from either the Physical Interface Module (PIM) port or the Status Indicator Board (SIB) port through to the SCC.

3.3.5.1 Test Mode Supported by the TPIC

The TPIC supports the following functions :

(1) The usual DTE/DCE/MON interface modes are supported. The tests run on either the built-in RS-232C test port or an external PIM.

(2) Software selectable sources are provided for the SCC's /RTXCA and /RTXCB inputs.

(3) Generate 2 timer gates to facilitate pulse width measurement.

(4) General purpose parallel port.

(5) General purpose interrupt inputs.

3.3.5.2 DCE/DTE And Monitor Mode Support

The signals DCE/DTE, MON, DCE, DTE from the TPIC are used to control the direction of signals on the PIM bus. Assertion of MON sets all signals as inputs. Negation of MON allows DCE/DTE to control the direction of signals (see section 3.8.6.).

3.3.5.3 Clock Multiplexing

By setting bits 4 and 5 of the TPIC configuration register, one of four possible clock sources is selected for the SCC /RTXCA input. The function of the control bits are as follow :

Bit 5 (select 1)	Bit 4 (select 0)	Clock Selected
0	0	X10 pin of the TPIC is selected (ie. 3.6864 MHz)
0	1	X20 pin of the TPIC is selected (3.78752 MHz)
1	0	XTC pin of the TPIC is selected
1	1	TC pin of the TPIC is selected

By setting bits 2 and 3 of the TPIC configuration register, one of four possible clock sources is selected for the SCC /RTXCB input. The function of the control bits is as follows :

Bit 5 (select 1)	Bit 4 (select 0)	Clock Selected
0	0	X10 pin of the TPIC is selected (ie. 3.6864)
0	1	X20 pin of the TPIC is selected (3.78752 MHz)
1	0	XTC pin of the TPIC is selected
1	1	RC pin of the TPIC is selected.

By setting bits 0 and 1 of the TPIC configuration register, one of four possible clock sources is selected to output on the TPIC XTC pin :

Bit 5 (select 1)	Bit 4 (select 0)	Clock Selected
0	0	TRXCA pin of the TPIC is selected.
0	1	TRXCB pin of the TPIC is selected.
1	0	low logic level (ie. SPACE)
1	1	high logic level (ie. MARK)

3.3.5.4 Pulse Width Measurement

The TPIC contains a subsystem to generate 2 timer gates to facilitate pulse width measurement (PWM) using timers 0 & 1 on the 80188 CPU chip. The pulse width measurement circuit has the following characteristic :

-the timebase is 2.016 MHz.

-the results returned is 16 bits wide.

-the triggering edge will be fixed to an ON/OFF transition.

-the TC EX-OR RC source allows measurement of the phase difference between RC & TC (any progressive change in result values between repeated samples over time indicates that a frequency difference exists).

Writing the desired pulse source control bits to the PWM register in the TPIC will arm the pulse width circuit to begin measurement on the ON/OFF transition of the selected source on the PIM bus.

The selector bits are encoded as follows:

PWM Select 2	PWM Select 1	PWM Select 0	Source Selected
0	0	0	XTC from PIM bus
0	0	1	TC from PIM bus
0	1	0	RC from PIM bus
0	1	1	TC EX-OR RC
1	0	0	TD from PIM bus
1	0	1	RD from PIM bus
1	1	0	IR0, interrupt request input to TPIC
1	1	1	IR1, interrupt request input to TPIC

When the selected source generates an ON/OFF transition, the signal TG0 goes high which enables the timer responsible for the OFF phase duration measurement. When the source subsequently generates an OFF/ON transition, TG0 goes low and TG1 goes high which disables the OFF duration timer and enables the timer responsible for the ON phase duration measurement. Finally, a second ON/OFF transition causes TG1 to go low which disables the ON duration timer.

The PWM interrupt goes high at this point to inform the CPU that the 2 timers now hold the duration counts for the selected signal. The interrupt is cleared by either re-arming the PWM circuit or masking out the PWMINT interrupt source by setting the interrupt mask register in the TPIC.

3.3.5.5 General Purpose Parallel Port

A general purpose bytewide port is provided on the TPIC to ease implementation of such features as PIM ID determination, X.21 & ISDN hardware support. Each port bit direction is individually programmable via a data direction register for maximum flexibility.

Any port bit configured as an input can read its current pin state transparently and will not be affected by a write.

Any port bit configured as an output shall latch the current state to its pin during the active phase of the write strobe (ie. /CS./WR) & will read back the current state on its pin.

The type of external Physical Interface Module attached (if any) may be determined by examining the port bits assigned to the PIM ID inputs. These port bits must be configured as inputs. The PIM id. codes are as follows:

PID	PID	PIDO	PIM Interface Type
0	0	0	RS232/MIL188
0	0	1	V.11
0	1	0	RS449
0	1	1	V.35
1	0	0	Unassigned
1	0	1	Unassigned
1	1	0	Unassigned
1	1	1	No PIM attached. Default to built-in RS-232C test port

A transition detector is included to generate a STATUS CHANGE (STCHG) interrupt whenever a port bit changes state. A STCLK input pin is provided to set the sampling period for the transition detector. The STCHG interrupt must be acknowledge by reading the port to determine the current pin states.

A read of any even chip address will provide the CPU with the current data on the port pins. Note that reading the PIO at address 2 also resets the STCHG interrupt (ie. a read of addresses 0, 4 or 6 does not reset the STCHG int.).

Note that the STCHG interrupt is fully maskable by setting the appropriate bit in the interrupt mask register in the TPIC.

3.3.5.6 General Purpose Interrupt Inputs

A pair of dedicated interrupt inputs are provided to support the TSR ASIC. These pins (IR0 & IR1) are level sensitive inputs which funnel through the interrupt mask register (IMR) to the global interrupt output pin (INT). IR0 & IR1 are also PWM sources.

3.3.5.7 TPIC Pinout (68-pin PLCC)

Pin #	Description
1,35	VDD. The +5V power pins.
2,18,34,51	VSS. The GND power pins.
65->68	D0->D3.
3->6	D4->D7. The 8-bit bidirectional data bus.
23->25	A0->A2. Address line inputs.
30	/CS. Chip select input.
29	/RD. Read strobe input.
28	/WR. Write strobe input.
11,12	IR0,IR1. General purpose interrupt inputs & PWM sources.
31	RESET. All write registers are cleared, all programmable I/O pins go to a high impedance state and the INT pin assumes the test out function.
45	INT. Global interrupt (& test out during reset) output.
46,47	TG0,TG1. External timer gate outputs for PWM.
8	X10. The 3.6864 MHz crystal oscillator input.
7	X20. The 3.78752 MHz crystal oscillator input.

3.3.5.7 TPIC Pinout (68-pin PLCC)

Pin #	Description
19->22	/RTS,/DTR,/CTS,/CD. Tristate output buffers for SCC-originated modem control signals to the PIM bus. As a DTE, /RTS & /DTR are enabled. As a DCE, /CTS & /CD are enabled. All are disabled in MON mode.
13->17	XTC,TC,RC,TD,RD. Clock & data signals. As a DTE, XTC & TD are outputs while TC,RC & RD are inputs. As a DCE, TC,RC & RD are outputs while XTC & TD are inputs. All are inputs in MON mode. All are available as PWM sources in any mode.
50	DCE/DTE. Unless over-ridden by MON, dedicated PIM bus signal directions are controlled by the state of this output.
48,49	DTE,DCE. Individually decoded external device tristate control outputs. Normally controlled by DCE/DTE.

3.3.5.8 TPIC Address Map

Addr	Read	Write	Description
0	PIO	CONF	PIO = Port Input/Output, CONF = CONFiguration reg.
1	IRR	DDR	IRR = Interrupt Request Reg. DDR = Data Direction Reg.
2	PIO*	PIO	* a read at this address will reset STCHG interrupt.
3	IRR	IMR	IMR = Interrupt Mask Reg.
4	PIO	PWM**	** a write to this port will reset the PWM interrupt. PWM = Pulse Width Measurement.
5	IRR	N/A	N/A = no action.
6	PIO	N/A	
7	IRR	N/A	

3.3.5.9 TPIC Register Description

1. PIO: **(read/write)** see section 3.3.5.5.

2. DDR: **(write only)**

Bitwise tristate control of the port output drivers is performed by the DDR. A 1 written to a DDR bit enables the corresponding PIO output latch driver. All DDR bits are cleared during reset, which disables all PIO pin drivers.

3. CONF:**(write only)**

bit	7	=	MON
bit	6	=	DCE/DTE
bit	5	=	RTCAS1
bit	4	=	RTCAS0
bit	3	=	RTCBS1
bit	2	=	RTCBS0
bit	1	=	XTCS1
bit	0	=	XTCS0

MON bit, **if set**:

- the DTE & DCE pins are reset unless over-ridden by PIMSEL.
- The PIM bus pins TD, RD, RTS, CTS, CD, TC, RC, DTR & XTC are high impedance.

If reset:

- The DTE & DCE pins decode DCE/DTE normally unless over ridden by PIMSEL.
- The direction of the PIM bus pins TD, RD, RTS, CTS, CD, TC, RC, DTR & XTC depends on the condition of DCE/DTE bit. Also see section 3.8.6
- N.B. The PIM bus signals DSR, SQ & RI are mapped over to the PIO, and are managed separately.

DCE/DTE bit, **if set**:

- The DTE pin is reset unless over-ridden by PIMSEL.
- The DCE pin is set unless over-ridden by MON.
- The PIM bus pin drivers for RD, CTS, CD, TC & RC are enabled unless over-ridden by MON.

If reset:

- The DTE pin is set unless over-ridden by MON.
- The DCE pin is reset unless over-ridden by PIMSEL.
- The PIM bus pin drivers for TD, RTS, DTR & XTC are enabled unless over-ridden by MON.

Bits 0 to 5 are clock source select lines, see section 3.3.5.3 for detail description.

4. PWM:(**write only**)

bits	4	to	7 are not used.
bit	3	=	PIMSEL
bit	2	=	PWMS2
bit	1	=	PWMS1
bit	0	=	PWMS0

PIMSEL, **if set**:

- The DTE & DCE pins are set.

- All built-in test port RS-232 drivers are enabled.

If reset:

- The state of the DTE & DCE pins follow the condition of the DCE/DTE bit in the configuration register. See above.

PWMS2,PWMS1,PWMS0 bits select 1 of 8 sources for the PWM logic as per section 3.3.5.4.

NOTE : Writing to the PWM register resets the PWM interrupt and re-arms the PWM logic.

5. IMR:(write only)

bits	4	to	7 are not used.
bit	3	=	STCHG
bit	2	=	PWM
bit	1	=	IR1
bit	0	=	IR0

A set bit enables the corresponding interrupt to the global INT output pin and makes that interrupt visible when the IRR is read. A reset bit disables the corresponding interrupt channel.

STCHG - see 3.3.5.5
PWM - see 3.3.5.4
IR1 - see 3.3.5.6
IR0 - see 3.3.5.6

6. IRR:**(read only)**

bits		4 to 7 are not used.	
bit	3	=	STCHG
bit	2	=	PWM
bit	1	=	IR1
bit	0	=	IR0

A set bit indicates a pending enabled interrupt.

3.3.5.10 CPU Interface Rules

The data bus interface is designed to work with both Intel & Motorola style CPUs. Intel bus timing will not be elaborated on here. Motorola bus timing is accommodated by tying /RD low, /WR to R/W, and /CS to /E qualified by address.

Read/write access & tristate enable/disable times are very fast and offer 0 wait state performance when interfacing with foreseeable generations of familiar CPUs. The chip simulation reports the worst-case propagation delay to be 75 ns. for the slowest path on the chip.

The address must be stable for the entire duration of a TPIC read or write access. Data from the CPU to the TPIC must be stable for the entire duration of a TPIC write access.

Although the TPIC has not been characterized in the way that we are accustomed to seeing in peripheral chip data sheets, the following assumptions for A.C. timing are valid:

Address setup/hold time to/from /CS.(/RD+/WR) > = 0 ns.
Data setup/hold time to/from /CS./WR > = 0 ns.
Read access time < = 75 ns.
/CS.(/RD+/WR) pulse width > = 75 ns.
/CS.(/RD+/WR) recovery time > = 75 ns.
Clock high/low times > = 30 ns. (any pin which receives a clock)
Input signal rise/fall times < = 20 ns.
Clock frequency < = 10 MHz (any pin which receives a clock)

3.3.6 Serial Communication Controller

A 80C30 SCC (Serial Communication Controller) is used on the DLC board. Details on theory of operation of this IC will not be included in this manual. For detial information on the 80C30 please refer to Zilog data sheet. This section will concentrate instead on the how the 80C30 is used in this particular application.

In general, Ch.A signals from the SCC are mapped to DTE functions & Ch.B signals to DCE functions. A detailed summary follows:

SCC pins	RS-232C pin
TxDA(15), RxDA(13)	TD(2)
TxDB(25), RxDB(27)	RD(3)
/RTSA(17), /DCDA(19)	RTS(4)
/DTRB(24), /CTSA(18)	CTS(5)
/RTSB(23), /DCDB(21)	CD(8)
/TRxCA(14), /RTxCA(12)	TC(15)
/TRxCB(26), /RTxCB(28)	RC(17)
/DTRA(16), /CTSB(22)	DTR(20)

For clocking requirements, software selectable sources are provided by the TPIC to the SCC's /RTXC inputs. The sources include the appropriate 1X clock on the test interface and 3.6864 MHz & 3.78752 MHz crystal oscillators external to the TPIC (see section 3.3.5.3).

The SCC's PCLK runs at 8.064 MHz.

The SCC's /TRxC pins will provide a 1X clock in phase-alignment with the test application. Internally, the SCC is capable of looping-back a 1X clock from the /RTxC pin, sourcing a 1X clock from the internal Baud Rate Generatot (BRG), or sourcing a 1X clock from the internal receive DPLL.

The 3.78752 MHz crystal frequency is used to generate 1X & 32X clocks for 110 & 134.5 bps operation.

The 3.6864 MHz crystal frequency is used to generate 1X & 32X clocks for 50, 75, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, 9600, 14400 & 19200 bps operation.

The 8.064 MHz crystal frequency (PCLK) is be used to generate 1X clocks for 38400, 48000, 56000, 57600, 64000 & 72000 bps operation.

NOTE : the 32X clocks are required only in BOP/NRZI reception & some async (eg. 1.5 stop bits or no 1X clock available) applications.

3.3.7 Transparent Synchronous Receiver

3.3.7.1 Test Interface Requirements

The primary purpose of this chip is to monitor "outsync data" on a modem link. Outsync data is defined as the data between the "outsync character(s)" sent at or near the end of the previous frame and the opening sync characters sent at the beginning of the next frame.

The receivers in the SCC must either be hunting for the opening sync pattern (ie. the receiver(s) are in standby) or in sync and receiving with optional sync character stripping (ie. the sync pattern only forces bit alignment when the receiver is in hunt). Determining the number of interframe flags while running the SCC in BOP modes requires external hardware. These restrictions inherent in use of the SCC are, in general, true of any multi-protocol serial communications controller.

The purpose of the TSR (Transparent Synchronous Receiver) is to run in parallel with an SCC and provide the hidden outsync data. This is possible because the TSR is designed such that there is no distinction between hunt and normal receive modes. The data is received anytime there is a clock present and the receiver re-syncs anytime the programmed pattern has been detected.

Bit alignment, normal receive data or sync, and receiver overrun status is available from the TSR on a character-by-character basis. The character length is programmable between 1 and 8 bits. The sync pattern is programmable between 1 and 16 bits with programmable "don't care" bits anywhere within the overall 16-bit sync pattern.

The TSR is capable of receiving NRZ or NRZI encoded data. Leading zeroes are automatically added into the received character (as far as the CPU is concerned) whenever the programmed receive character length is less than 8 bits (this relieves the CPU from masking out extra bits in software).

The TSR may use the on-chip sync pattern detection circuit or an external sync detector (if a sync pattern longer than 16 bits must be accommodated).

3.3.7.2 TSR Pin Description

Pin #	Description
13, 24	VDD. The +5V supply pins.
1, 12	VSS. The GND pins.
20->23	D0->D3.
2->7	D4->D7. The bidirectional CPU interface data bus.
6->8	A0->A2. Address input bus from the CPU.
9	/CS. Chip select input.
10	/RD. Read strobe input.
11	/WR. Write strobe input.
14	RXC. Receive clock input. RXD is clocked in on the rising edge of RXC.
15	RXD. Receive data input. May be encoded NRZ or NRZI.
16	/ESYNC. Externally-generated sync input.
17	RESET. Chip reset input.
18	TEST. Factory test mode input.
19	INT. Interrupt output.

3.3.7.3 TSR Register Address Map

Addr	Read	Write	Description
0	SREG	LSYNC	SREG = status register LSYNC = low sync register
1	RCHAR	HSYNC	RCHAR = received character HSYNC = high sync register
2	SREG	LMASK	LMASK = low mask register
3	RCHAR	HMASK	HMASK = high mask register
4	SREG	CREG	CREG = control register
5	RCHAR	N/A	N/A = no action
6	SREG	N/A	
7	RCHAR	N/A	

3.3.7.4 Register Description

1. SREG:**(read only)**

bits	6	&	7 are not used
bit	5	=	RXOR
bit	4	=	RXCA
bit	3	=	SYRX
bit	2	=	RXL2
bit	1	=	RXL1
bit	0	=	RXL0

RXOR (Receiver Overrun) :

- becomes set if RCHAR was not read in time to prevent some loss of data between 2 successive character boundary or sync events.
- is reset by a read of RCHAR.

RXCA (Received Character Available) :

- becomes set by a character boundary or sync event.
- is reset by a read of RCHAR.

SYRX (Sync Received) :

- becomes set by a sync event
- becomes reset by a character boundary event with no sync coincidence.

RXL2,RXL1,RXL0 (Received Character Length) :

- indicates the width (= RXLn+1) of the character available in RCHAR.

2. RCHAR:(**read only**)

The received character is read with the LSB (ie. 1st bit rec'd) aligned with bit 0. If the programmed receive character length is less than 8 bits, then the dummy MSBs are automatically zero-filled.

Reading RCHAR resets the RXOR and RXCA bits in SREG and also resets the INT pin.

3. LSYNC,HSYNC:(**write only**)

A sync pattern of up to 16 bits in length may be programmed by writing to the respective sync registers. In all cases of sync pattern length, the MSB (ie. the last bit sent) of the pattern must be aligned with HSYNC.7 inorder to guaranty LSB alignment of the received characters subsequently read from RCHAR. If parity is used, then the programmer must allow for the appropriate bit field insertions in preparing the final data to be written to the sync registers. The excess bits (ie. for sync pattern lengths < 16 bits need not be assigned any particular value because they will be aligned with cleared mask bits in the appropriate LSBs of the mask registers. LSYNC & HSYNC are not affected by reset.

4. LMASK,HMASK:(**write only**)

A "don't care" mask for the sync pattern allows parity insensitive sync pattern recognition and sync pattern length control. A 1 written to a mask register bit enables the corresponding sync register bit for pattern matching while a 0 written makes the same bit a "don't care". The appropriate LSBs of the mask registers must be programmed with zeros when the desired sync pattern length < 16 bits.

If all mask bits are reset, then an interrupt with the RXCA and SYRX set in SREG will occur after every rising edge of RXC.

LMASK & HMASK are not affected by reset.

5. CREG:**(write only)**

bits 6 & 7 are not used
bit 5 = ESYNCE
bit 4 = INTE
bit 3 = NRZI
bit 2 = RCL2
bit 1 = RCL1
bit 0 = RCL0

ESYNCE (External sync enable) :

- if set, the /ESYNC pin provides character synchronization.

- if reset, the internal sync pattern detection logic provides character synchronization.

INTE (Interrupt enable) :

- enables/disables (1/0) assertion of INT after a sync or character boundary event.

NRZI (RXD decoding format) :

- selects NRZI/NRZ (1/0) data reception.
  RCL2,RCL1,RCL0 (Programmed receive character width) :

RCL2, RCL1, RCL0 (Programmed receive character width) :

- character width = RCLn+1 (eg. RCLn = 4 for 5 bit characters).

- 0 < range < 9

3.3.7.5 TSR Operation

The receive data is single-buffered (ie. there is no FIFO). Accordingly, the TSR interrupt must be serviced quickly to prevent receiver overruns. The most time-critical scenario is when a normal character has been received on the previous clock rising edge and sync pattern matching is satisfied on the next clock rising edge. Less than 1 bit time response latency is required of the CPU (This is not as bad as it may sound because in effect the previous received character overlapped the sync pattern by all but 1 bit and was therefore a redundant preview of the MS sync pattern byte). In steady-state character synchronization, the CPU response latency must not exceed the programmed (receive character width -1) bit times. When operating in parallel with an SCC, the TSR will invariably respond to events on the test interface ahead of the SCC due to a lack of FIFOs, microcode delays, & serial delay lines.

The normal sequence of events is as follows:

1) powerup reset.

2) sync & mask programming.

3) mode programming.

4) normal receive interrupts, discard data because of indeterminate character alignment, SCC in hunt mode.

5) sync interrupt, character alignment is now established, buffer SCC data.

6) normal receive interrupts, discard TSR data until outsync characters are read from the SCC.

7) normal receive interrupts, buffer TSR data, SCC in hunt mode.

8) sync interrupt, discard TSR data, buffer SCC data, GOTO step 6).

In steady-state character synchronization, the RXLn bits must always match the programmed RCLn value, otherwise a hardware error has occurred (ie. this should never happen).

In all cases the RXLn bits must be < = the programmed RCLn value, otherwise a hardware error has occurred (ie. this should never happen).

In all cases the RXLn bits report the RCHAR bit position received when the sync or character boundary event occurred.

The sequence of events for each interrupt is as follows:

1) a rising edge on RXC causes a sync or normal receive interrupt.

2) the CPU reads SREG to determine the nature of the interrupt.

3) the CPU reads RCHAR, the interrupt is reset.

3.3.7.6 MPU Interface Rules

The data bus interface is designed to work with both Intel & Motorola style MPUs. Intel bus timing will not be elaborated on here. Motorola bus timing is accommodated by tying /RD low, /WR to R/W, and /CS to /E qualified by address.

Read/write access & tristate enable/disable times are very fast and offer 0 wait state performance when interfacing with foreseeable generations of familiar MPUs (the chip simulation reports the worst-case propagation delay to be 71 ns. for the slowest path on the chip).

The address must be stable for the entire duration of a TSR read or write access. Data from the CPU to the TPIC must be stable for the entire duration of a TSR write access.

Although the TSR has not been characterized in the way that we are accustomed to seeing in peripheral chip data sheets, the following assumptions for A.C. timing are valid:

Address setup/hold time to/from /CS.(/RD+/WR) > = 0 ns.
Data setup/hold time to/from /CS./WR > = 0 ns.
Read access time < = 71 ns.
/CS.(/RD+/WR) pulse width > = 71 ns.
/CS.(/RD+/WR) recovery time > = 71 ns.
Clock high/low times > = 30 ns. (any pin which receives a clock)
Input signal rise/fall times < = 20 ns.
Clock frequency < = 10 MHz (any pin which receives a clock)

3.4 SIB

The SIB is the built in RS232 interface module on the 9440. As mentioned earlier, this is the default interface to user equipment if no other external PIM is attached to the 9440.

The SIB circuitry uses the same active break out technique as the NAVTEL DATACHECK 2 unit. The RS-232C interface consists of two female 25 pin D connectors, with 25 SPST switches, 50 stake pins, and 12 pairs of dual red and green LEDs in- between. This section also includes a positive and negative source for mark and space levels and a set of monitor LEDs.

There are 12 separate RS-232C drivers located on the DLC board allowing the 9440 to drive all of the DTE (TD, RTS, DTR, XTC) and DCE (RD, CTS, DSR, CD, TC, RC, RI, SQ) signals to either a mark or space level. There are also 12 receivers for receiving DTE and DCE signals.

The LED circuit is an emitter-follower transistor amplifier with resistors in the collector legs of the circuit to prevent any direct semiconductor path between the power rails.

3.5 CRT MONITOR DESCRIPTION

3.5.1 General Description

A 5 inch solid state raster scan green CRT monitor is the internal display used on the 9440. The CRT is an OEM component from Kristel, model number 65TP-JB1. The unit is designed for high quality display of alphanumerics and graphics.

The monitor requires separate TTL compatible input signals for operation. The separate signals are 1) vertical sync, 2) horizontal sync, and 3) video. The signal amplitude is typically 2.4 volts minimum positive oriented.

3.5.2 Electrical Specification

Synchronization

- Horizontal:

1) 16.66 $\pm$ 0.27 KHz, positive polarity.
2) 4.5 $\pm$ 1 us pulse width

- Vertical: (40 column by 20 row mode)

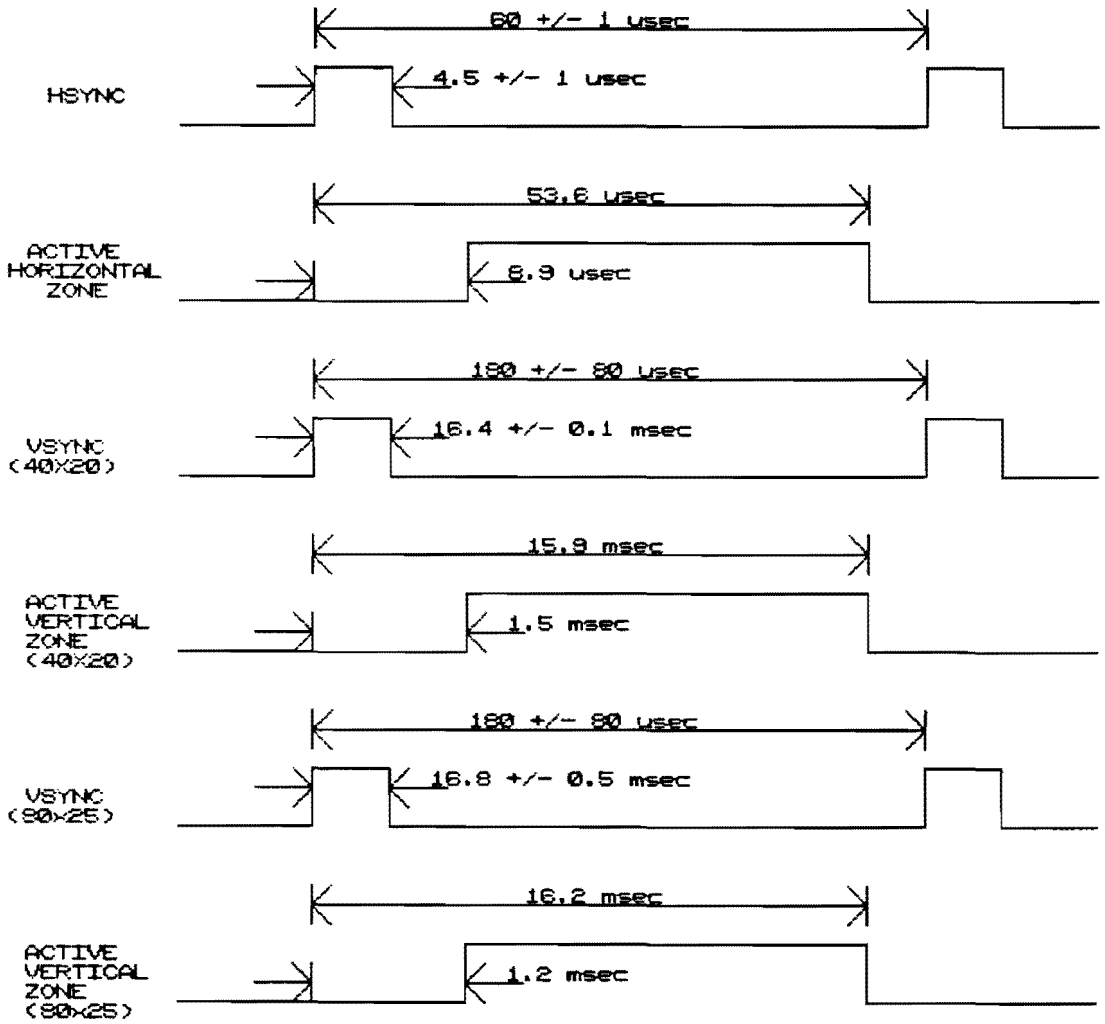
1) 60.9 $\pm$ 0.3 Hz, positive polarity.
2) 180 $\pm$ 80 us pulse width.

(80 by 25 mode)

1) 59.5 $\pm$ 1.7 Hz, positive polarity.
2) 180 $\pm$ 80 us pulse width.

Video	- positive polarity, +5V CMOS level signal.
Blanking Time	- see timing diagram, section 3.5.3.
Viewing Area Size	- 40 by 20 mode:7.0 cm high by 9.4 cm wide. - 80 by 25 mode:7.4 cm high by 9.4 cm wide.
Video Performance	- up to 750 lines centre resolution. - bandwidth up to 25 MHz. - high intensity bit input capability.
Power Input	- +12 VDC $\pm$ 0.2 VDC, 12 watt max.

3.5.3 CRT Timing



3.6 DISK DRIVE DESCRIPTION

3.6.1 General Information

The disk drive used on the 9440 is a SONY 3.5" Micro Floppy Disk Drive. The drive is selected because of the features offered. These include : a low profile, a low power consumption, single power voltage, light weight, ruggedness and high reliability.

3.6.2 Specification

3.6.2.1 Configuration

The drive consists of Read/Write heads, head positioning mechanism, disk motor, interface logic circuit and Read/Write circuit.

3.6.2.2 Physical Dimension

Height : 25.4 mm (1.0 inch).
Width : 101.6 mm (4.0 inches).
Depth : 150.0 mm (5.9 inches).

3.6.2.3 Weight

Weight : 425 g (0.94 pound).

3.6.2.4 Performance

NOTE :

1) The SONY Micro Floppy Disk Drive can operate in either normal density mode or high density mode. In the 9440, the drive is used in the high density mode only. Therefore all performance specification outlined in this section is for the high density mode operation only.

2) The SONY drive detects high density disk through the existence of a hole in the diskette and switch to high density mode operation automatically.

Recording Capacity (unformatted, MFM)

- 2.0 Mbytes/disk, 1.0 Mbytes/surface.

Transfer Rate

- Burst transfer rate : 500 kbits/sec.

Access Time

- Track to track slew rate : 3 msec min.
- Head settling time : 15 msec max.
- Motor start time : 500 msec max.

Functional

- Rotation speed : 300 rpm + 1.5%.
- Recording density : 17434 BPI.
- Track density : 135 TPI.
- Number of cylinders : 80
- Number of Tracks : 160
- Read/write heads : 2

Reliability

- Mean time between failures (MTBF) : 30,000 POH.
- Mean time to repair (MTTR) : 30 minutes.
- Preventive Maintenance (PM) : not required
- Component life : 5 years or 15,000 POH.
- Error rate:
  1) soft read error, less then 1 per 10 bits read.
  2) Hard read error, less than 1 per 10 bits read.
  3) Seek error, less than 1 per 10 seeks.

Input Power Requirements

- Power Consumption :

1)Standby	0.1 W max.
2)Operation (read/write)	1.1 W tpy.

- Supply voltages :

Voltage	Max.Ripple	Current
+5.0V + 10%	0.1Vpp	20 mA max. (standby) 220 mA typ. (read/write) 680 mA max. (motor starts) 890 mA max. (step during motor rotates)

3.6.3 Signal Interface

3.6.3.1 DC Characteristics of Interface Signals

Output signal from drive :

-CMOS open drain driver is used for the output.

output voltage	(VOH)	:	Open
	(VOL)	:	0.4 V max.
	(IOL)	:	48 mA max.

-MPC interface : 1K ohm pull-up resistor are put on each output line from the drive.

Input signal to drive :

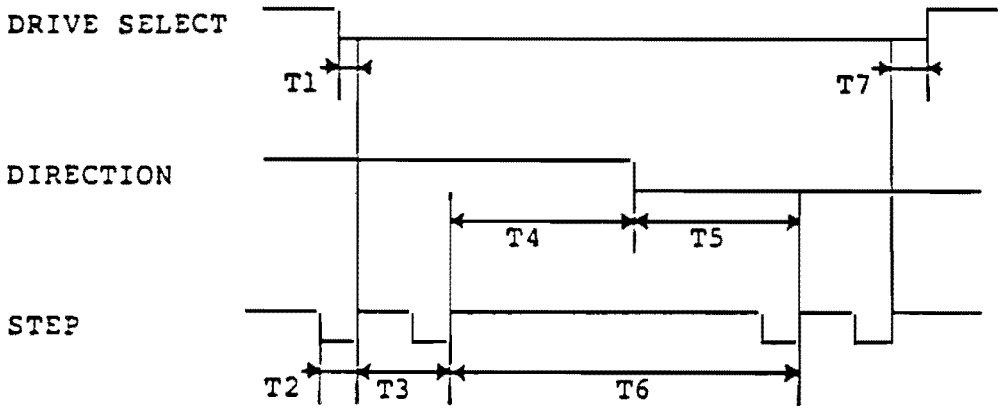
-Input voltage	(VIH) : 2.2 V min. (VIL) : 0.8 V min.
-MPC interface	: 74HCT240 driver IC is used.

3.6.3.2 Interface Signal Definition

See section 3.8.3.

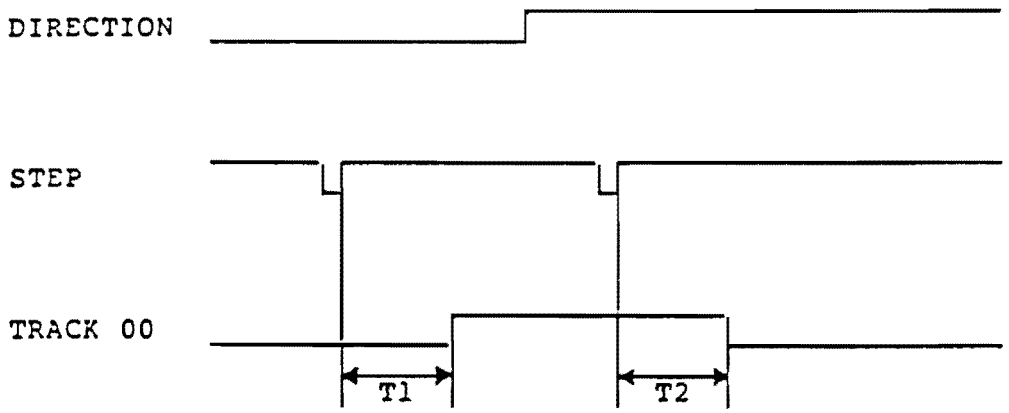
3.6.4 Timing Requirement

3.6.4.1 Head Access



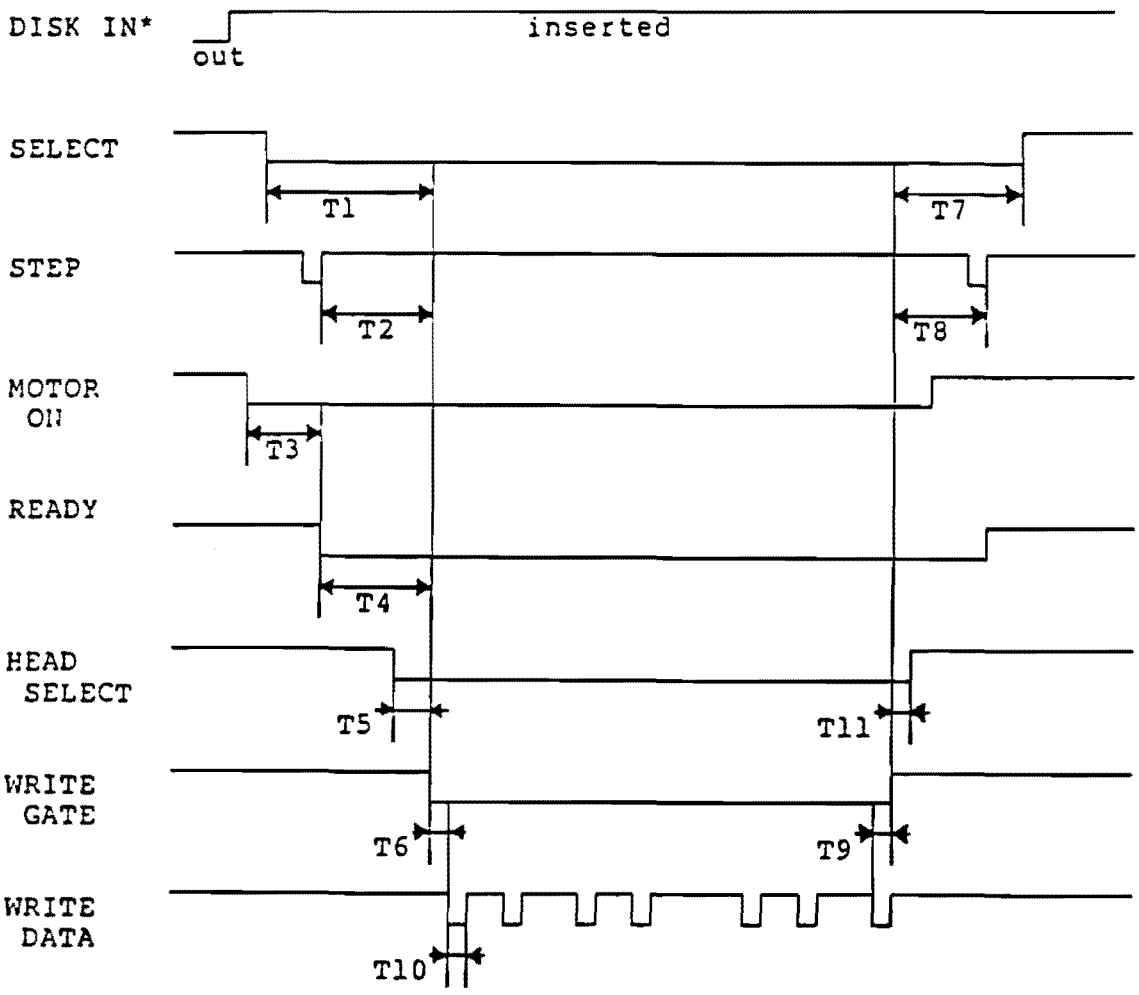
T1	:	0.5 usec min.
T2	:	0.5 usec min.
T3	:	3.0 msec min.
T4	:	0.5 usec min.
T5	:	0.5 usec min.
T6	:	18 msec min.
T7	:	0.5 usec min.

3.6.4.2 Track 00 Signal



T1	:	2.9 msec max.
T2	:	2.9 msec max.

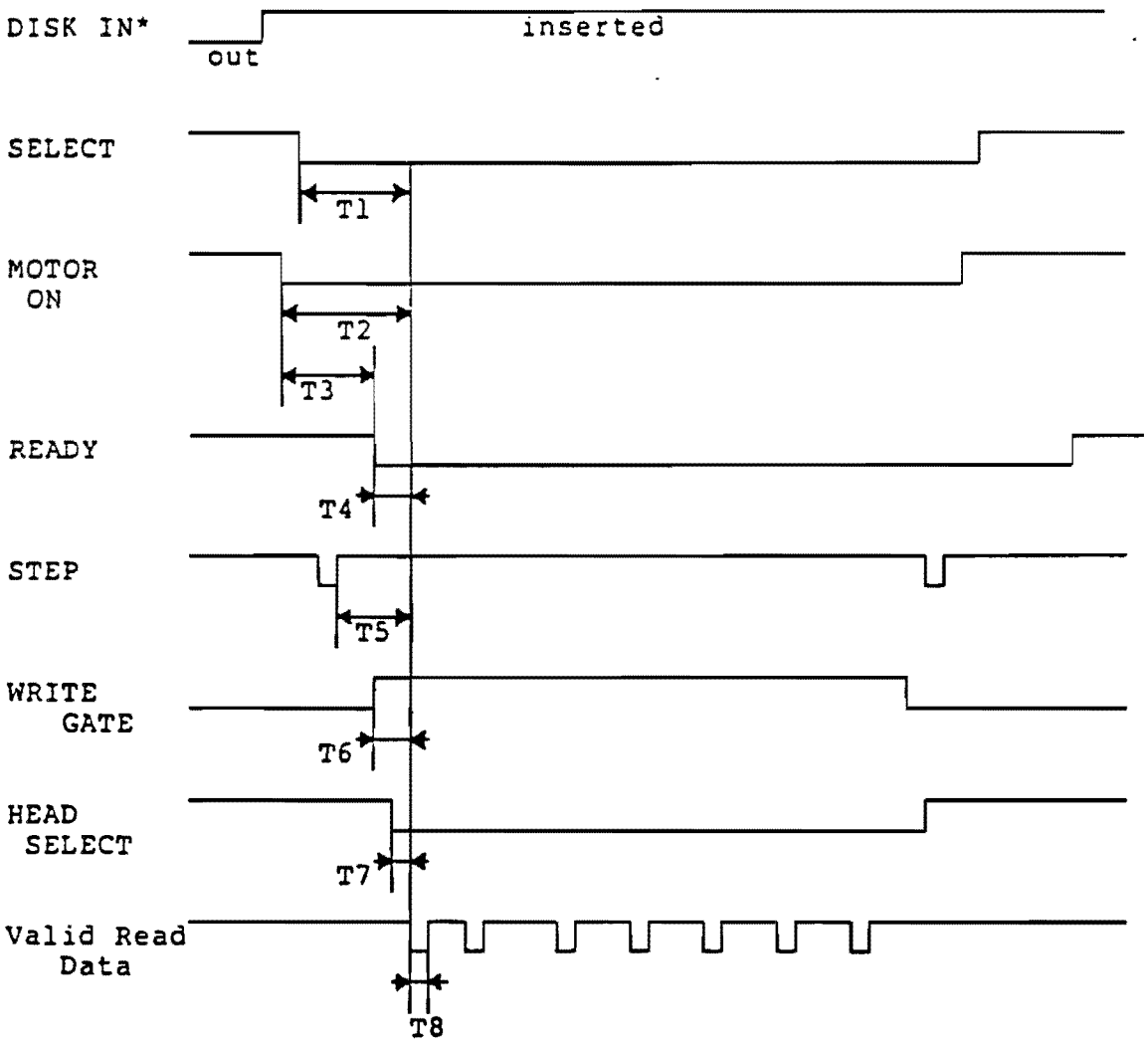
3.6.4.3 Write Data Timing



T1	:	0.5	usec min.	T7	:	0.5	usec min.
T2	:	18	msec min.	T8	:	585	usec min.
T3	:	500	msec max.	T9	:	4.0	usec max.
T4	:	0.5	usec max.	T10	:	150	nsec min., 1000 nsec max.
T5	:	100	usec min.	T11	:	see section 3.8.3	
T6	:	4	usec max.				

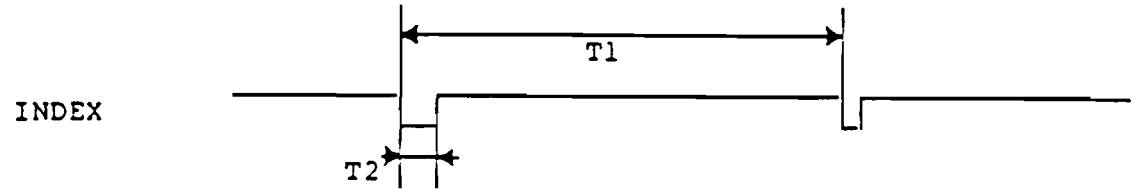
NOTE: The DISK-IN sensor signal inside the drive is high when a disk is inserted in the drive.

3.6.4.4 Read Data Timing



T1	:	0.5	usec min.	T5	:	18	msec max.
T2	:	500	msec min.	T6	:	615 usec max.	
T3	:	500	msec max.	T7	:	100	usec max.
T4	:	0	sec max.	T10	:	350	nsec min., 550 nsec max.

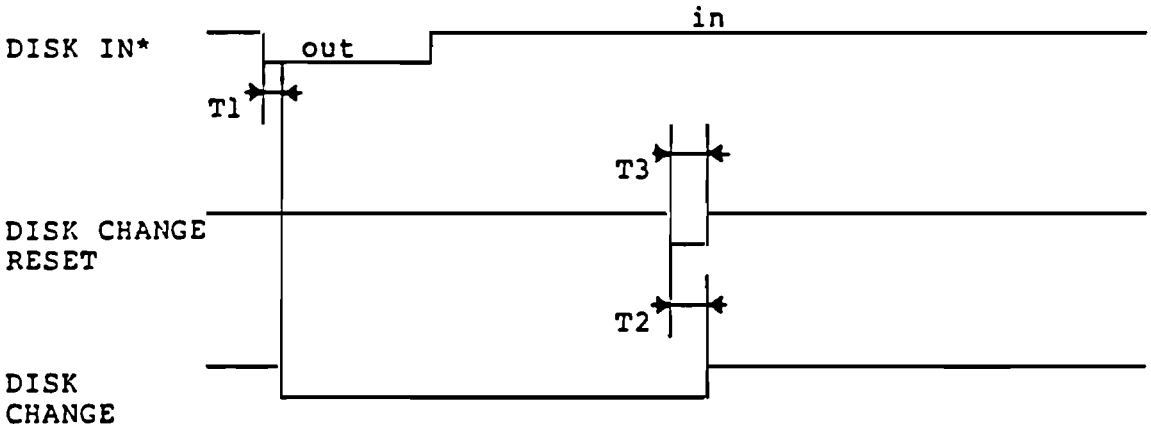
3.6.4.5 Index Pulse



T1* : 198 msec min., 200 msec max.
T2 : 1.5 msec min., 1.7 msec max.

NOTE : * When the disk motor rotation is at the steady state.

3.6.4.6 Disk Change



T1 : 0.5 usec max. T3 : 1.0 usec min.
T2 : 1.0 usec max.

3.7 POWER SUPPLY

3.7.1 General Description

The OEM power supply used in the 9440 is from Computer Products, model number : XL50-7601. It is a universal input 50 watt switching power supply. Universal input voltage eliminates the need for an external 115/220 VAC system switch and cable assembly. Failures due to improper input voltage are eliminated.

The XL50-7601 will maintain regulation down to zero current on all outputs, eliminating the need for preload resistors at light loads. Standard features of this power supply are :

- 85 VAC to 264 VAC continuous input.
- Overvoltage protection.
- Output short circuit protection.
- 16 mSec hold-up time
- CSA/UL/VDE approved.

3.7.2 Output Characteristic

Output Voltage	Output Current Minimum	Max.(1)	Peak(2)	Ripple P-P(3)	Total Regulation (4)
+5.1V(I1)	0A	7.0A	7.0A	50mV	± 2.5%
+12V (I2)	0A	2.5A	5.0A	120mV	± 5%
-12V	0A	0.7A	1.0A	120mV	± 5%

NOTE :

(1) Forced air cooled, 20CFM at 1 atmosphere.

(2) Peak outputs lasting less than 1 minute with duty factor less than 5%. During peak loading the outputs may go outside of total regulation limits.

(3) 50 MHz bandwidth, peak to peak. Measured differentially.

(4) Total Regulation is defined as the static output regulation at 25 degree C. Including initial tolerance, line voltage within stated limits, load current within stated limits, and output voltages adjusted to their factory setting. Also, for stated regulation : I1/I2 < 5.

3.7.3 Electrical Characteristics

Parameter	Condition	Limits
Input Voltage	All rated load conditions	85VAC to 264VAC
Input Frequency		47Hz to 440 Hz Range
Input Surge Current	High line, cold start	20A maximum
Conducted RFI		Meets FCC and VDE limit B
Safety Ground Leakage current	132VAC, 60Hz	0.2 mA maximum
Output Voltage Adjustability	+5V output	+ 3%
Line Regulation	Low line to high line, full load, all outputs	0.3%
Overshoot/ undershoot	Turn-on	None
Transient Response	+5V output, 2.5A to 5 A load change	500mV peak transient settling to within 0.5% in 500us
	+12V output, 1A to 2A load change	300mV peak transient settling to within 0.5% in 500us
Temperature Coefficient	All outputs	+ 0.03% per degree C maximum
Overvoltage Protection Threshold	+5V output	6.25V + 0.75V
Total Output Power	Continuous, 50 degree C ambient	0W to 50W
	Peak	60W
Hold Up Time	50W output power,85VAC input	8mS
	110VAC	16mS
	170VAC	60mS
	220VAC	100mS
Efficiency power	100VAC input, 50W output	65% minimum

3.7.4 Connector Pinout

J1	Pin 1	AC Hot
	Pin 2	AC Neutral
J2,J3,J4	Pin 1	-12VDC
	Pin 2	+12VDC
	Pin 3	Return
	Pin 4	+5VDC

3.8 INTERCONNECT SUMMARY

3.8.1 MPC Backplane SHARE RAM Bus Specification

Pin #	Signal Name	I/O	Functional Description
1...8	SA0 ... SA7	O	Address lines (latched and buffered)
9...16	SA8 ... SA15	O	Address lines (buffered)
17..20	SA17... SA19	O	Address lines (latched and buffered) Comment: All address decode timing calculations (for bus resident devices) must be made with respect to ALE going low (inactive).
21..28	SAD0... SAD7	I/O	Bus data lines (buffered) Comment: AC245 buffer is used. OE' signal for that buffer is supplied by PAL device and is factored by DEN' signal. This eliminates any problem with data setup/hold on 80C188 bus.
29	NSDEN	O	DEN' control line buffered
30	SDTR	O	DTR control line buffered
31	NSSRD	O	RD' control line buffered
32	NSSWR	O	WR' control line buffered
33	SMIO	O	NS2 status signal (low means I/Oo transfer, high means memory transfer; (latched and buffered)
34	SALE	O	ALE control line buffered
35	S2XCLK	O	24 MHz clock signal, buffered, no skew with respect to 80188 X1 clock input.
36	RDYNWT	I	Ready signal from the bus used to insert the wait states during I/O transfers.
37	NSLOCK	O	LOCK signal buffered
38	NSRES	O	Power on reset signal
39	SDRQ1	I	DMA channel 1 DRQ input, buffered
40	SINT1	I	Interrupt input, buffered

Pin #	Signal Name	I/O	Functional Description
41	SINT2	I	Interrupt input, buffered
42	SINT3	I	Interrupt input, connected to EPLD
43	SNPCS4	O	Peripheral CS' line
44	SNPCS5	O	Peripheral CS' line
46,48,50 52,54,56, 58,60	GND	N/A	Ground
49,51, 53,55	+5V	N/A	DC power supply +5V
45,47	+12V	N/A	DC power supply +12V
57,59	-12V	N/A	DC power supply -12V

NOTE : 1) I/O stands for Input/Output in the above table.
2) A signal is define as input or output with respect to the MPC board. For example, SA0 to SA7 are output signals from the MPC board.

3.8.2 Internal CRT Interconnect Specification

Pin #	Signal Name	I/O	Functional Description
1	System ground		Ground Reference
2	Not used		3 Remote Brite Lower end of the remote brightness control pot on the MPC
4	Remote Brite		Center arm of the remote brightness control pot on the MPC
5	Not used		
6	H		Horizontal sync
7	+12V		+12V power input
8	VID		Video
9	V		Vertical Sync
10	System ground		Ground reference

NOTE : All signals are at TTL levels, low is between 0 to 0.8 V and high levels are between 2.4 volts and 5.0 volts.

3.8.3 Disk Drive Interface Bus

Pin #	Signal Name	I/O	Functional Description
1	NDSKCHG RST	O	Disk change reset. If this signal is true (low) while a drive is selected, the NDSKCHG line becomes false (high) when a disk is inserted.
2	NDSKCHG	I	Disk change. This line is true (low) whenever a disk is removed from the drive. The line remains true until both of the following conditions are met: (a) A disk is inserted. (b) NDSKCHG RST signal is low when the drive is selected.
3	GND	N/A	Signal ground.
4	N_IN_USE	O	In use. When this line is low and drive is selected, the IN USE lamp turns on. When this line is high or the drive is not selected, the lamp is off.
5	GND	N/A	Signal ground.
6	NDS3	O	Drive select 0. The select line for drive 3 is used to enable or disable all other interface signals except a NMOTOR line. When the select line is true (low), the drive is enabled and considered active. When the select line is false (high), the disk drive will ignored all inputs from the MPC FDC and all drive outputs are disabled. This line is not used by the MPC board since the 9440 will only support 2 disk drives (drive 0 and drive 1).
7	GND N/A	Signal ground.	

Pin #	Signal Name	I/O	Functional Description
8	NINDEX	I	Index. When the drive is selected, a true (low) pulse is generated on this line by each revolution of the spindle.
9	GND	N/A	Signal ground.
10	NDS0	O	Disk drive select 0. (see NDS3)
11	GND	N/A	Signal ground.
12	NDS1	O	Disk drive select 1. (see NDS3)
13	GND	N/A	Signal ground.
14	NDS2	O	Disk drive select 2. (see NDS 3)
15	GND	N/A	Signal ground.
16	NMOTOR	O	Motor on. When this signal is true (low) and a disk is inserted, the spindle motor starts to run. When this line is made false (high) or a disk is ejected, the spindle motor decelerates and stops. However, if the NMOTOR signal become false (high) during either a write or erase operation, the disk motor does not stop rotating until both the ERASE GATE signal and the NWRGATE signal become false (high).
17	GND	N/A	Signal ground.
18	NDIR	O	Direction. When a drive is selected, a false (high) level on this input causes a NSTEP pulse input to move the Read/Write head away from the disk spindle. A true (low) level causes a NSTEP pulse input to move the Read/Write head toward the drive spindle.
19	GND	N/A	Signal ground.

Pin #	Signal Name	I/O	Functional Description
20	NSTEP	O	Step. When a drive is selected, a true (low) pulse on this line causes the Read/Write head to move to the adjacent track. The direction of the head movement is determined by the status of the NDIR signal at the trailing edge of the pulse. The step operation can be performed even if there is no disk inserted in the drive.
21	GND	N/A	Signal ground.
22	NWRDATA	O	Write data. If the NWRGATE signal is true (low), a true pulse (low) on the NWRDATA line causes a bit to be written on the disk. Pulses on this line is neglected when NWRGATE signal is false (high).
23	GND	N/A	Signal ground.
24	NWRGATE	O	When this line is made true (low) while a drive is selected, the write current circuits are enabled and information may be written under the control of the NWRDATA output.
25	GND	N/A	Signal ground.
26	NTRK00	I	Track 00. This line is true (low) when the drive is selected and the Read/Write head is positioned on track 00.
27	GND	N/A	Signal ground.
28	NWP	I	Write protect. If a write protected disk is inserted while a drive is selected, this line becomes true (low) and the drive will not be able to write data. At all other times, except when the disk is ejected while the drive is selected, this line becomes false (high).
29	GND	N/A	Signal ground.
30	NRDDATA	I	Read data. When the drive is selected, a true (low) pulse is generated on this line every time a bit is detected.

Pin #	Signal Name	I/O	Functional Description
31	GND	N/A	Signal ground.
32	NHDSEL	O	Head select. When the drive is selected, a true (low) level on this input causes Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected. If the NHDSEL signal changes during either a write or erase operation, the head is not changed until both the ERASE GATE and NWRGATE signal become false (high).
33	GND	N/A	Signal ground.
34	NCHG/RDY	I	Ready. This line is true (low) when all of the following conditions are met : (a) The drive is selected. (c) The NMOTOR signal is true (low). (d) The motor rotational speed settles with 300 rpm +/- 10%.

3.8.4 Keyboard Interface

Pin #	Signal Name	I/O	Functional Description
1	SHIFT	I	SHIFT key sense line.
2	CONTROL	I	CONTROL key sense line.
3	LOCK	I	LOCK key sense line.
4	DR0	O	Drive line 0.
5	S0	I	Sense line 0.
6	DR1	O	Drive line 1.
7	S1	I	Sense line 1.
8	DR2	O	Drive line 2.
9	S6	I	Sense line 6.
10	DR3	O	Drive line 3.
11	S5	I	Sense line 5.
12	DR4	O	Drive line 4.
13	S4	I	Sense line 4.
14	DR5	O	Drive line 5.
15	S3	I	Sense line 3.
16	DR6	O	Drive line 6.
17	S2	I	Sense line 2.
18	DR7	O	Drive line 7.
19	S7	I	Sense line 7.
20	DR8	O	Drive line 8.

3.8.5 Transistion PCB Interface

The purpose of the transistion PCB is to take MPC signals from a single 14 conductor ribbon cable and break out the signals to three external connectors. These connectors are for the terminal emulation port(DTE), printer port(DCE) and external CRT monitor port. The signals carried by the ribbon cable are described below:

Pin #	Signal Name	I/O	Functional Description
1	RESET	I	Reset signal to the 80188 CPU.
2	GND	N/A	Signal ground.
3	GND	N/A	Signal ground.
4	SPKR	O	Audio speaker signal.
5	+12V	N/A	+12 V DC supply.
6	RD	I/O	Receive data line to RS232 DTE and DCE connectors.
7	TD	I/O	Transmit data line to RS232 DTE and DCE connectors.
8	CTS	O	For DTE emulation this is the CTS output signal from MPC. For DCE emulation this is the DTR output signal.
9	GND	N/A	Signal ground.
10	GND	N/A	Signal ground.
11	INTENS	O	Intensity signal to external CRT monitor.
12	HSYNC	O	Horizontal sync signal to external CRT.
13	NVSYNC	O	Vertical sync signal to external CRT.

Pin #	Signal Name	I/O	Functional Description
14	VIDEO	O	Video signal to external CRT.

NOTE :

1) Input/Output (I/O) definition is with reference to the MPC board.

2) RD and TD signals could be either input or output depending on which mode (ie. DTE or DCE) that the MPC is emulation.

3) The RTS and DTR signals on the RS232 DTE emulation port are always asserted (ie. resistive pullup to +12V DC, see PCB schematic, drawing # 04-100285B).

4) The DSR and CD signals on the RS232 DCE emulation port are always asserted. Furthermore the CTS signal is looped to RTS.

5) All video signals are TTL levels.

3.8.6 PIM Interface Bus

Pin #	Signal Name	I/O DCE	I/O DTE	Functional Description
1, 2	GND	N/A	N/A	RS-232C signal & system ground.
3	+12V	N/A	N/A	+12V power supply line.
4, 6	+5V	N/A	N/A	+5V power supply line.
5	-12V	N/A	N/A	-12V power supply line.
7	RC	OUT	IN	Receive clock, this signal could be selected as a source to the Pulse Width Measurement (PWM) circuit implemented on the DLC TPIC chip.
8	TC	OUT	IN	Transmit clock, PWM source.
9	XTC	IN	OUT	External clock, PWM source.
10	RD	OUT	IN	Receive data, PWM source.
11	TD	IN	OUT	Transmit data, PWM source.
12	NSQ	OUT	IN	Signal quality, supported via general purpose port on the DLC TPIC chip.
13	NCD	OUT	IN	Carrier detect, this signal is one of the sources for the 80C30 SCC interrupt request on the DLC board.
14	NCTS	OUT	IN	Clear to send, SCC interrupt source.
15	NRTS	IN	OUT	Request to send, SCC interrupt source.
17	NDSR	OUT	IN	Data set ready, supported via TPIC's general purpose port.
18	NDTR	IN	OUT	Data terminal ready, SCC interrupt source.
19	NRI	OUT	IN	Ring indicator, supported via TPIC's general purpose port.
20	SYNC	OUT	OUT	Supported via TPIC's general purpose port.

Pin #	Signal Name	I/O DCE	I/O DTE	Functional Description
21	PID2	IN	IN	PIM ID line 2, supported via TPIC's general purpose port.
22	EVENT	IN	IN	Supported via TPIC's general purpose port.
23	PID1	IN	IN	PIM ID line 1, supported via TPIC's general purpose port.
24	MON	OUT	OUT	Monitor mode, when asserted all of the above signals are set as inputs.
25	PID0	IN	IN	PIM ID line 0, supported via general purpose port.
26	DCENDTE	OUT	OUT	DCE/DTE mode, sets direction of above signals.

NOTE: (1) The signals DCENDTE & MON control the direction of signals on the PIM bus. Assertion of MON sets all signals as inputs. Negation of MON allows DCENDTE to control the direction of signals as indicated under the I/O column in the above table. Lastly the definition of input/output is with respect to the DLC board.

(2) PID 2 to PID 1 are used to identify the type of PIM attached on the PIM bus. The PIM ID signals are defined as follow :

PID2	PID1	PID0	PIM Interface Type
0	0	0	RS232/MIL188
0	0	1	V.11
0	1	0	RS449
0	1	1	V.35
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	No PIM attached.

When no PIM is attached, the SIB will be the defaulted interface to the circuit under test.

3.8.7 SIB Interface Bus

Pin#	Signal Name	I/O	Functional Description
1	RXRTS	I	RTS signal received from a RS232 DCE interface.
2	RXSD	I	DCE transmit data input.
3	RXXTC	I	DCE external clock input.
4	RXDTR	I	DCE data terminal ready input.
5	TXTC	O	Transmit clock output to the RS232 DCE interface.
6	TXRC	O	DCE receive clock output.
7	TXDSR	O	DCE data set ready output.
8	TXCD	O	DCE carrier detect output.
9	TXRD	O	DCE receive data output
10	TXCTS	O	DCE clear to send output.
11	TXSQ	O	DCE signal quality output.
12	TXRI	O	DCE ring indicator output.
13	TXRTS	O	Request to send output to the RS232 DTE interface.
14	TXSD	O	DTE transmit data output.
15	TXXTC	O	DTE external clock output.
16	TXDTR	O	DTE data terminal ready output.
17	RXTC	I	Transmit clock signal input from the RS232 DTE interface.
18	RXRC	I	DTE receive clock input.
19	RXDSR	I	DTE data set ready input.
20	RXCD	I	DTE carrier detect input.
21	RXRD	I	DTE receive data input.
22	RXCTS	I	DTE clear to send input.

Pin #	Signal Name	I/O	Functional Description
23	RXSQ	I	DTE signal quality input.
24	RXRI	I	DTE ring indicator input.
25, 26	NO USED	N/A	
27, 29	+12V	N/A	+12V power supply line.
31, 32	-12V	N/A	-12V power supply line.
28, 30,	GND	N/A	Signal ground.

NOTE : I/O (Input/output) definition for a signal is with respect to the DLC board.

SECTION 4

TEST AND MAINTENANCE PROCEDURE

4.1 SYSTEM TEST PROCEDURE

4.1.1 Introduction

This procedure will describe the system tests used to verify the correct operation of the 9440 unit.

4.1.2 Equipment

The following is a list of equipment required for this test :

- 25 pin "D" type loopback connector
- 26 pin row header loopback connector
- 9440 system disk
- Navtel Datatest 3 unit
- Digital Multimeter

4.1.3 Set Up

a) Plug the power cord into the unit.

b) Insert the 9440 system disk into the disk drive.

c) Turn the 9440 unit on.

4.1.4 Test Procedure

4.1.4.1 Power Supply Test

Use a DVM to check the DC power on the system and verify that they are within the following limits :

+5V	supply	:	+5.00	±	0.25 V
+12V	supply	:	+12.00	±	0.60 V
-12V	supply	:	-12.00	±	0.60 V

4.1.4.2 MPC Serial DTE Port Test

a) Select TERM EMUL from main menu softkey "F4".

b) Connect a wire between pin #6 and pin #20 of the DTE connector.

c) Connect a wire between pin #2 and pin #3 of the DTE connector.

d) Push the RUN key on the keyboard.

e) The screen should display whatever has been typed on the keyboard.

4.1.4.3 MPC Serial DCE Port Test

a) Disconnect all wires from the DTE connector.

b) Select TERM EMUL from main menu softkey "F4".

c) Connect a wire between pin #5 and pin #20 of the DCE connector.

d) Connect a wire between pin #2 and pin #3 of the DCE connector.

e) The screen should display whatever has been typed onthe keyboard.

4.1.4.4 External TTL Video Connector Test

a) Connect an external TTL video monitor to the TTL video connector of the 9440 unit.

b) The monitor should display whatever is on the 9440 screen.

4.1.4.5 Status Indicator Board LED Test

a) Select Cable Test function from the 9440 main menu.

b) Close all switches on the break out box.

c) Select "F1" for testing DCE leads.

d) Push the RUN key on the keyboard.

e) All red LEDs on the bottom row should be on.

f) Push PREV key on the keyboard.

g) Select "F2" for testing DTE leads.

h) Push the RUN key on the keyboard.

i) All red LEDs on the top row should be on.

j) Push the PREV key on the keyboard.

k) Push "F3" for individual lead test.

l) Push the RUN key on the keyboard.

m) Push a softkey for testing individual LEDs.

n) Red LED should be on for the selected leads.

o) Green LED should be on when not selected.

4.1.4.6 Hardware Reset Button Test

a) Push the reset button on the left side of the 9440 unit.

b) The 9440 unit should beep once then reboot.

4.1.4.7 Bert Test

a) Connect the loopback connector to the DCE of the circuit under test connector.

b) Close all switches on the break out box.

c) Select Bert test from main menu "F3".

d) Select DCE EM "F2" from the bert test menu.

e) Push the RUN key.

f) The Bert test should run with no errors.

NOTE : Configuration of the DCE loopback connector is :
pin 2 connected to pin 3
pin 4 connected to 6 and 20

4.1.4.8 PIM Port Test

a) Remove the RS-232 "D" type loopback connector.

b) Plug the PIM loopback connector to the PIM port.

c) Select Bert test from the main menu.

d) Select DCE EM "F2" from the bert test menu.

e) Push the RUN key.

f) The Bert test should run with no errors.

NOTE : Configuration of the PIM port loopback connector is :
pin 1 connected to pins1,13,14,15,18,23,25
pin 10 connected to pin 11

4.1.4.9 Disk Format Test

a) Insert a blank disk into the 9440 unit.

b) Go to the "Disk Util" menu and format a diskette for data capture. Keep the capture buffer size on the diskette to 128 kbytes.

c) Disk should format with no errors.

d) Save the capture disk for the data capture test.

4.1.4.10 Data Capture Test

a) Use a DT3 unit for data capture test for the 9440 unit.Connect the DT3 DCE port to the DTE port of the 9440 unit with a RS-232 cable.

NOTE : Any unit capable of sending data to a RS232 DTE port may be substituted for the DT3.

b) Setup the DT3 for the following:

- BERT test
- internal clock
- 19200 Baud
- Fox Cont
- 7 bits data
- no parity
- DCE

Press run on the DT3 unit.

c) Select "MONITOR" F1 on the main menu of the 9440 unit.

d) Setup the "MONITOR" menu for the following:

SOURCE	: LINE
CAPTR TO	: DISK BUFFER
PROTOCOL	: SYNC
CLOCK	: EXT DCE
SPEED	: 19200
CODE	: ASCII
LEVEL	: 7
PARITY	: NONE

e) Remove the system disk.

f) Insert the Capture disk.

g) Press the "RUN" key for running the Capture program.

h) The 9440 display should show whatever has been transmitted by the DT3 unit.

i) Press "STATS" F1 key to view the Monitor Statistics.

j) Wait until the characters received reaches 128K then press the RUN/HALT key to stop the capture program.

k) Press "PREV" key to go back to the 9440 main menu.

l) Press the "DISK UTIL" F6 key.

m) Use the up and down arrow keys to select file CAPTURE.BFR.

n) Press the "COPY" F1 key.

o) Press the "SCREEN" F4 key.

p) This will display the file Capture.ber on the screen.

q) The screen should display the following:

ADBDCDDDEDFDGD...

Every second character should be a "D".

4.2 DISK DRIVE MAINTENANCE

The SONY drive specification indicates that no preventive maintenance procedure is required for their MP-17W-50L drive. In case of failures, reader should reference SONY disk drive service manual on how to test / repair the disk drive.

One thing that should be pointed out about the SONY manual, it does reference SONY's own internal test jig and setup, so it will be difficult to use their test procedure. However the drive adjustment procedures, schematic and assembly drawing included in that manual is still quite useful.

The best approach to service the disk drive is probably to buy an off the shelf disk drive tester and use it to check out the performance of the SONY drive. Once the problem had been located then reference the SONY manual on how to repair the faulty part.

Keep in mind that when selecting a disk drive tester that there are basically two classes of disk drive tester, analog or digital. Both type requires diagnostic diskettes to work in conjunction with the tester. In general, digital diagnostic testers are much easier to use and require less technical know how.

At NAVTEL Canada, the digital diagnostic approach is selected for verifying drive performance. The manufacturer of the tester is DYSAN, and the digital diagnostic diskette is also available from DYSAN. There are many other disk drive tester manufacturers and the reader should make their own evaluation to see which type is best suited for their operation.

Lastly, current disk drive cost is low enough that replacing the faulty disk drive with a new unit should also be considered as an alternative to repair.

4.3 CRT MONITOR ALIGNMENT PROCEDURE

4.3.1 Reference

Locations of all the adjustment pots are indicated on the component placement drawing for the CRT. A copy of which is included in section 7 of this manual.

4.3.2 CRT Handling Safety Note

All CRT's maintain a voltage charge at the anode, even when inoperative. Therefore, when a CRT is replaced or a monitor is used in kit form, always discharge the picture tube anode to ground using an insulated wire or a screwdriver.

4.3.3 Contrast Check

a) Select "TERM MUL" from main menu.

b) Use the arrow keys to set the following:

- TYPE :VT-100
- INTERFACE :IGNORE
- LCL ECHO :ON

c) Push the run key.

d) Key in a line of "H"s.

e) Adjust the contrast control (R319) of the CRT for the best representation of the displayed characters.

4.3.4 Brightness Check

a) Select high intensity screen for brightness check.

b) Increase brightness control potentiometer (POT1) on the MPC board to maximum, raster lines should be just barely visible.

c) If necessary, increase or decrease the master brightness control (R229) of the CRT until raster lines are just barely visible.

d) The CRT brightness is adjusted at the factory for a brightness of 225 Lux + 10 Lux on a high intensity screen. However CRT intensity is basically a user preference item and may be altered by readjusting the brightness control on the MPC.

4.3.5 Focus Check

CRT focus may be adjusted by turning focus control potentiometer (R206) to obtain best overall focus. Centre may be compromised in order to gain better corner focus.

4.3.6 Horizontal and Vertical Size Check

a) Select any display screen that does not have high intensity portions.

b) If the horizontal size requires readjustment use the coil (L202) to set the width to 9.4 cm.

c) If the vertical size requires readjustment use the height control (R109) to set the height to 7.0 cm. Readjustment of vertical linearity control (R117) may be necessary.

4.3.7 Geometry Check

a) If necessary loosen yoke clamp screw and rotate yoke for straight display.

4.3.8 Vertical Linearity Check

a) Use a vernier calliper to measure the combined height of the top and bottom five rows of characters. The two measurement should not vary by more than 1.8 mm.

b) Use (R117) to adjust the vertical linearity. Readjustment of the vertical size may be necessary.

4.3.9 Horizontal Linearity Check

Use a vernier calliper to measure the combined length of the right-most, left-most and centre five characters of the screen. The three measurement should not vary by more than 1.2mm.

4.4.10 Pincushion and Barrel Check

Use a vernier caliper to measure the overall width of the screen at the top and bottom, the overall deviation must be less than 2mm.

4.5 SYSTEM DISASSEMBLY TIPS

4.5.1 Disassembling A 9440

Refer to NAVTEL drawing number 03-100040B , 9440 FINAL ASSEMBLY sheet 1 for details on how to disassemble a 9440 system.

The easiest way to disassemble a system is as follows :

a) Unscrew four 8-32 x 3/4" flat phillips screws that holds the softbag on to the 9440 case (item # 7 on the final assembly drawing).

b) Stand the 9440 on its keyboard end.

c) Unscrew four 8-32 x 7/16" binding phillips screws. These are located beside the handle release knobs, 2 on each side of the chassis. The screws are item # 6 on the assembly drawing.

d) Unscrew two 8-32 x 7/16" phillips screws. These are located on the bottom of the 9440 units towards the rear of the unit. The screws are item # 6 on the assembly drawing.

Once the 10 screws listed above are removed, then lift the two halves of the case up and they should come apart, lay unit back down. Unscrew 3 6-32 x 3/8" screws that hold rear panel assembly to chassis. All internal subsystems of the 9440 are now accessible.

NOTE : The four 8-32 x 3/4" flat phillips screws used to hold the soft bag to the 9440 case MUST NOT be substituted with other screws. Failure to do so may short out the internal power supply to the chassis.

4.5.2 Removing Printed Circuit Board (PCB)

Refer to NAVTEL drawing number 03-100041B , 9440 UNIT ASSEMBLY sheets 3 and 6 for details on how to remove PCB from a 9440 system.

To gain access to the printed circuit board (PCB), three screws holding the chassis strap (item # 6 on sheet 3 of the drawing) must be removed. Note that the chassis strap is isolated from the metal chassis. When reassembling the chassis strap take care to keep this isolation intact. Failure to do so may result in noise from the CRT induced on to the MPC or DLC PCB's.

4.5.3 Accessing Printed Circuit Board For Troubleshooting

Refer to 9440 System Block Diagram (drawing # 04-100041B) when using the instruction in this section and always turn off the AC power to the system when removing the PCB's.

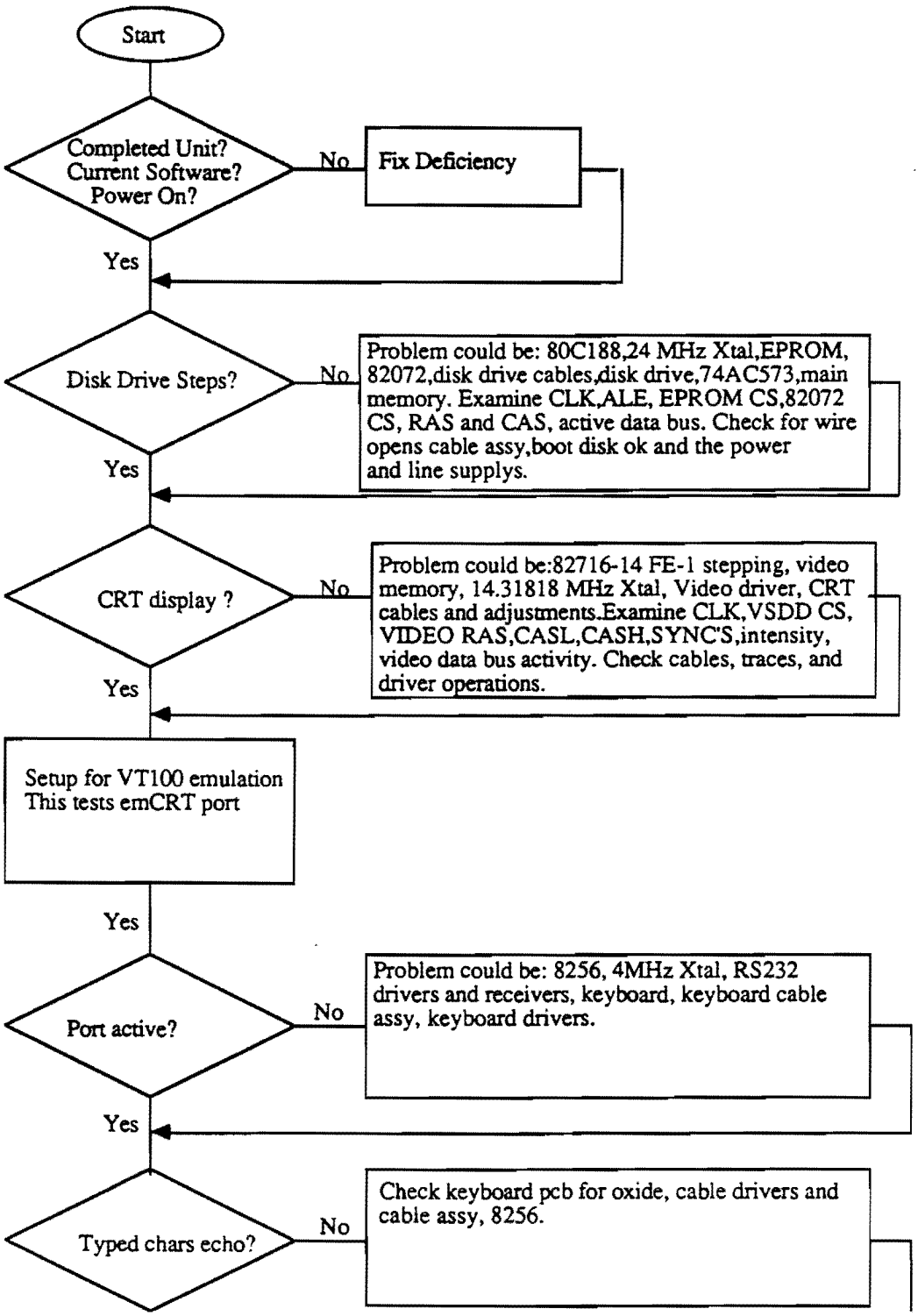
Both the MPC and the DLC boards may remain attached to the 9440 system when troubleshooting both cards. The only exceptions are : the DLC to SIB interface cable (NAVTEL# 59B100283B) and the MPC power supply cable (NAVTEL # 59B100362B). A repair cable kit (NAVTEL # 59100041V1) which includes extension cables for those two cables can be ordered from NAVTEL.

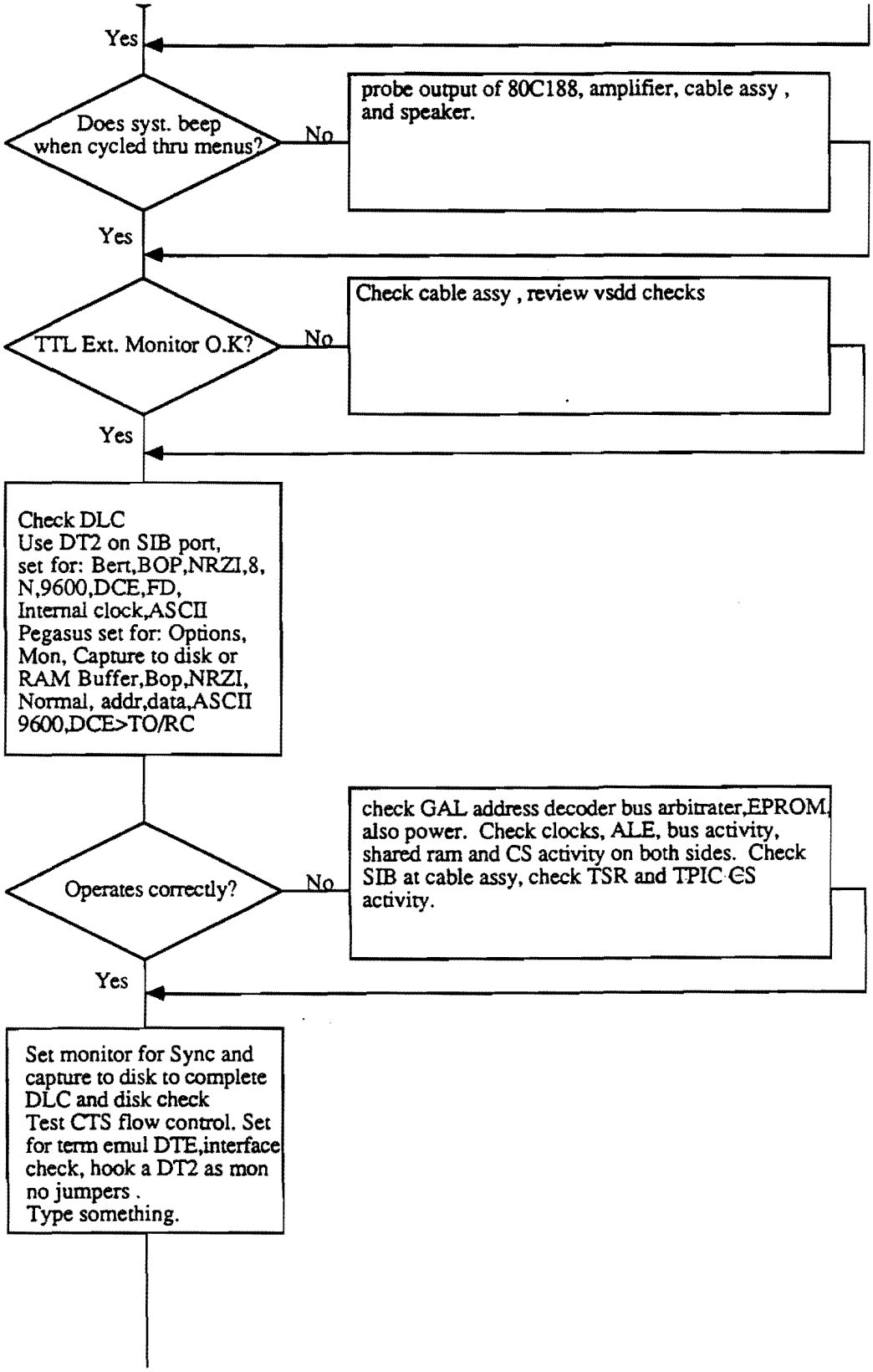
To remove the DLC board, first disconnect the SIB interface cable (part # 59B100283B), the PIM cable (part # 59B100284B), the ground strap (part # 59-100805A) and the disk drive cable to the MPC (part # 59B100366B). Next slide the board out of the chassis card guides and lay the PCB horizontally on the metal chassis. Be sure to put a piece of insulating material between the PCB and the chassis. A piece of antistatic mat would be ideal for this situation. It provides the insulation while reducing the chance of electrostatic discharge damage to the component on the DLC board. Now use a extension cable to connect the DLC to the SIB and re-connect the PIM cable and the ground strap to the DLC and the disk drive cable to the MPC.

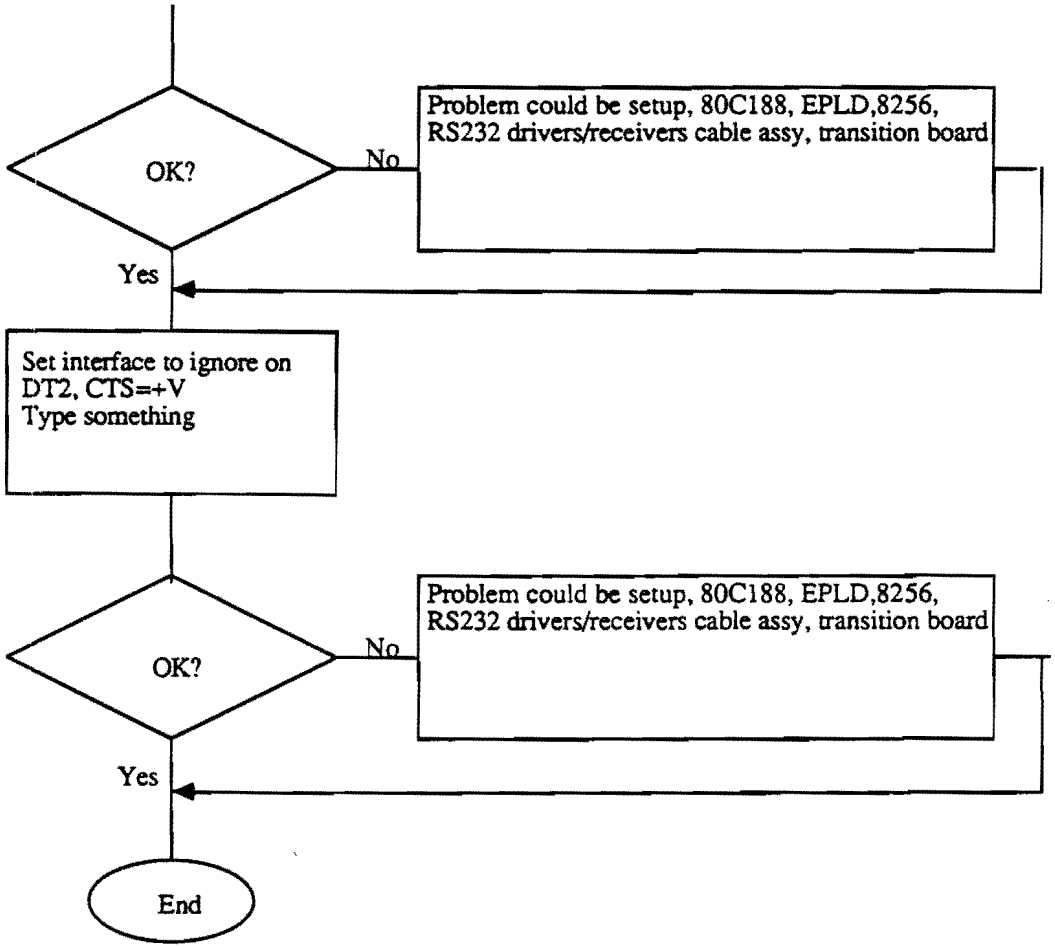
To remove the MPC board, first disconnect the power supply cable (both ends), the ground strap (part #59-100718A) and the keyboard interface cable (part # 59B100363B). Then lift the PCB out of the chassis card guides and lay it on top of the chassis. Again be sure to insulate the PCB against the metal chassis. Re-connect the ground strap and the keyboard cable. Finally use the power cable from the cable kit to re-connect the MPC to the power supply.

SECTION 5

TROUBLE SHOOTING GUIDE




Yes
Does syst. beep when cycled thru menus?
No
probe output of 80C188, amplifier, cable assy , and speaker.
Yes
TTL Ext. Monitor O.K?
No
Check cable assy , review vsdd checks
Yes
Check DLC
Use DT2 on SIB port, set for: Bert,BOP,NRZI,8, N,9600,DCE,FD, Internal clock,ASCII
Pegasus set for: Options, Mon, Capture to disk or RAM Buffer,Bop,NRZI, Normal, addr,data,ASCII 9600,DCE>TO/RC
Operates correctly?
No
check GAL address decoder bus arbitrater,EPROM, also power. Check clocks, ALE, bus activity, shared ram and CS activity on both sides. Check SIB at cable assy, check TSR and TPIC CS activity.
Yes
Set monitor for Sync and capture to disk to complete DLC and disk check
Test CTS flow control. Set for term emul DTE,interface check, hook a DT2 as mon no jumpers .
Type something.


OK?
No
Problem could be setup, 80C188, EPLD,8256, RS232 drivers/receivers cable assy, transition board
Yes
Set interface to ignore on DT2, CTS=+V
Type something
OK?
No
Problem could be setup, 80C188, EPLD,8256, RS232 drivers/receivers cable assy, transition board
Yes
End

SECTION 6

BILL OF MATERIALS

6.1 MAIN PROCESSOR CARD (01-100042A) BILL OF MATERIALS

COMP.NO	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100042A	
78-100472A	LABEL, WHT 1.0" X 0.5", EPROM	PD100693X0
52-100719A	TERMINAL, KWIK DISCONNECT PCB MOUNT	P9
51-100723A	HEADER	P6
51-100722A	HEADER, 1X4 STRAIGHT 0.156" CENTERS	P8
51-100620A	HEADER, 2 X 7 STRAIGHT, SHROUDED AND POLARIZED	P3
51-100619A	HEADER, 2 X 5 STRAIGHT, SHROUDED & POLARIZED	P4
51-100493A	HEADER, RIGHT ANGLE 2X30, 0.1 SPACING	P7
51-100491A	HEADER, RIGHT ANGLE 2X17, 0.1 SPACING	P5
51-100446A	HEADER, RIGHT ANGLE 2X10, 0.1 SPACING	P1
50-100759A	SOCKET, 2X12 DIP	U3
50-100673A	SOCKET, 20 PIN DIP	U40
50-100382A	SOCKET,IC 32 POS.,0.6 SPACE	U16
50-100277A	SOCKET, IC 68-PIN PLCC	U1,U26
33-100026A	CRYSTAL, 24 MHZ PARALLEL	XTAL1
31-100540A	DRAM, 64K X 4, ZIP (20pins)	U27-U30
31-100295A	DRAM, 256K X 4, 100ns DIP	U20-U25
30-100674A	IC, N80C188-12, 8-BIT INTEGRATED MICROPROCESSOR	U1
30-100293A	IC, 8256AH MICROPROCESSOR SUPPORT CONTROLLER	U2
30-100288A	IC, N82716, VIDEO STORAGE & DISPLAY DEVICE	U26
30-044639A	IC P82072 FLOPPY DISK CONTROLLER	U32
29-100677A	IC, P5C032-25, 300 GATE EPLD, 20 pins (.3 DIP)	PD100346X0
29-100676A	IC, P5C060-45, 600 GATE EPLD, 24 pins (.3 DIP)	PD100693X0
29-100672A	IC, 32K X 8 EPROM, 170ns ACCESS, 27C256-1	
29-100671A	IC, 74AC573, OCTAL TRANSPARENT LATCH	U4,U5
29-100670A	IC, 74AC245 OCTAL BIDIRECTIONAL TRANSCEIVER	U34-U38
29-100669A	IC, DELAY LINE, 100ns, 5 TAP	U15
29-100547A	IC, 74HCT244 OCTAL TRI-STATE BUFFER	U39
29-100303A	IC, 74AC74 DUAL D-TYPE FLIP-FLOP	U14
29-100302A	IC, 74AC00 QUAD 2-INPUT NAND GATE	U13
29-100294A	IC, 74AC32 QUAD 2-INPUT POS-OR GATES	U8,U11
29-041978A	IC, 74HCT240 INVERTING LINE DRIVER	U33
19-100730A	RESISTOR NETWORK, 27 10 PIN ISOLATED	RN10,RN11
19-100678A	RESISTOR NETWORK, 4606X-101-102, 5 X 1K BUSSED SIP	RN5
19-100444A	RESISTOR NETWORK, 5 X 100 OHMS SIP (10X1)	RN1-RN4, RN9
01-100693A	EPLD2 ASSY FOR MPC-4 REV A:3	U40
01-100346A	EPLD1 ASSY FOR MPC-4 REV A:4	U3
01-100273A	EPROM ASSEMBLY MPC-4 REV 4.4	U16
10100270V2	PCB, MPC 9440	
072142	INSULATOR PLASTIC #HM221	XTAL1, XTAL2, XTAL4
061253	SOCKET 40 PIN LOW PROFILE	U2,U32
061074	HEADER 3 PIN SINGLE IN LINE #929705/01/3	P2

COMP.NO	COMPONENT DESCRIPTION	REMARKS
051554	CRYSTAL 14.31818 MHZ PARALLEL PKG HC43U/6	XTAL4
051546	CRYSTAL 4.0960 MHZ PAR.	XTAL2
047754	IC MC1488P	U7
041950	IC 74HC14	U12
041949	74HC132 QUAD 2 INPUT NAND SCHMITT	U9
041946	IC 74HC157	U17-U19
041935	IC 74HC138 3 TO 8 LINE DECODER/DEMUX	U6
041934	IC 74HCU04 HEX INVERTER	U10,U31
041932	IC 74HC74 DUAL D TYPE FLIP/ FLOP	U41
033417	2N6715 NPN MED PWR T237 1W 40V 60B@.1A 50M@.05A	Q1
033415	2N6727 PNP MED PWR T237 1W 40V 60B@.1A 50M@.05A	Q2
031914	DIODE IN914 SIL 75MA 75V PWV	D3-D7
031402	DIODE 1N4002A SIL.1A/100V	D1,D2
028479	POT 500K OHMS 1/4W SINGLE TURN 3/8" SQ. SEALED	POT1
024127	RES.NETWORK 4306R/101/103	RN6-RN8
022555	RESISTOR 1/4W 5% 10 MEG OHM	R3
022547	RESISTOR 1/4W 5% 1 OHM	R24
022522	RESISTOR 1/4W 5% 2.2MEG OHM	R8
022510	RESISTOR 1/4W 5% 1MEG OHM	R1,R5
022310	RESISTOR 1/4W 5% 10K OHM	R2,R6,R7,R12,R13,R15
022268	RESISTOR 1/4W 5% 6K8 OHM	R14,R16
022222	RESISTOR 1/4W 5% 2K2 OHM	R9
022210	RESISTOR 1/4W 5% 1K OHM	R4,R26
022020	RESISTOR 1/4W 5% 20 OHM	R10
012207	CAPACITOR NPO 10nF 50V 5%, AXIAL	C16
012204	CAPACITOR NPO 330pF 100V 5%, AXIAL	C13
012196	CAP., 2.2uf TANT., 10%, min 15V, AXIAL	C31,C45
012196	CAP., 2.2uf TANT., 10%, min 15V, AXIAL	C11,C25,C27-C30,C52
012194	CAP., 1.0 uf TANT., +/-10%, min 20V, AXIAL	C8,C9,C44,C46
012193	CAP., 22pf NPO CERAMIC , +/-5%, min. 50V, AXIAL	C1,C2,C39,C40
012192	CAP., 0.1 uf CERAMIC, Z5U, 20%, 50V, AXIAL	C3-C7,C10,C20-C24,C26, C32-C36,C38,C43, C47-C51
012162	CAP., 39PF,NPO,200V,5%	C12,C14
012130	CAP., 100uf,ELECTROLYTIC, AXIAL, +-20%,10V	C18,C19
011206	CAP., 0.1UF 50V WIMA MKS 2/0U1/50V/20%	C15,C17
011205	CAP., 47uf, DIPPED TANT, 16V, 20V, +-10%	C37

6.2 DATA LINK CONTROLLER (01-100043A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100043A	
78-100472A	LABEL, WHT 1.0" X 0.5", EPROM	
58-100597A	WIRE, 30 AWG, GREEN WIRE WRAP	SEE 03-100271B DWG
52-100719A	TERMINAL, KWIK DISCONNECT PCB MOUNT	P5
51-100493A	HEADER, RIGHT ANGLE 2X30, 0.1 SPACING	P2
51-100491A	HEADER, RIGHT ANGLE 2X17, 0.1 SPACING	P4
51-100490A	HEADER, RIGHT ANGLE 2X13, 0.1 SPACING	P1
50-100673A	SOCKET, 20 PIN DIP	U8,U20
50-100277A	SOCKET, IC 68-PIN PLCC	U4,U29
39-100375A	RELAY, DIP HE722A0510	K1-K6
33-100373A	CRYSTAL, 16.128 MHZ	Y2
32-100156A	IC, L4A 0094 TRANSPARENT SYNCHRONOUS RECEIVER	U24,U28
32-100155A	IC, L4A 0093 TEST PORT INTERFACE CONTROLLER	U4
31-100745A	SRAM, 32K X 8 CMOS LP, < = 85ns 0.6" DIP X 28 PINS	U11,U19
30-100269A	CONTROLLER, SERIAL COMMUNICATIONS Z80C30	U18
30-100268A	MICRO PROCESSOR 80188 8 BIT, 68 PIN, NON JEDEC	U29
29-100984A	IC, PEEL 18CV8P-25 20 PINS X 0.3" DIP	PD100345R2
29-100754A	IC, GAL16V8-15LP 20 PINS X.3" DIP	PD100692X1
29-100670A	IC, 74AC245 OCTAL BIDIRECTIONAL TRANSCEIVER	U3,U6,U7
29-100303A	IC, 74AC74 DUAL D-TYPE FLIP-FLOP	U17
29-100302A	IC, 74AC00 QUAD 2-INPUT NAND GATE	U35
25-100798A	TRANSISTOR, 2N3904 NPN TO92 T&R	Q1,Q2
01-100692A	EPLD2 ASSY FOR DLC-4 REV. A:4	U8
01-100345A	EPLD1 ASSY FOR DLC-4 REV B:5	U20
01-100274A	EPROM ASSEMBLY DLC-4 REV 3.2	U10
10100271V3	PCB, DLC 9440	
072142	INSULATOR PLASTIC #HM221	Y1,Y2
061263	SOCKET MACHINE CONTACT 28 PIN OPEN #SM028S6T	U10
061253	SOCKET 40 PIN LOW PROFILE	U18
061252	SOCKET 28 PIN LOW PROFILE	U11,U19
061242	SOCKET 24 PIN LOW PROFILE	U24,U28
061074	HEADER 3 PIN SINGLE IN LINE #929705/01/3	P3
051541	CRYSTAL 3.6864 MHZ PARALLEL RESONENT 50PPM	Y1
047871	IC 27C256/2 200nS	
047754	IC MC1488P	U21,U26,U31,U34
041948	IC 74HC00	U33
041944	IC 74HC125 QUAD TRI STATE NON INVERTING BUFFER	U14
041937	IC 74HC02 QUAD 2 INPUT NOR GATE	U22
041934	IC 74HCU04 HEX INVERTER	U25,U32
041933	IC 74HC32 QUAD 2 INPUT OR GATE	U23,U30
041932	IC 74HC74 DUAL D TYPE FLIP/ FLOP	U27
041930	IC 74HCT573 OCTAL TRI STATE LATCH	U1
041929	IC 74HCT245 OCTAL TRI STATE BUS TRANSCEIVER	U2,U5,U12,U13,U15
041925	IC 74C914	U9,U16

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
031405	DIODE 1N4005A SIL 1A/600V	D1-D8
024139	RES. NETWORK 4310R/102/103	RN5,RN6,RN8
024127	RES.NETWORK 4306R/101/103	RN1,RN9
024123	RES. NETWORK 4310R/102/471	RN2-RN4
024108	RES.NETWORK 4310R/101/103	RN7
022510	RESISTOR 1/4W 5% 1MEG OHM	R3,R4,R11,R14
022247	RESISTOR 1/4W 5% 4K7 OHM	R12,R13 (SOLDER SIDE)
022210	1RESISTOR 1/4W 5% 1K OHM	R10,R8
022147	1RESISTOR 1/4W 5% 470 OHM	R1,R2
022118	1RESISTOR 1/4W 5% 180 OHM	R6,R7,R9
022110	1RESISTOR 1/4W 5% 100 OHM	R5
012197	CAP., 220pf CERAMIC, +/-5%, min 50V, AXIAL(T&R),	C21-C29, C10, C15, C16, C36-C38, C49-C51, C56-C58,C65-C6
012194	CAP., 1.0 uf TANT., +/-10%, min 20V, AXIAL(T&R),	C4, C12, C31, C33-C35, C42, C44, C45, C47, C48, C54, C60, C63, C64, C68
012193	CAP.,22pf NPO CERAMIC ,+/-5%, min. 50V, AXIAL(T&R)	C52,C53,C69,C70
012192	CAP., 0.1 uf CERAMIC, Z5U,20%,50V,AXIAL(TAPE&REEL)	C1, C3, C5-C9, C11, C13, C14, C17-C20, C30, C39-C41, C43, C46, C59, C61, C62, C32
011205	CAP. 47uf, DIPPED TANT, 16V, 20V, +-10%	C2 C32

6.3 KEYBOARD ASSEMBLY (01-100044A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100044A	
10100272V2	PCB, KEYBOARD 9440	
59B100511A	CABLE, KEYBOARD GND STRAP,REV C:6	
59B100363B	CABLE, KEYBOARD CONNECTOR 20 LINES, REV C:3	
81-100183D	PLASTIC, HINGE SOCKET SET 9440	
81-100182C	PLASTIC, INDEX SHAFT 9440, REV D:8	
81-100181D	PLASTIC, KEYBOARD UPPER COVER, REV E:8	
81-100180D	PLASTIC, KEYBOARD LOWER COVER, REV E:8	
80-100818B	INDEX PLATE, 9440, REV A:4	
71-100539A	CABLE TIE, NYLON SELF LOCKING	
69-100825A	DISC SPRING, S-0.551OD, 0.283ID, 0.0197THK	
69-100824A	BALL BEARING, 1/8" DIA, SS18-8	
67-100858A	SCREW, 4-24 X 3/8" TYPE H-L PAN PHILLIPS	
65-100857A	WASHER, FLAT STEEL, ID=1/8", OD=3/8"	
42-100275A	KEYBOARD, CONTACT RUBBER SWITCH	SEE 03-100272B DWG

6.4 STATUS INDICATOR BOARD (01-100045A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100045A	
10100045V2	PCB, 9440 SIB (2PCBS/PANEL)	
52-100799A	JUMPER WIRE, GND.TEST POINT 0.1"	GND
076828	PIN, P.C. GOLD .040 x .300	TP1-TP53
072145	SPACER NYLON .187 x .090 (908-090)	FOR DIP SWITCHES
063114	SWITCH DIP 10 POSITION #11-20	SW2
063112	SWITCH DIP 5 POSITION #21-25	SW3
063111	SWITCH DIP 10 POSITION #1-10	SW1
033408	TRANSISTOR 2N3904 NPN SML SIG T092	Q1-Q25 (ODD)
032228	LED, RED, T&R T1 PACKAGE	LD1-LD25 (ODD)
032233	2LED GREEN TLG123A	LD2-LD26 (EVEN)
033112	TRANSISTOR 2N3906 PNP SML SIG T092	Q2-Q26 (EVEN)
022510	RESISTOR 1/4W 5% 1MEG OHM	R18
022347	RESISTOR 1/4W 5% 47K OHM	R7,R14-R17,R19-R21,R24-R28
022210	RESISTOR 1/4W 5% 1K OHM	R1-R4,R8-R13,R22,R23,R29-R42
022147	RESISTOR 1/4W 5% 470 OHM	R5,R6
011201	CAP. 10uf, DIPPED TANT, 16V,+-10%	C1,C2
011133	CAP 0.1uF 50V CERAMIC Z5U 0.1 LS RADIAL	C3,C4

6.5 TRANSISTION BOARD (01-100285A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100285A	
10100285V2	PCB, TRANSITION 9440 (2PCBS/PANEL)	
54-100416A	CONNECTOR, D25S PCB MOUNT	J1-J2
54-100415A	CONNECTOR, D9S PCB MOUNT	J3
51-100510A	HEADER, 2 X 7 RIGHT ANGLE 0.100 SPACING	P1
44-100470A	PEGASUS SPEAKER, 8OHM, PCB MOUNT	SPKR
41-100729A	SWITCH, PUSH BUTTON TO-5	SW1
072116	INSULATOR FOR TO-5 SWITCHES	FOR PB SWITCH
023285	RESISTOR 5%, 1/2W, 300 OHMS	R1-R4

6.6 9440 UNIT ASSEMBLY (01-100041A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION	REMARKS
	PART NUMBER 01-100041A	
81-100179C	PLASTIC,KEYBOARD CABLE COVER DT4	
81-100177D	PLASTIC FRONT DISPLAY BEZEL DT4 REV D:8	
80-100828A	CRT SHIELD REV A:4	
80-100199C	MOUNTING FRAME FLOPPY DRIVE 9440 REV D:4	
80-100198C	CHASSIS STRAP 9440 REV D:5	
80-100197C	CHASSIS METAL CARD GUIDE 9440 REV E:5	
80-100196E	MAIN CHASSIS 9440 REV F:8	
80-100195D	CHASSIS REAR PANEL REV C:9	
80-100187A	FAN GUARD	
79-100753B	DECAL, LEFT SIDE 9440 REV B:3	
9-100752B	DECAL, RIGHT SIDE 9440 REV A:2	
79-100751A	DECAL, FRONT 9440 REV A:2	
79-100191B	PANEL METAL SIB 9440	
79-100190B	OVERLAY SIB 9440	
71-100539A	CABLE TIE, NYLON SELF LOCKING	
69-100838A	HEX M/F STANDOFF 4.55 X 5/16	
67-100879A	SCREW, TAPPING #8 X 3/4" STEEL ZINC PLATED PAN PHILLIP HEAD	
67-100837A	SCREW, 8-32 X 5/16, SELF TAPPING	
67-100808A	SCREW, 6-32 X 1/4", BINDING/PHILLIPS (STEEL-ZINC PLTD)	
67-100714A	SCREW, 8-32 X 1/2" BINDING PHILLIPS BRIGHT ZINC PLATED STEEL	
67-100713A	SCREW, 3M X 5MM PAN PHILLIPS CLEAR CHROMATE FINISH ZINC PLATED STEEL	
67-100712A	SCREW, 4-40 X 1 1/2" FLAT PHILLIPS BRIGHT ZINC PLATED STEEL	
67-100711A	SCREW, 4-40 X 1/2" BINDING PHILLIPS BRIGHT ZINC PLATED STEEL	
67-100710A	SCREW, 4-40 X 5/16" BINDING PHILLIPS BRIGHT ZINC PLATED STEEL	
66-100804A	NUT, 8-32 SQUARE (1/8" THK)	
65-100717A	LOCKWASHER, #8 INT. TOOTH ZINC PLATED FLAT STEEL	
65-100716A	LOCKWASHER, #6 INTERNAL TOOTH, ZINC PLATED FLAT STEEL	
60-100481A	CONNECTOR, AC, SWITCH UNFUSED SCREW-ON MOUNT	
59-100873A	CABLE, SIB GND. STRAP	
59-100806A	CABLE, DISKDRIVE GND STRAP REV A:2	
59-100805A	CABLE, DLC PCB GND STRAP REV A:2	
59B100282B	CABLE, SIB TO DCE PORT 9440	J13-J23
59B100369B	CABLE,MPC/DLC BUSS	J6-J16 60 LINES
59B100368B	CABLE ASSY, TRANSITION/MPC 9440	
59B100366B	CABLE DISK DRIVE DATA	J9-J20 34 LINES
59B100365B	CABLE,DISK DRIVE POWER	J10-J21 4 LINES
59B100362B	CABLE,DC POWER OUT 9440	J15-J26 4 LINES
59B100361B	CABLE, AC POWER IN 9440	P1-J25 3 LINES
59B100284B	CABLE, PIM PORT 9440	P2-J19
59B100283B	CABLE, DLC / SIB1	J4-J17
59B100281B	CABLE, SIB TO DTE PORT 9440	J5-J18

COMP. NO.	COMPONENT DESCRIPTION
58-100718A	CABLE ASSY, MPC PCB GND STRAP REV B:5
49-100728A	DISK DRIVE, 3.5" MICRO FLOPPY SONY
45-100279A	POWER SUPPLY ASSEMBLY, XL50 - 7601
35-100280A	CRT DISPLAY 5" GREEN
01-100417A	FAN ASSY, 9440 REV A:1
01-100364A	CRT ABLE ASSEMBLY, REV A:2
01-100285A	PCB ASSY 9440 TRANSITION REV. A:3
01-100045A	PCB ASSEMBLY SIB 9440 REV B:7
01-100044A	FINAL ASSEMBLY KEYBOARD REV B:3
01-100043A	PCB FINAL ASSEMBLY DLC-4 REV B:4
01-100042A	PCB FINAL ASSEMBLY MPC-4 REV B:4
076879	HEX STANDOFF 4-40 x 5/16" HEX M/F #4502440AB
076877	SCREW LOCK ASSEMBLY #205818
075117	LOCKWASHER #4 INTERNAL TOOTH, ZINC PLTD FLAT STEEL
075114	WASHER SHOULDER #8 #3236
075105	WASHER #4 LOCK SPRING SPLIT
075104	WASHER #4 FLAT ROUND
074102	NUT 6/32 HEX
074101	NUT 4/40 HEX
073106	SCREW 6/32 X 3/8" PAN PHILLIPS
072104	SLEEVING 3/8"I.D.x1.5"LONG, H.S.

6.7 9440 FINAL ASSEMBLY (01-100040A) BILL OF MATERIALS

COMP. NO.	COMPONENT DESCRIPTION
	PART NUMBER 01-100040A
98-100839A	BAG, PLASTIC 26" W X 36" L X 3 MIL
98-100287B	FOAM END CAPS 9440/60
97-100064A	CARD REGISTRATION WARRANTY
96-100041A	OPERATOR MANUAL ASSY, 9440 REV. A:2
95-100399A	MANUAL, NAVTEL PRODUCT GUIDE
84-100189D	BAG, ACCESSORY 9440 REV
81-100178D	PLASTIC, HANDLE 9440 REV C:6
81-100176E	PLASTIC, CASE HALF 9440
78-100159B	LABEL, 3 1/2 DISKETTE, NAVTEL
78-100118A	LABEL, PACKAGING 2.75 X1.0000
73-100185C	FEET, REAR RUBBER 9440
69-100859A	FOAM SPACER, 3.5 X 3.5 X 1.0000
67-100809A	SCREW, 8-32 X 3/4", FLAT/PHILLIPS, STEEL-ZINC PLTD
67-100715A	SCREW, 8-32 X 7/16 PHILLIPS BLACK OXIDE
65-100716A	LOCKWASHER, #6 INTERNAL TOOTH, ZINC PLATED FLAT
59-100526B	CABLE ASSY, RS232 M/F TO M 5'
49-049002A	DISKETTE 3.5" FLOPPY
01D100290A	DISKETTE ASSY, 9440 SYSTEM DISK REV 3.1
01-100041A	UNIT ASSEMBLY, 9440 REV
107019	UNIT CARTON 9440/60
085502	JUMPER ASSY 2 WAY
085501	JUMPER ASSY 3 WAY
084099	LABEL, SERIAL NUMBER 1.9" x 15/16"
083069	PLUG & CORD #17250
073106	SCREW 6/32 X 3/8" PAN PHILLIPS
072123	TUBING #2 FOR JUMPERS 1

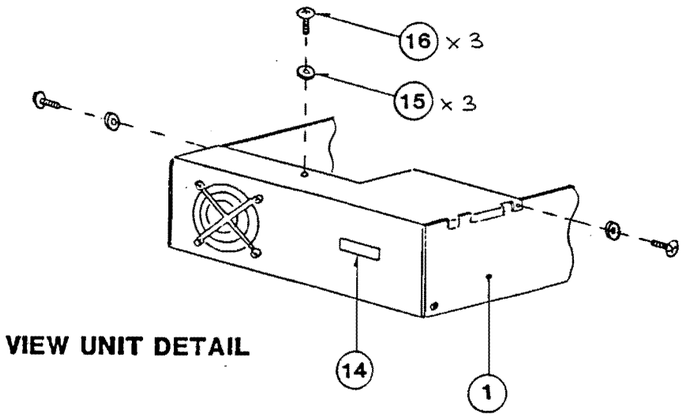
SECTION 7

ASSEMBLY DRAWING AND SCHEMATIC

DRAWING LIST

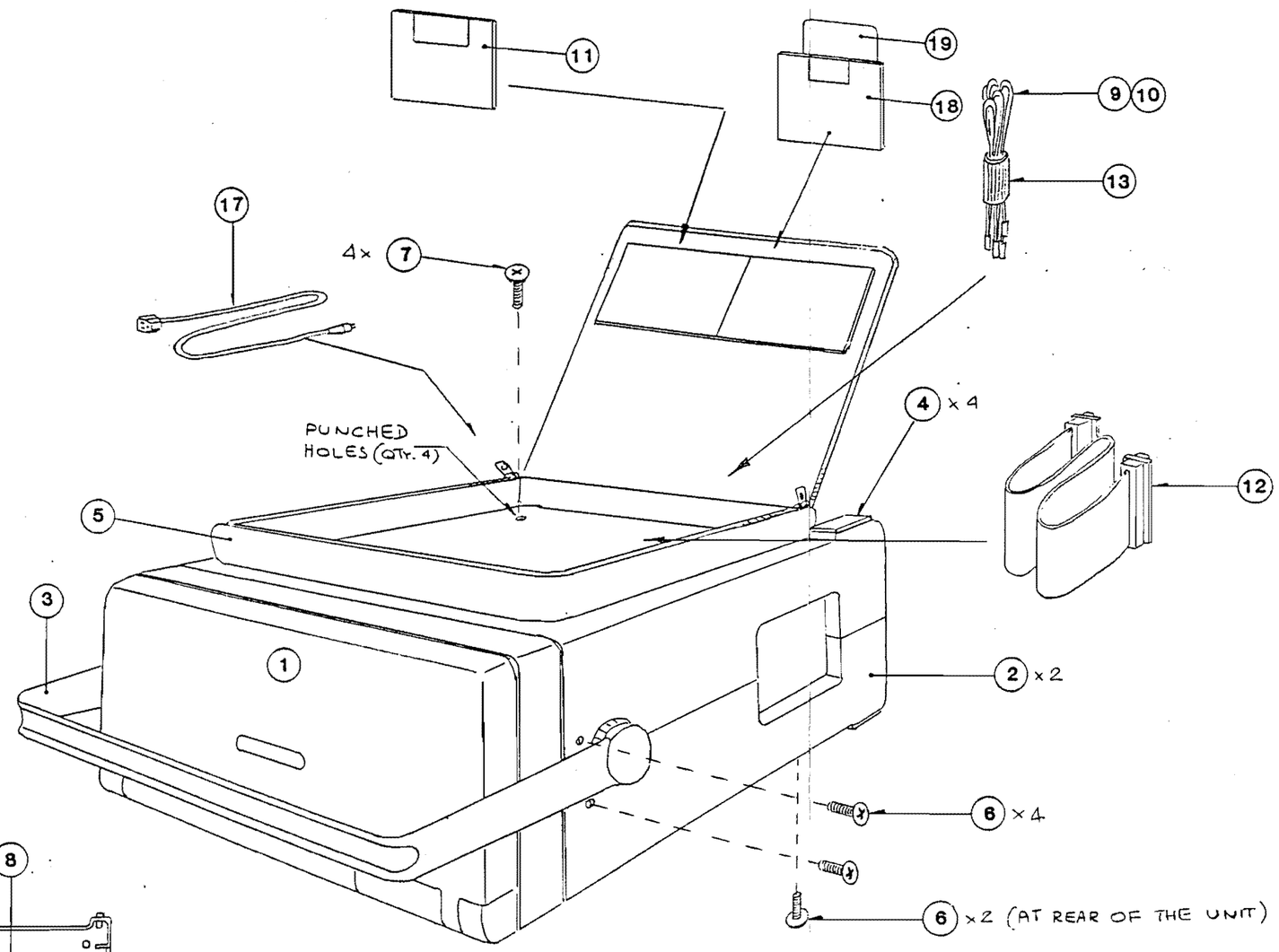
DRAWING NUMBER	DESCRIPTION	REV.	LEV.	NUMBER OF PAGES
03-100040B	9440 FINAL ASSEMBLY	D	3	2
03-100041B	9440 UNIT ASSEMBLY	E	4	6
03-100042B	MPC-4 PCB FINAL ASSEMBLY	B	1	1
03-100043B	DLC-4 PCB FINAL ASSEMBLY	B	1	1
03-100044B	KEYBOARD FINAL ASSEMBLY	C	5	2
03-100045B	SIB PCB ASSEMBLY	B	4	2
03-100270B	MPC PCB ASSEMBLY	C	5	3
03-100271B	DLC PCB ASSEMBLY	D	4	3
03-100271B	DLC PCB ASSEMBLY	E	7	2
03-100272B	KEYBOARD PCB ASSEMBLY	B	1	1
03-100285B	9440 TRANSISTION PCB ASSEMBLY	A	1	1
03-100417B	FAN ASSEMBLY	A	3	1
04-100041B	SYSTEM BLOCK DIAGRAM	D	9	1
04-100045C	9440 STATUS INDICATOR BOARD	B	2	1
04-100270B	9440 MPC	C	3	5
04-100271B	9440 DLC	E	5	5
04-100272D	9440 KEYBOARD SCHEMATIC	A	2	1
04-100285B	9440 TRANSISTION BOARD	A	1	1
35-100280A	5" CRT COMPONENT LEGEND	-	5	1

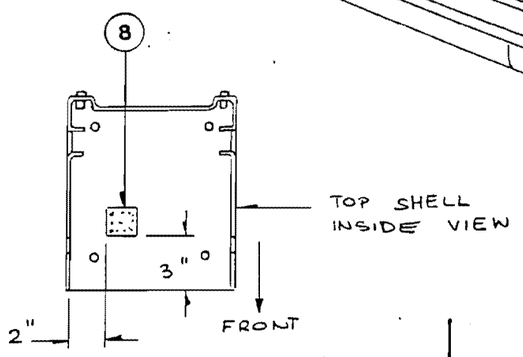
NOTE: Two versions of DLC assembly drawing are included. The earlier version is for older revision DLC PCB which required trace cuts and wire adds. However electrically, the two versions of DLC board are identical.



REAR VIEW UNIT DETAIL

ITEM	DESCRIPTION	PART #	QTY.
19	LABEL FOR 3.5" DISKETTE	78-100159B	1
18	DISKETTE 3.5", BLANK	49-049002A	1
17	PLUG AND CORD	083069	1
16	SCREW 6-32 x 3/8" BINDING PHILLIPS	073106	3
15	WASHER # 6 INTERNAL TOOTH	65-100716A	3
14	LABEL, SERIAL NUMBER	084099	1
13	TUBING # 2 FOR JUMPERS	072123	1
12	CABLE RS-232 M/F TO M	59-100526B	1
11	SYSTEM DISK 9440	01D100290A	1
10	JUMPER 2 WAY	085502	4
9	JUMPER 3 WAY	085501	2
8	FOAM SPACER	69-100859A	1
7	SCREW 8-32 x 3/4" FLAT PHILLIPS	67-100805A	4
6	SCREW 8-32 x 7/16" BINDING PHILLIPS	67-100715A	6
5	SOFT BAG	84-100189D	1
4	FEET, REAR RUBBER	73-100185C	4
3	HANDLE	81-100178D	1
2	HALF CASE	81-100176E	2
1	UNIT ASSEMBLY	01-100041A	1





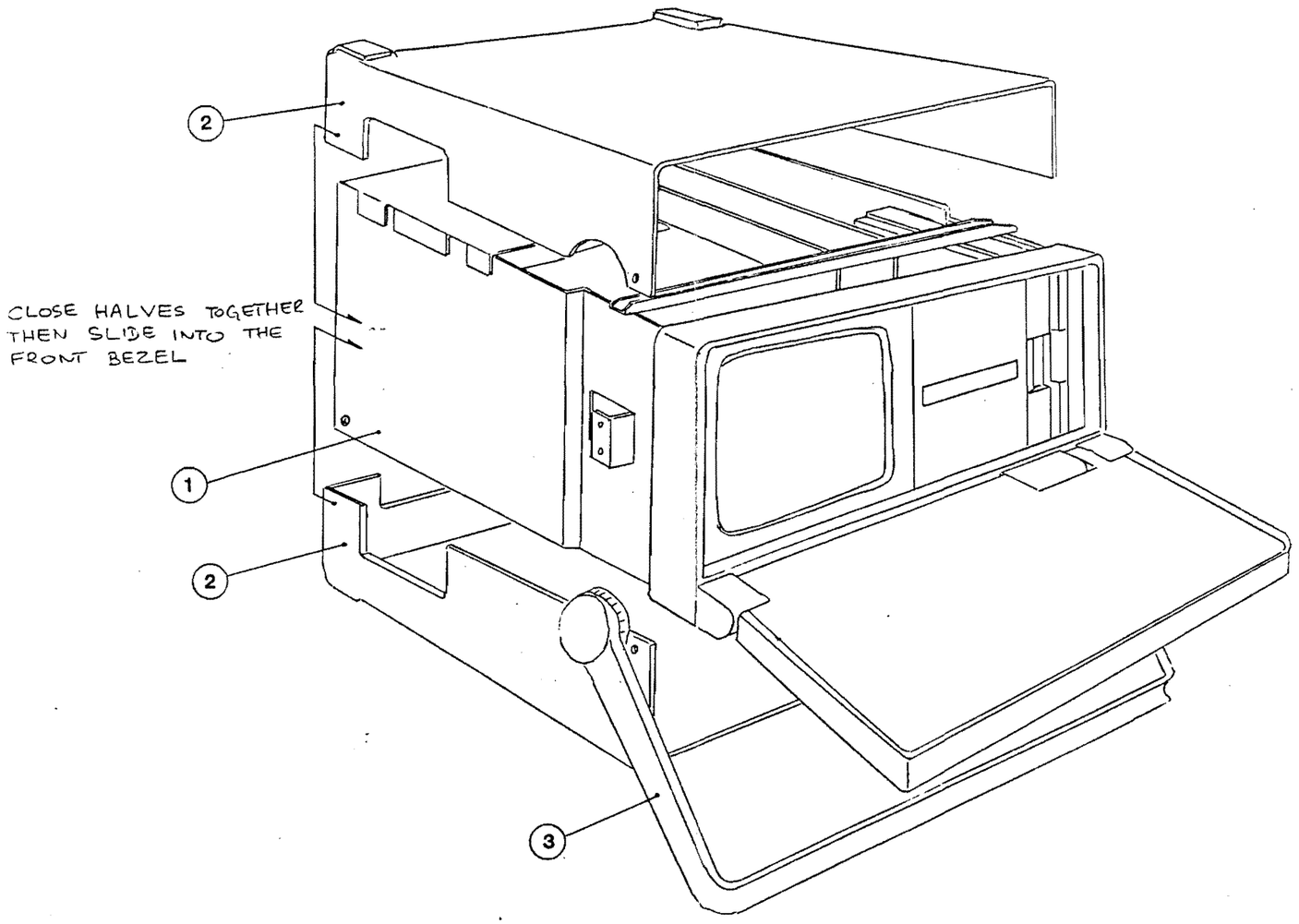
FOAM SPACER DETAIL

(RW) ECO 1324	D	3
(RW) ECO 1248	C	2
ECO 1228	B	1
change	rev	lss

title: **9440 FINAL ASSEMBLY**

Navtel

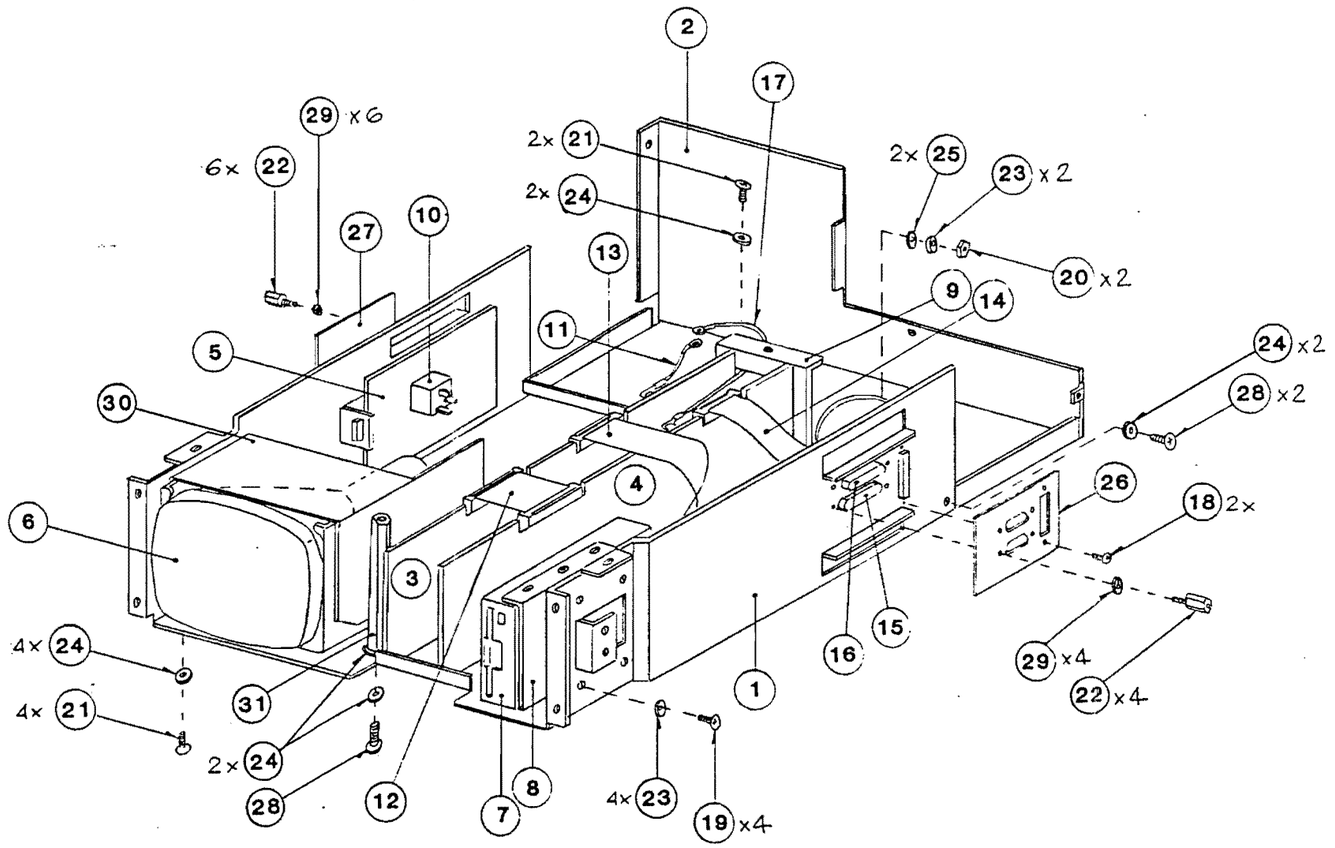
scale: NA	dwn: CP 13 NOV 88	appvd: M. Wong 14 Nov-88
prod: 9440	chkd: (RW) 14.11.88	p.eng:
proj: F001	dwg: 03-100040B	
sht 1 of 2	rev: D	lss: 3



ITEM	DESCRIPTION	PART #	QTY.
3	HANDLE	81-100178D	1
2	HALF CASE	81-100176E	2
1	UNIT ASSEMBLY	01-100041A	1

change	rev	lss	title: 9440 FINAL ASSEMBLY -EXPLODED VIEW	scale: NA	dwn: CP 11 DEC 88	oppvd:
ECO 1324	D	3		prod: 9440	chkd:	p.eng:
ECO 1248	C	2	Navtel	proj: F001	dwg: 03-100040B	
				sht 2 of 2	rev: D	lss: 3

ITEM	DESCRIPTION	PART #	QTY.
31	STANDOFF HEX 6-32 x 4.5"	69-100838 A	1
30	CRT SHIELD	80-100828 B	1
29	WASHER # 4 LOCK SPRING SPLIT	075105	10
22	SCREW 6-32 x 3/8" PAN PHILLIPS	073106	3
27	DECAL, LEFT SIDE	79-100753B	1
26	DECAL, RIGHT SIDE	79-100752B	1
25	WASHER # 4 FLAT ROUND	075104	2
24	WASHER #6 INTERNAL TOOTH	65-100716A	10
23	WASHER # 4 INTERNAL TOOTH	075117	6
22	SCREW LOCK ASSEMBLY	076877	10
21	SCREW 6-32 x 1/4" BINDING PH.	67-100808A	6
20	NUT 4-40 HEX	074101	2
19	SCREW 4-40 x 5/16" BINDING PH.	67-100710A	4
18	SCREW 4-40 x 1/2" BINDING PH.	67-100711A	2
17	GROUND STRAP PCB, DLC	59-100805A	1
16	CABLE, SIB TO DCE PORT	59-100282B	1
15	CABLE, SIB TO DTE PORT	59B100281B	1
14	CABLE, PIN PORT	59B100284B	1
13	CABLE, DISK DRIVE DATA	59B100366B	1
12	CABLE, MPC/DLC BUSS	59B100369B	1
11	GND STRAP PCB, MPC	58-100718A	1
10	CONNECTOR, AC SWITCH	60-100481A	1
9	CHASSIS METAL CARD GUIDE	80-100197C	1
8	MOUNTING FRAME FLOPPY	80-100199C	1
7	DISK DRIVE, 3.5" FLOPPY	49-100728A	1
6	CRT DISPLAY, 5" GREEN	35-100280A	1
5	TRANSITION PCB	01-100285A	1
4	DLC PCB	01-100043A	1
3	MPC PCB	01-100042A	1
2	CHASSIS REAR PANEL	80-100195D	1
1	MAIN CHASSIS	80-100196E	1



NOTE:

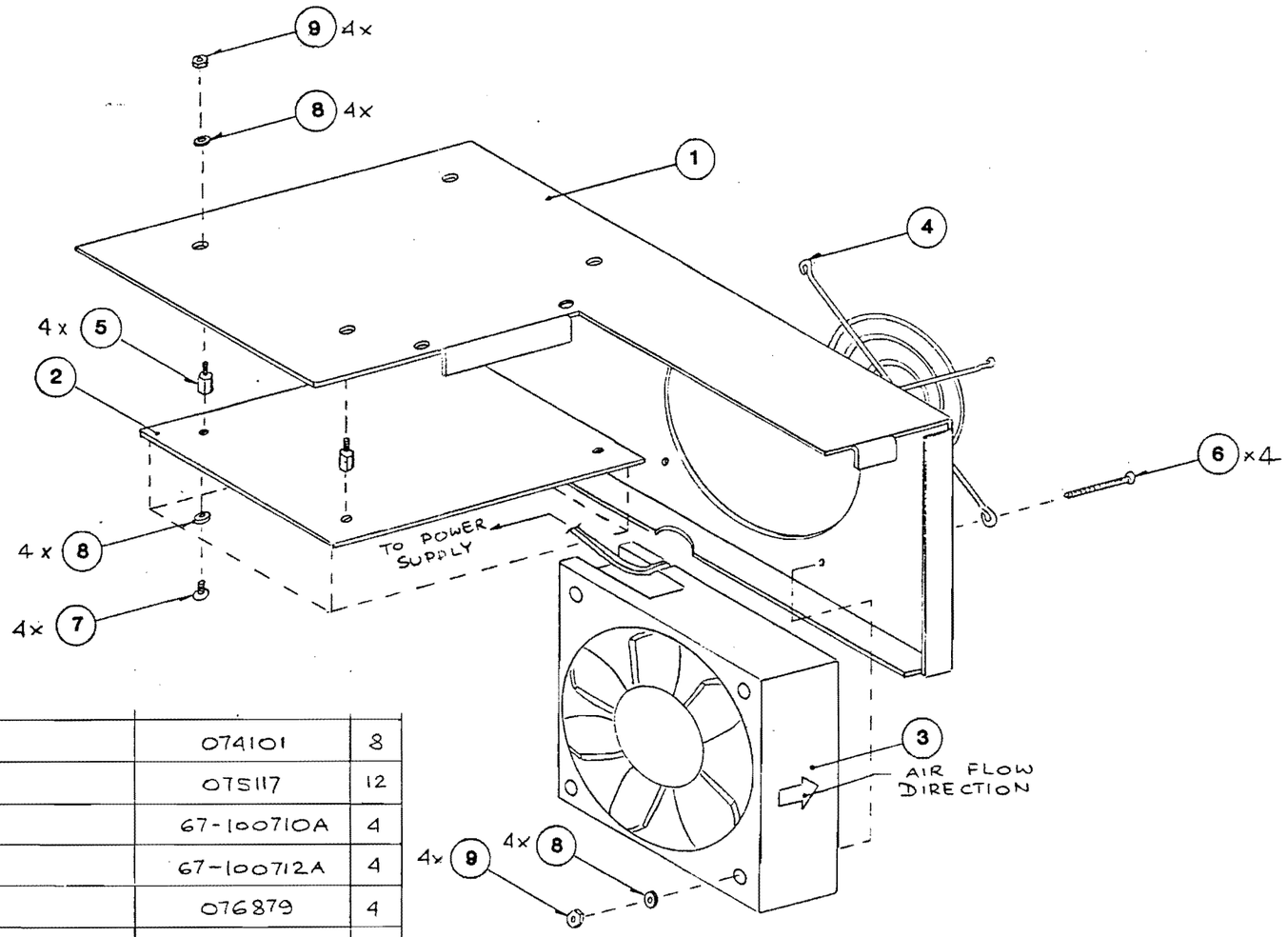
1. FOR CONNECTIONS AND CABLES DRESSING SEE SH 5 OF 6
2. FOR DISK DRIVE INSTALLATION DETAIL AND CHASSIS STRAP MOUNTING DETAIL SEE SH 3 OF 6
3. FOR REAR PANEL ASSEMBLY DETAIL SEE SH 2 OF 6
4. FOR FRONT BEZEL ASSEMBLY DETAIL SEE SH 4 OF 6
5. FOR CRT SHIELD DETAIL SEE SH 3 OF 6

change	rev	lss
ECO 1298	E	4
ECO 1298	D	3
ECO 1248	C	2
ECO 1216	B	1

title: **UNIT ASSEMBLY**

Navtel

scale: NA	dwn: CP 8 NOV 88	oppvd:	
prod: 9440	chkd: 10.4.88	p. eng:	
proj: F001	dwg: 03-100041B		
sht 1 of 6	rev: E	lss: 4	



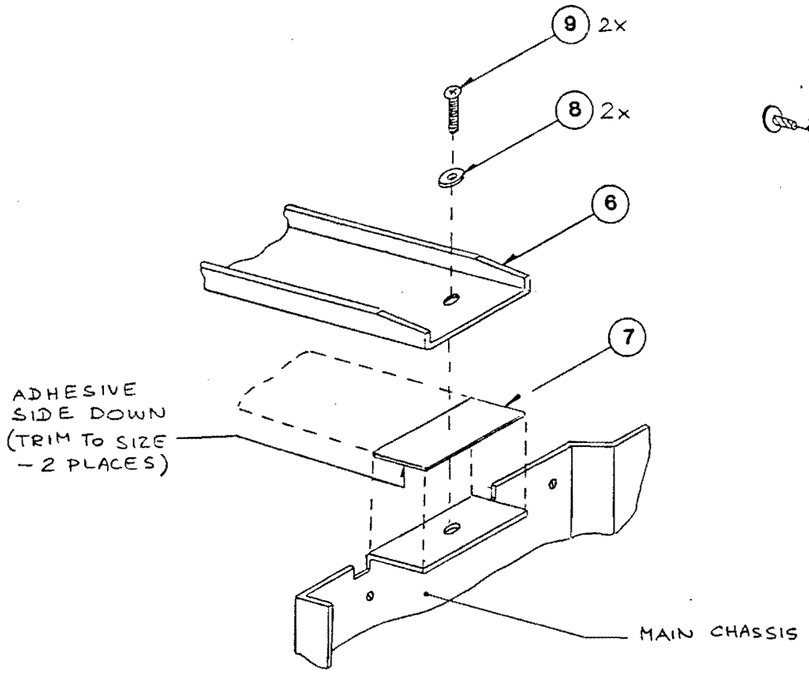
ITEM	DESCRIPTION	PART #	QTY.
9	NUT 4-40 HEX	074101	8
8	WASHER # 4 INTERNAL TOOTH	075117	12
7	SCREW 4-40 x 5/16" BINDING PHILLIPS	67-100710A	4
6	SCREW 4-40 x 1 1/2" FLAT PHILLIPS	67-100712A	4
5	HEX STANDOFF 4-40 x 5/16" M/F	076879	4
4	FAN GUARD	80-100187A	1
3	FAN ASSEMBLY, 9440	01-100417A	1
2	POWER SUPPLY ASSEMBLY	45-100279A	1
1	CHASSIS REAR PANEL	80-100195A	1

change	rev	lss
ECO 1298	E	4
ECO 1298	D	3
ECO 1248	C	2
ECO 1216	B	1

title:
UNIT ASSEMBLY
-REAR PANEL DETAIL

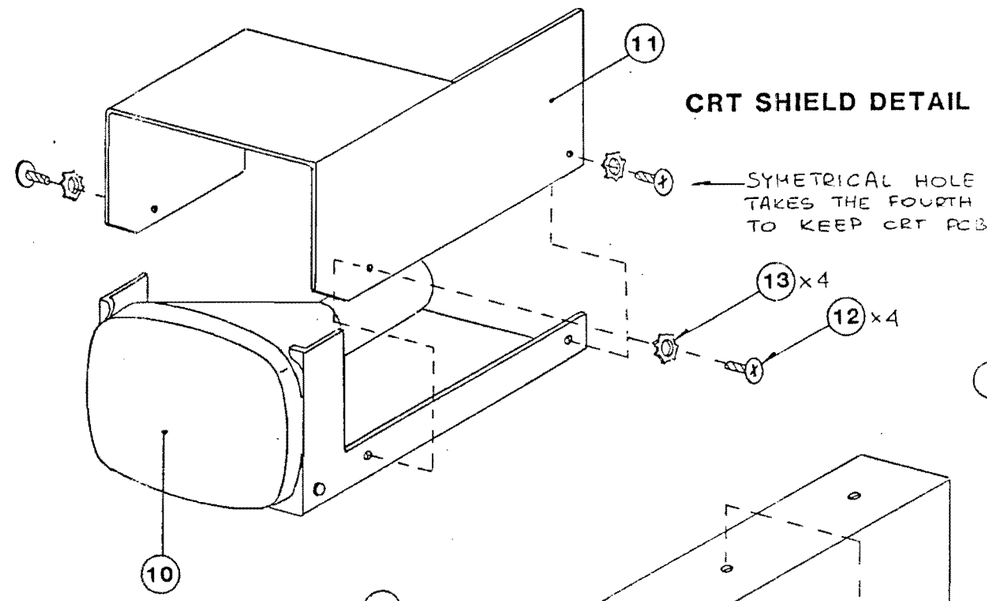
Navtel

scale: NA	dwn: CP 8 NOV 88	appvd: M. Wong 10 Nov 88	
prod: 9440	chkd: 10-11-88	R. eng:	
proj: F001	dwg: 03-100041B		
sht 2 of 6	rev: E	lss: 4	



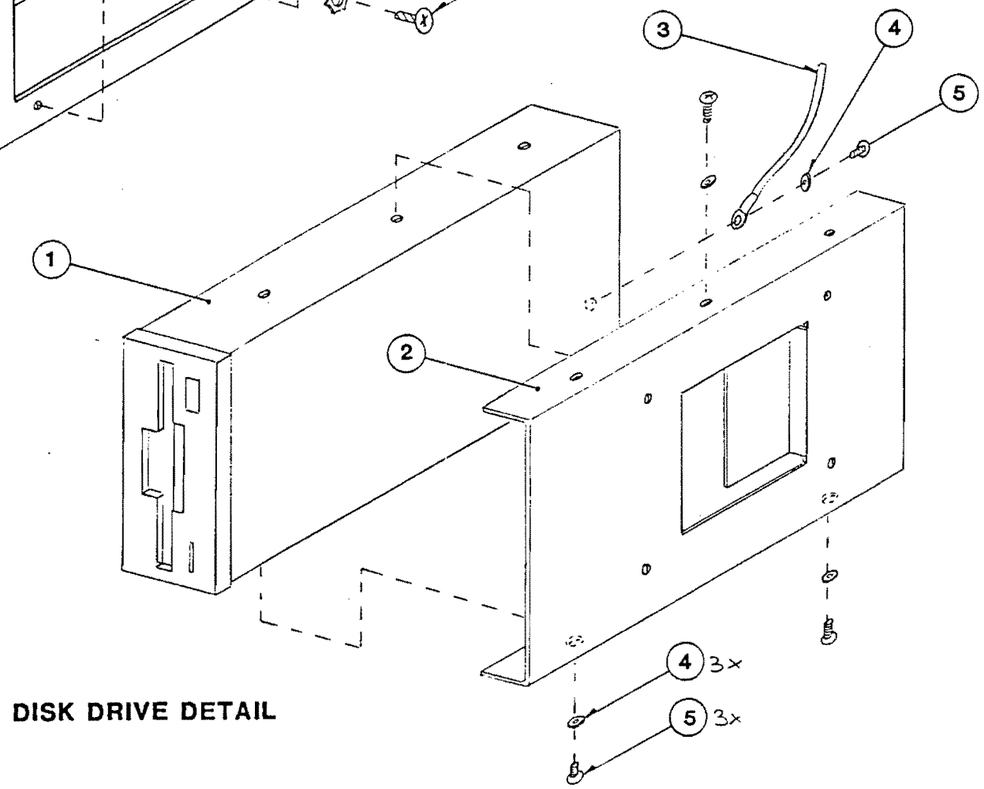
CHASSIS STRAP MOUNTING DETAIL (BOTH SIDES)

ITEM	DESCRIPTION	PART #	QTY.
13	STAR WASHER # 8	65-100717A	4
12	SCREW # 8 x 5/16" SELF TAPPING	67-100837A	4
11	CRT SHIELD	80-100828B	1
10	CRT DISPLAY, 5" GREEN	35-100280A	1
9	SCREW 8-32 x 1/2" BINDING, PHILLIPS	67-100714A	2
8	SHOULDER WASHER # 8	075114	2
7	ELECTRICAL TAPE, 1" WIDE, BLACK	93-100840A	AR
6	CHASSIS STRAP	80-100198C	1
5	SCREW, 3M x 5mm PAN PHILLIPS	67-100713A	4
4	WASHER # 4 INTERNAL TOOTH	075117	4
3	DISK DRIVE GND LEAD	59-100806A	1
2	MOUNTING FRAME FLOPPY DRIVE	80-100199C	1
1	DISK DRIVE, FLOPPY	49-100728A	1



CRT SHIELD DETAIL

SYMETRICAL HOLE OF THE CRT FRAME TAKES THE FOURTH SCREW AN WASHER TO KEEP CRT PCB DOWN

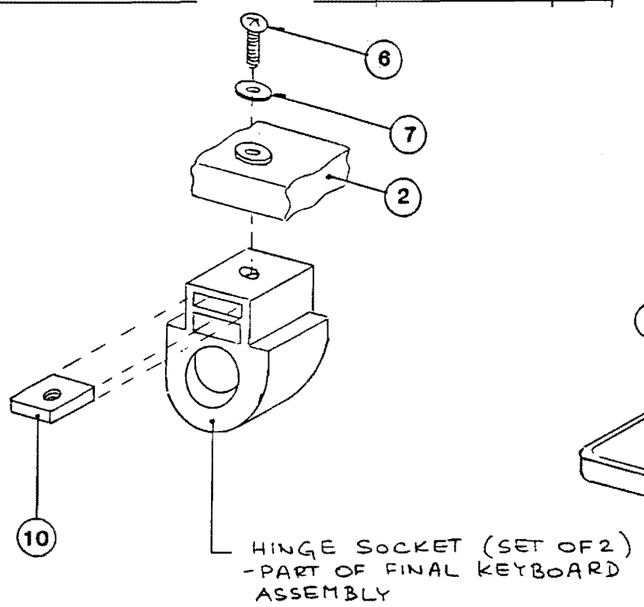


DISK DRIVE DETAIL

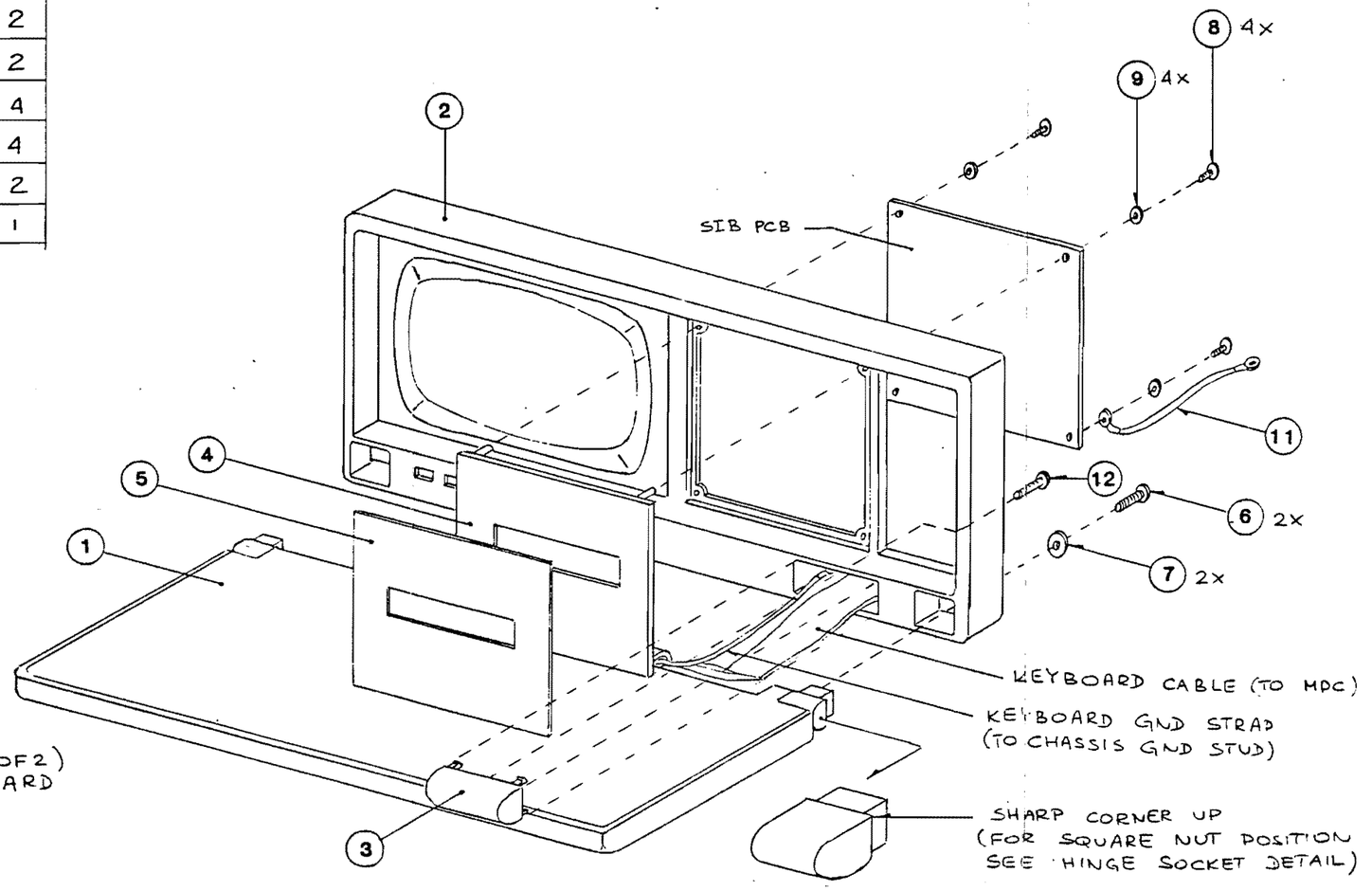
	ECO 1298	E	4	title: UNIT ASSEMBLY -DISK DRIVE, CRT AND CHASSIS STRAP DETAIL	scale: NA	dwn: CP 8 NOV 88	appvd: M.Woug 10 Nov 88
	ECO 1298	D	3		prod: 9440	chkd: RSW 10-11-88	p.eng:
	ECO 1248	C	2		proj: F001	dwg: 03-100041B	
	ECO 1216	B	1	Navtel	sht 3 of 6	rev: E	lss: 4
	change	rev	lss				

ITEM	DESCRIPTION	PART #	QTY.
1	FINAL KEYBOARD ASSEMBLY	01-100044A	1
2	FRONT DISPLAY BEZEL	81-100177D	1
3	KEYBOARD CABLE COVER	81-100179C	1
4	METAL PANEL SIB	79-100191B	1
5	OVERLAY SIB	79-100190B	1
6	SCREW 8-32x1/2" BINDING PH.	67-100714A	2
7	LOCKWASHER #8 INTERNAL TOOTH	65-100717A	2
8	SCREW 4-40x5/16" BINDING PH.	67-100710A	4
9	WASHER # 4 INTERNAL TOOTH	075117	4
10	NUT 8-32 SQUARE	66-100804A	2
11	SIB GND LEAD	59-100873A	1

ITEM	DESCRIPTION	PART #	QTY.
12	SCREW, TAPPING #8 x 3/4" PAN, PHILLIPS	67-100879A	1



HINGE SOCKET DETAIL



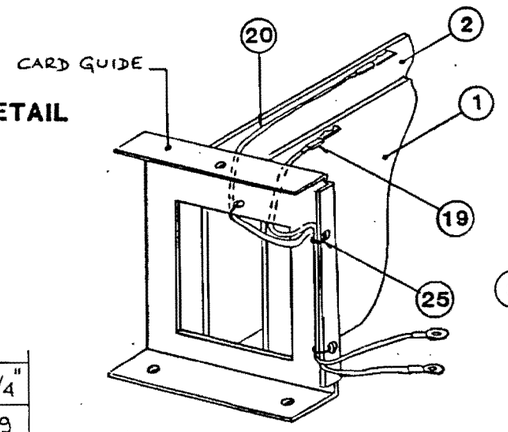
	change	rev	lss
RGW	ECO 1298	E	4
RGW	ECO 1298	D	3
	ECO 1248	C	2
	ECO 1216	B	1

title: **UNIT ASSEMBLY -FRONT BEZEL DETAIL**

Navtel

scale: NA	dwn: CP 8 NOV 88	appvd: M.Wing IC No. 86
prod: 9440	chkd: RGW 10.11.88	p.eng: IC No. 106
proj: F001	dwg: 03-100041B	
sht 4 of 6	rev: E	lss: 4

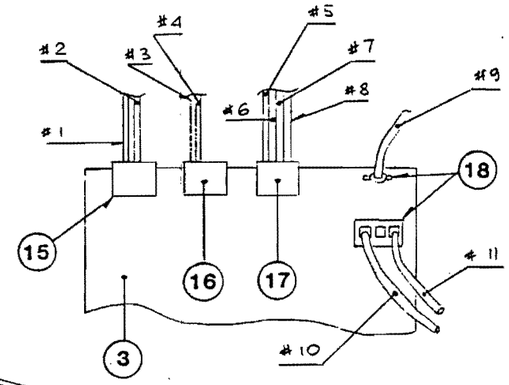
CARD GUIDE DETAIL



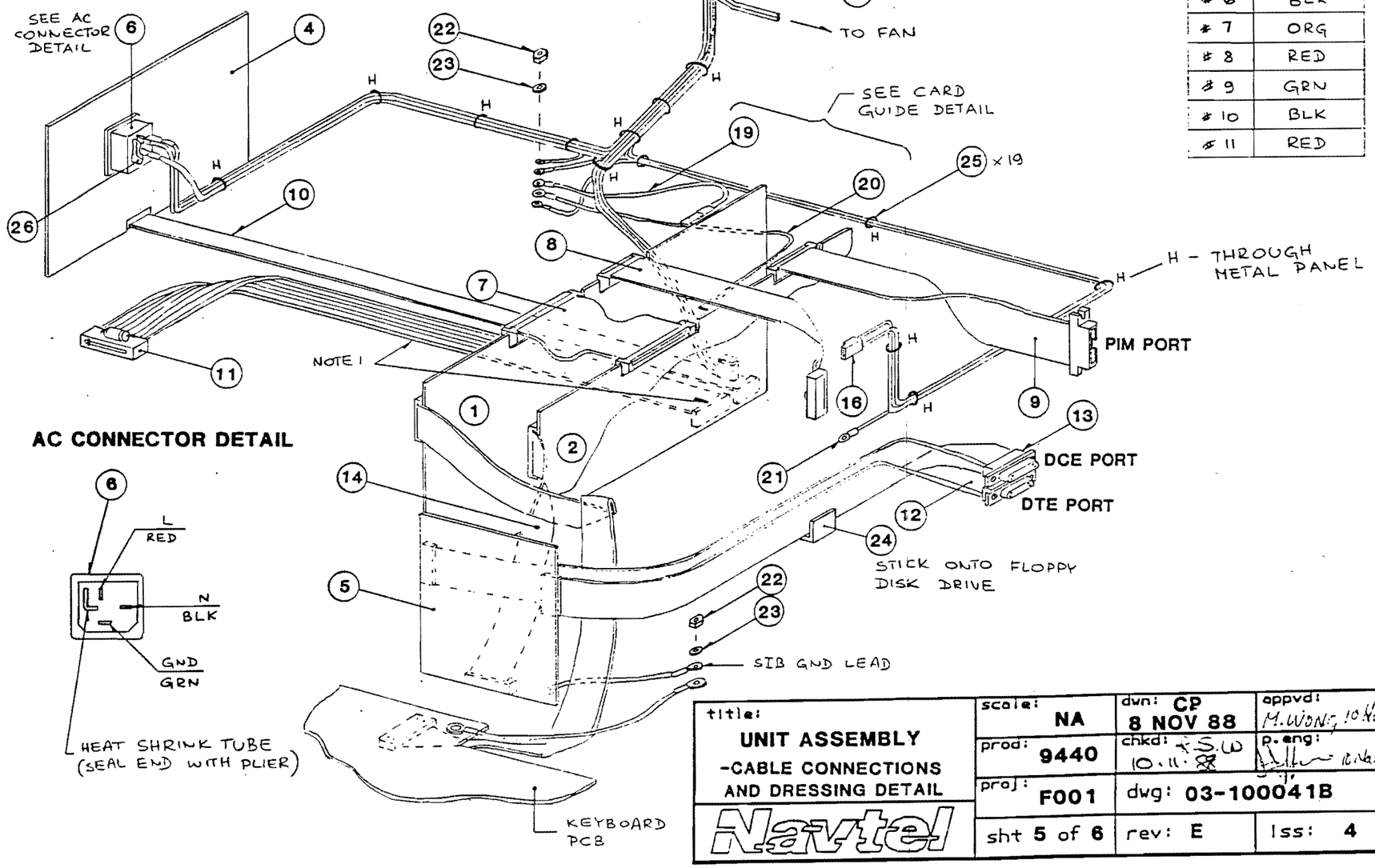
NOTE:
1. SECURE CRT CONNECTOR TO MPC BOARD WITH BEAD OF SILASTIC.

ITEM	DESCRIPTION	PART #	QTY.
26	HEAT SHRINK TUBE 1/2"DIA, CLEAR	61-100841A	3/4"
25	CABLE TIE	71-100539A	19
24	CABLE CLIP, ADHESIVE	077111	1
23	LOCKWASHER #6 INTERNAL TOOTH	65-100716A	2
22	NUT 6/32 HEX	074102	2
21	DISK DRIVE GND LEAD	59-100806A	1
20	PCB GND STRAP, DLC	59-100805A	1
19	PCB GND STRAP, MPC	58-100718A	1
18	CABLE AC POWER IN	59B100361B	1
17	CABLE DC POWER OUT	59B100362B	1
16	CABLE DISK DRIVE POWER	59B100365B	1
15	FAN ASSEMBLY	01-100417A	1
14	CABLE DLC/SIB	59B100283B	1
13	CABLE SIB/DCE PORT	59B100282B	1
12	CABLE SIB/DTE PORT	59B100281B	1
11	CRT CABLE ASSEMBLY	01-100364A	1
10	CABLE MPC/TRANSITION	59B100368B	1
9	CABLE DLC/PIM PORT	59B100284B	1
8	CABLE DISK DRIVE DATA	59B100366B	1
7	CABLE MPC/DLC BUSS	59B100369B	1
6	CONNECTOR, AC, SWITCH	60-100481A	1
5	SIB PCB ASSEMBLY	01-100045A	1
4	TRANSITION PCB ASSEMBLY	01-100285A	1
3	POWER SUPPLY ASSEMBLY	45-100279A	1
2	DLC FINAL ASSEMBLY	01-100043A	1
1	MPC FINAL ASSEMBLY	01-100042A	1

POWER SUPPLY CONNECTION DETAIL

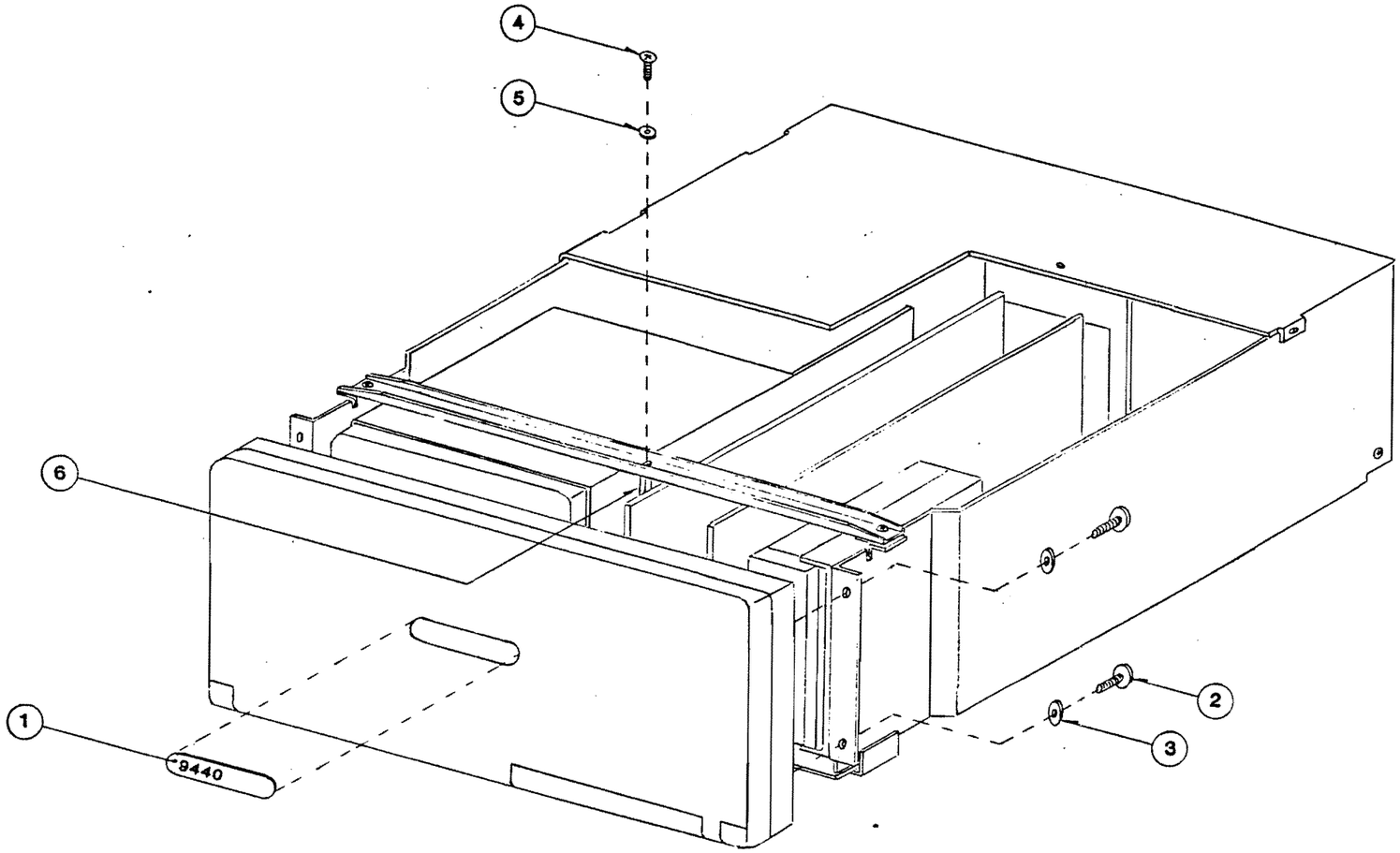


WIRE COLOUR CODING	
WIRE #	COLOUR
#1	RED
#2	BLK
#3	BLU
#4	YEL
#5	WHT
#6	BLK
#7	ORG
#8	RED
#9	GRN
#10	BLK
#11	RED



AC CONNECTOR DETAIL

title: UNIT ASSEMBLY -CABLE CONNECTIONS AND DRESSING DETAIL	scale: NA	dwn: CP 8 NOV 88	appvd: M. WONG 10 Nov 88
	prod: 9440	chkd: T.S.W 10.11.88	P. eng: 10 Nov 88
	proj: F001	dwg: 03-100041B	
Navtel	sht 5 of 6	rev: E	Iss: 4



NOTE:
1. MOVE THE CRT TOWARD THE BEZEL UNTIL .05 CLEARENCE REMAINS.

ITEM	DESCRIPTION	PART #	QTY.
6	STANDOFF HEX 6-32 x 4.5"	69-100838A	1
5	WASHER #6 INTERNAL TOOTH	65-100716A	1
4	SCREW 6-32 x 3/8 PAN PHILLIPS	073106	1
3	LOCKWASHER #8 INTERNAL TOOTH	65-100717A	4
2	SCREW 8-32 x 1/2" BINDING PHILLIPS	67-100719A	4
1	FRONT DECAL 9440	79-100751A	1

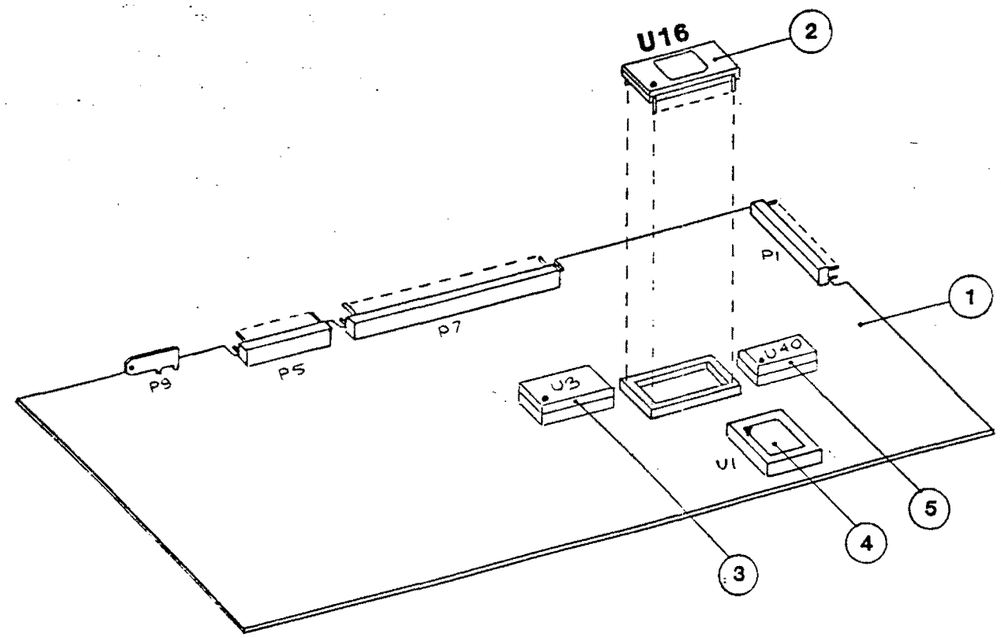
change	rev	lss
ECO 1298	E	4
ECO 1298	D	3
ECO 1248	C	2
ECO 1216	B	1

title: **UNIT ASSEMBLY**

Navtel

scale: NA	dwn: CP 8 NOV 88	appvd: M. WONG 10 NOV 88
prod: 9440	chkd: RSD 10-11-88	R. eng: [illegible] 10 NOV 88
proj: F001	dwg: 03-100041B	
sht 6 of 6	rev: E	lss: 4

DWG: **03-100042B**



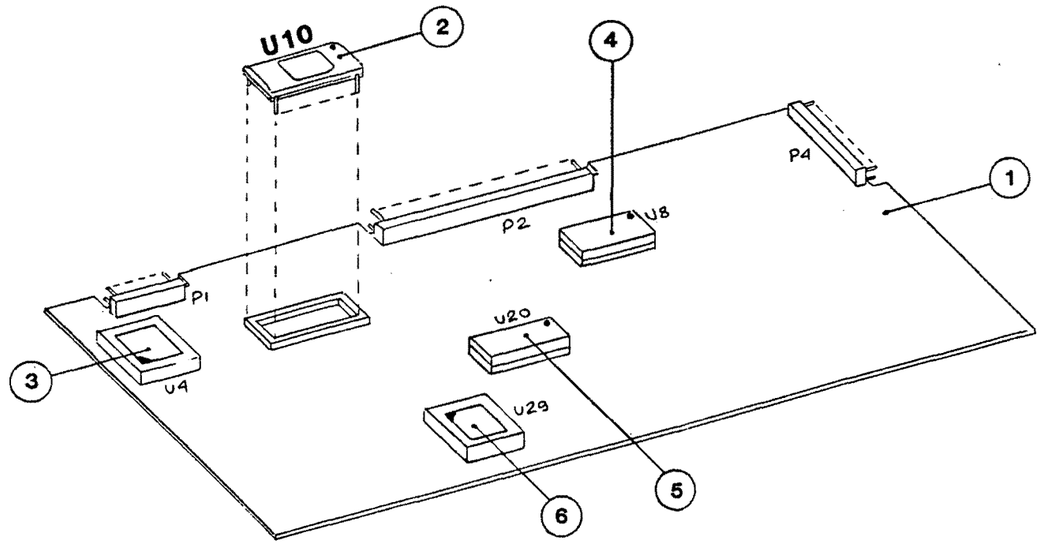
ITEM	DESCRIPTION	PART #	QTY.
5	EPLD2 ASSEMBLY FOR MPC-4	01-100693A	1
4	IC, N80C188-12, 8 BIT MICROPROCESSOR	30-100674A	1
3	EPLD1 ASSEMBLY FOR MPC-4	01-100346A	1
2	EPROM ASSEMBLY FOR MPC-4	01-100273A	1
1	MPC-4 PCB SUB ASSEMBLY	01-100270A	1

appvd.	change	rev.	iss.
RSW	ECO 1298	B	1

title: **MPC-4 PCB FINAL ASSEMBLY**

Navtel

scale: **NA**	dwn: **CP 8 JAN 89**	appvd: g.c	
prod: **9440**	chkd: RSW 10.01.89	p.eng:	
proj: **F001**	dwg: **03-100042B**		
sht **1** of **1**	rev: **B**	iss: **1**	



ITEM	DESCRIPTION	PART #	QTY.
6	MICRO PROCESSOR 80188, 8 BIT, 68 PIN	30-100268A	1
5	EPLD1 ASSEMBLY FOR DLC-4	01-100345A	1
4	EPLD2 ASSEMBLY FOR DLC-4	01-100692A	1
3	L4A 0093 TEST PORT INTERFACE CONTROLLER, 68 PIN	32-100155A	1
2	EPROM ASSEMBLY FOR DLC-4 PCB	01-100274A	1
1	DLC-4 PCB SUB ASSEMBLY	01-100271A	1

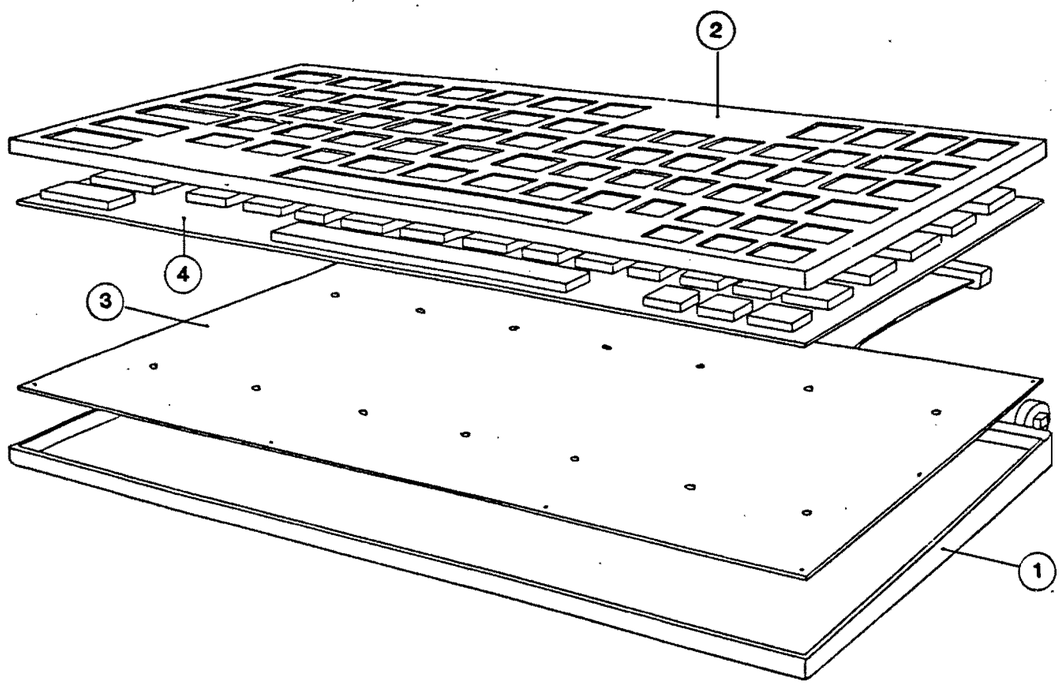
appvd.	change	rev.	iss.
J.A	ECO 1298	B	1

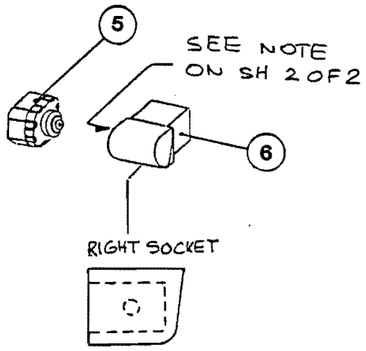
title: **DLC-4 PCB FINAL ASSEMBLY**

Navtel

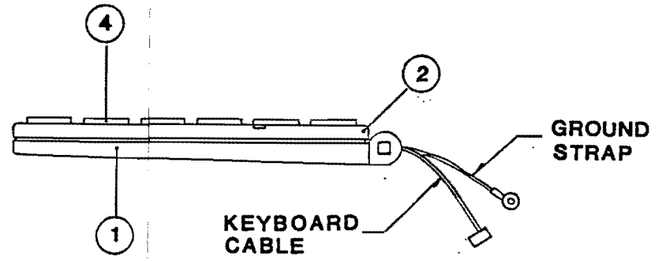
scale: **NA**	dwn: **CP 8 JAN 89**	appvd: J.A	
prod: **9440**	chkd: 10·01·89	p.eng:	
proj: **F001**	dwg: **03-100043B**		
sht **1** of **1**	rev: **B**	iss: **1**	

DWG: **03-100044B**

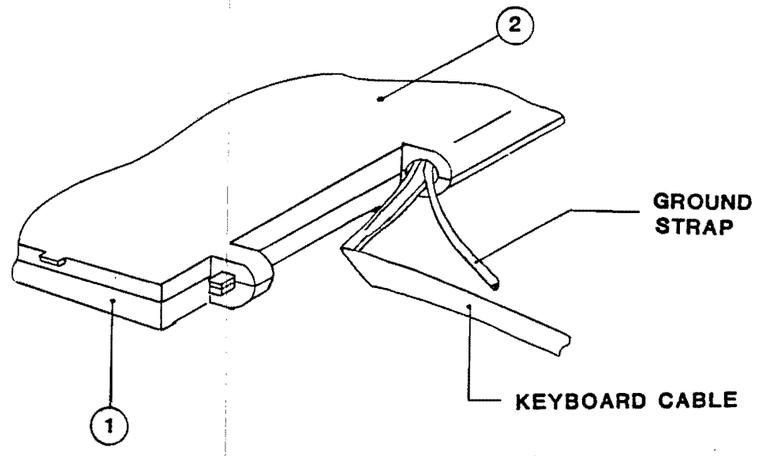




SIDE (RIGHT) VIEW



CABLE DETAIL (REAR VIEW)



ITEM	DESCRIPTION	PART #	QTY.
6	PLASTIC HINGE SOCKET (SET OF 2)	81-100183D	1
5	FOR HINGE DETAIL - SEE SHEET 2 OF 2	———	2
4	KEYBOARD, RUBBER KEY PAD OVERLAY	42-100275A	1
3	KEYBOARD PCB ASSEMBLY	01-100272A	1
2	PLASTIC KEYBOARD UPPER COVER	81-100181D	1
1	PLASTIC KEYBOARD LOWER TRAY	81-100180D	1

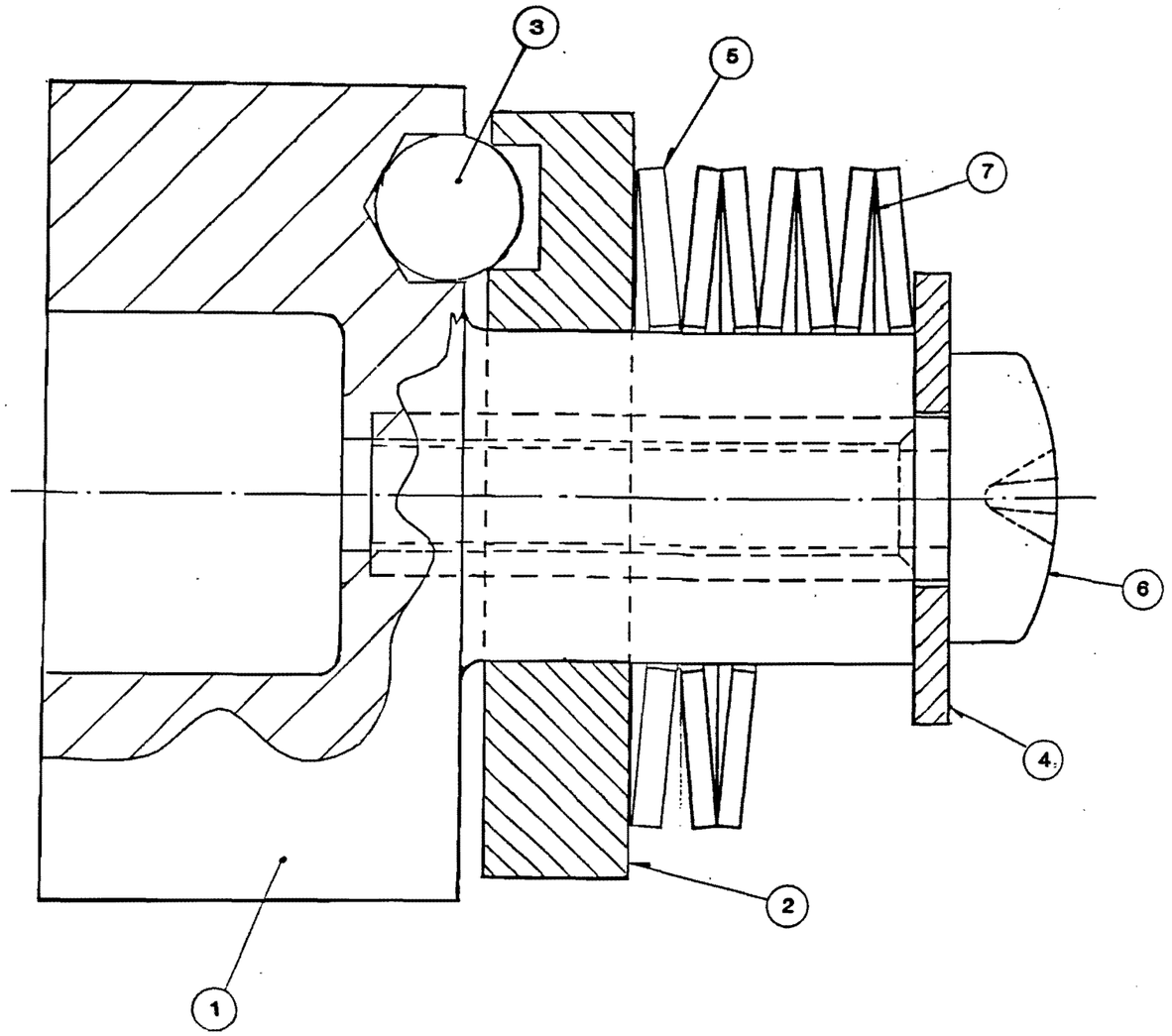
appvd.	change	rev.	iss.
RSW	ECO 1310	C	5
RSW	ECO 1310	C	4
	ECO 1248	B	3

title: **KEYBOARD FINAL ASSEMBLY**

Nortel

scale: **NA**	dwn: **CP 29 SEP 88**	appvd: CB 30-09-88	
prod: **9440**	chkd: RSW 30.9.88	p.eng:	
proj: **F001**	dwg: **03-100044B**		
sht **1** of **2**	rev: **C**	iss: **5**	

DWG: **03-100044B**



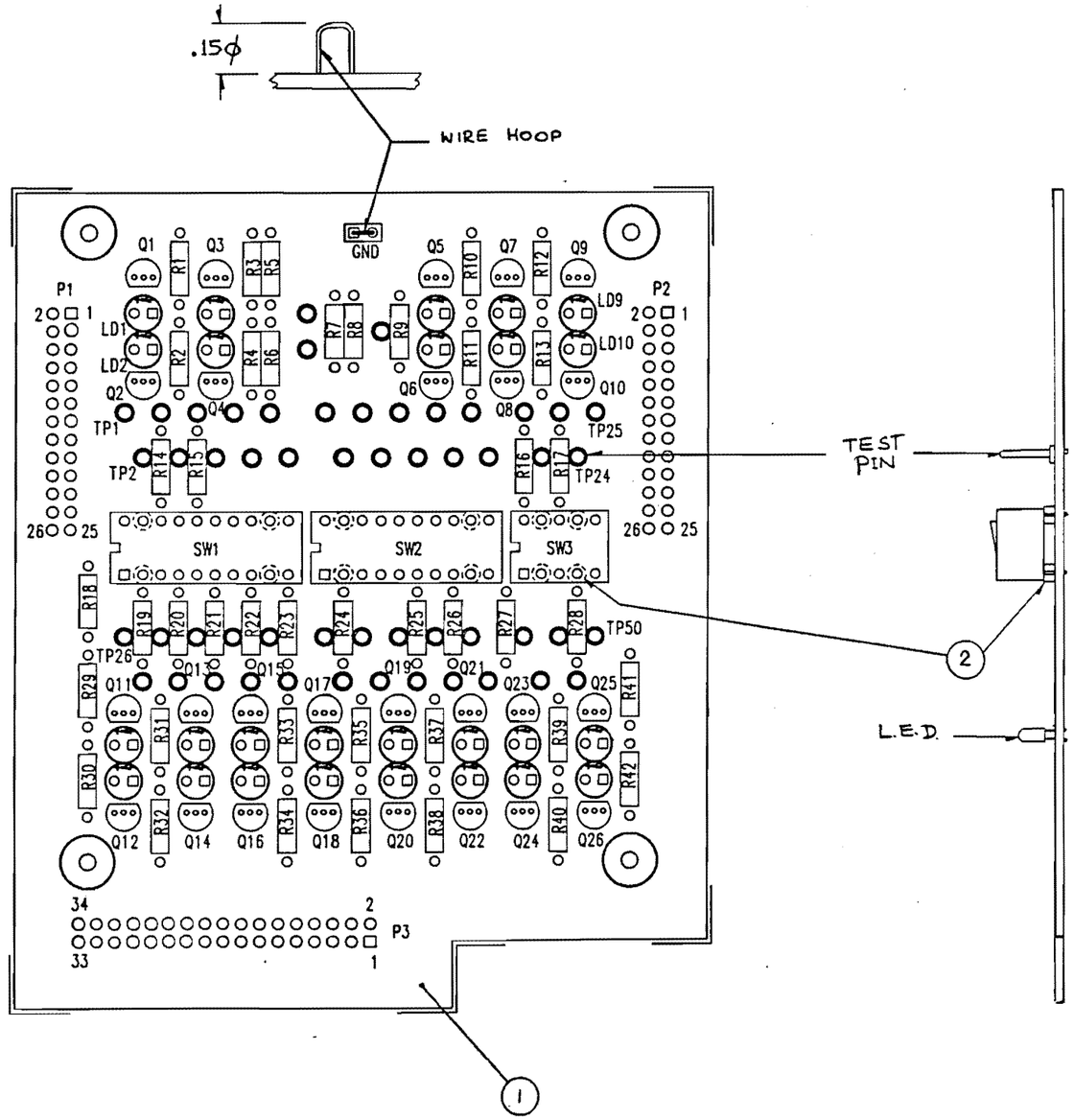
ITEM	DESCRIPTION	PART #	QTY.
1	INDEX SHAFT	81-100182C	2
2	INDEXING PLATE	80-100818B	2
3	BALL BEARING 1/8" DIA	69-100824A	6
4	WASHER # 6, BRASS	65-100857A	2
5	DISC SPRING	69-100825A	2
6	SCREW 4-24 x 3/8" TYPE H-L, PAN PHILLIPS	67-100858A	2
7	DISC SPRING	69-100898A	12

FOR MORE HINGE DETAILS
SEE DWG. 03-100044D

Before keyboard assembly is installed, lubricate hinge assembly disk spring and ball bearings with WD-40 lubricant (use tube applicator) and spray the inside of the hinge plastic socket with "white Lithium' grease.

appvd.	change	rev.	iss.
RGW	ECO 1310	C	5
DSW	ECO 1310	C	4
	ECO 1248	B	3

title: **KEYBOARD ASSEMBLY -HINGE DETAIL**	scale: **NA**	dwn: **CP 7 DEC 88**	appvd:
Navtel	prod: **9440**	chkd:	p.eng:
	proj: **F001**	dwg: **03-100044B**	
	sht **2** of **2**	rev: **C**	iss: **5**



ITEM	DESCRIPTION	PART #	QTY.
2	SPACER NYLON .187 x .ϕ9ϕ (9ϕ8 - ϕ9ϕ)	ϕ72145	12
1	SIB PCB	10:1000450V2	1

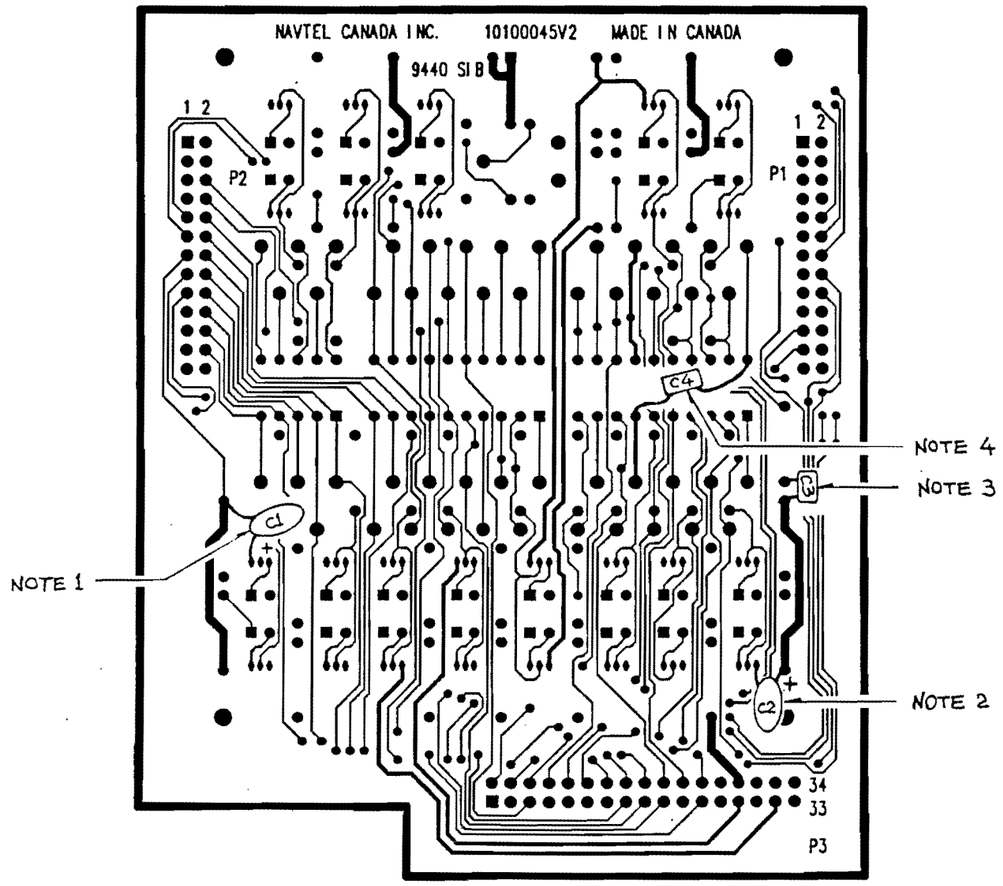
change	rev	iss
ECO1295	B	3
ECO1024	A	2

title: **SIB PCB ASSEMBLY**

Navtel

NAVTEL #01-100045A

scale: NA	dwn: CP 26 APR 88	appvd:
prod: 9440	chkd: 20.04.88	p.eng:
proj: F001	dwg: 03-100045B	
sht 1 of 2	rev: B	iss: 4



SOLDER SIDE VIEW

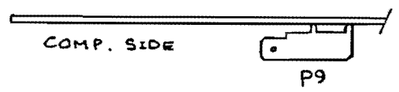
ON THE SOLDER SIDE

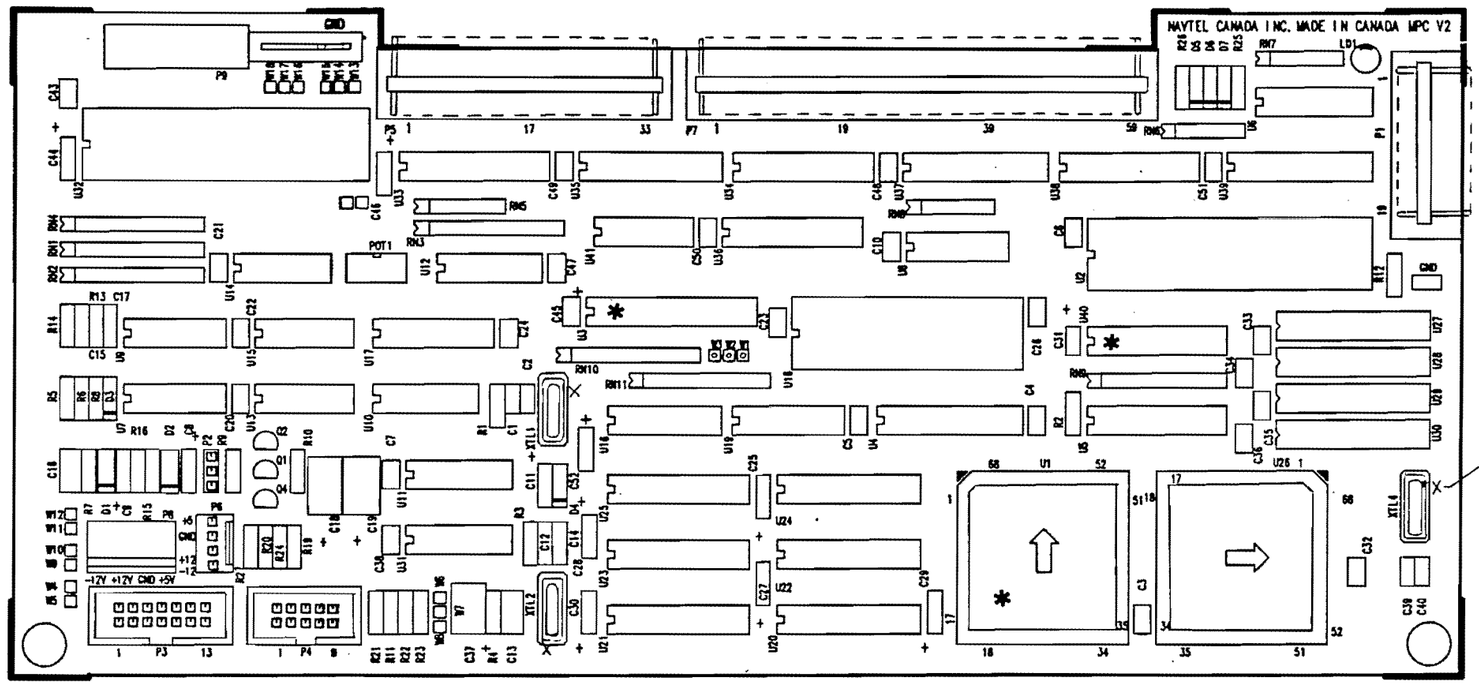
1. INSTALL CAPACITOR C1 BETWEEN Q25 COLLECTOR (POSITIVE SIDE) AND TOP END OF R41 (NEGATIVE SIDE).
2. INSTALL CAPACITOR C2 BETWEEN Q12 COLLECTOR (NEGATIVE SIDE) AND BOTTOM END OF R30 (POSITIVE SIDE).
3. INSTALL CAPACITOR C3 BETWEEN BOTTOM END OF R18 AND TOP END OF R29.
4. INSTALL CAPACITOR C4 BETWEEN SW1 PIN 20 AND SW1 PIN 7.

appvd.	change	rev.	iss.

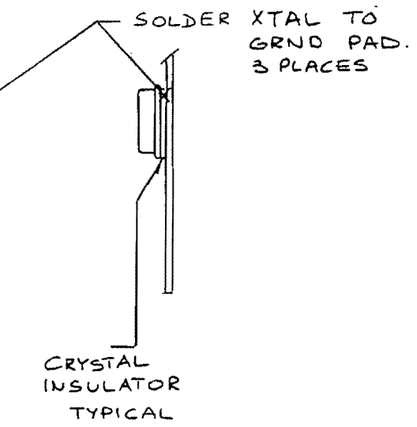
title: **9440 SIB PCB ASSEMBLY**	scale: **N/A**	dwn: **CHEN 07 FEB 89**	appvd:
Navtel	prod: **9440**	chkd:	p.eng:
	proj: **F001**	dwg: **03-100045B**	
	sht **2** of **2**	rev: **B**	iss: **4**

GND TERMINAL DETAIL





CRYSTAL DETAIL



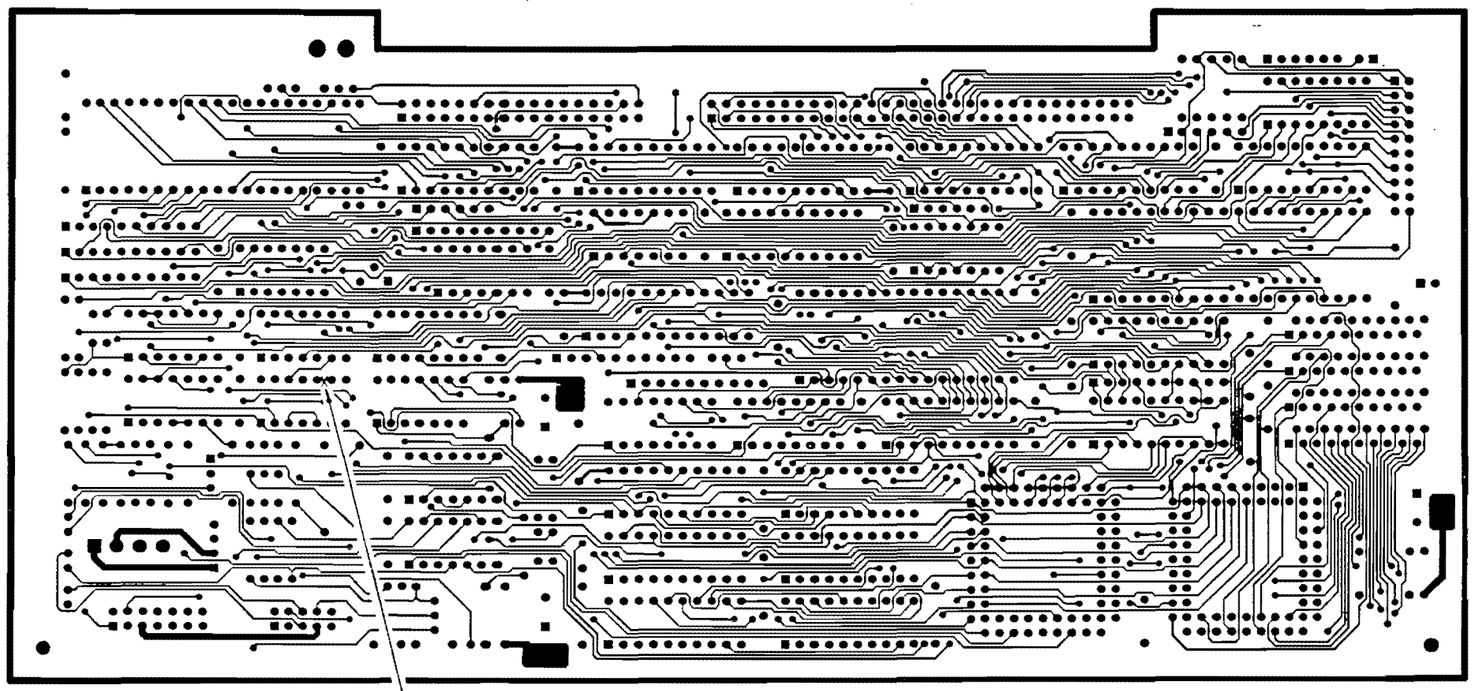
*** SHOWN FOR REFERENCE ONLY - PART OF FINAL ASSEMBLY**

NAVTEL #01-100270A

RSW	ECO 1328	C	5
RSW	ECO 1298	B	4
RSW	ECO 1185	A	3
	ECO 1185	A	2
appvd.	change	rev.	iss.

title: **MPC PCB ASSEMBLY**	scale: **NA**	dwn: **CP 6 OCT 88**	appvd:
	prod: **9440**	chkd: RSW 13.10.88	p.eng:
	proj: **F001**	dwg: **03-100270B**	
Navtel	sht **1** of **3**	rev: **C**	iss: **5**

DWG: **03-100270B**



NOTE 1

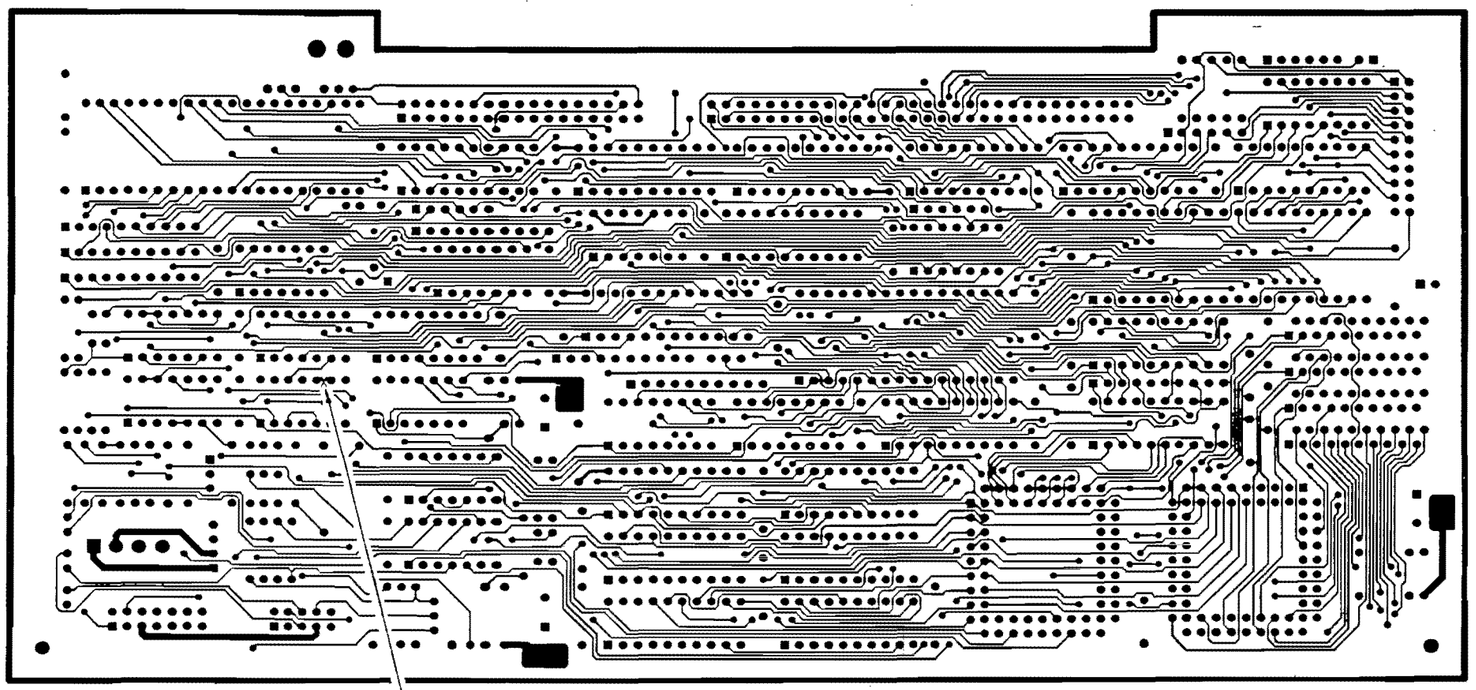
COMPONENT SIDE

NOTE 1 : CUT TRACE BETWEEN U13 PIN 9 AND U13 PIN 10.

appvd.	change	rev.	iss.
	ECO1328	C	5

title: MPC PCB ASSEMBLY	scale: N/A	dwn: CHEN 01 FEB 89	appvd:
	prod: 9440	chkd:	p.eng:
	proj: F001	dwg: 03-100270B	
Nortel	sht 2 of 3	rev: C	iss: 5

DWG: **03-100270B**



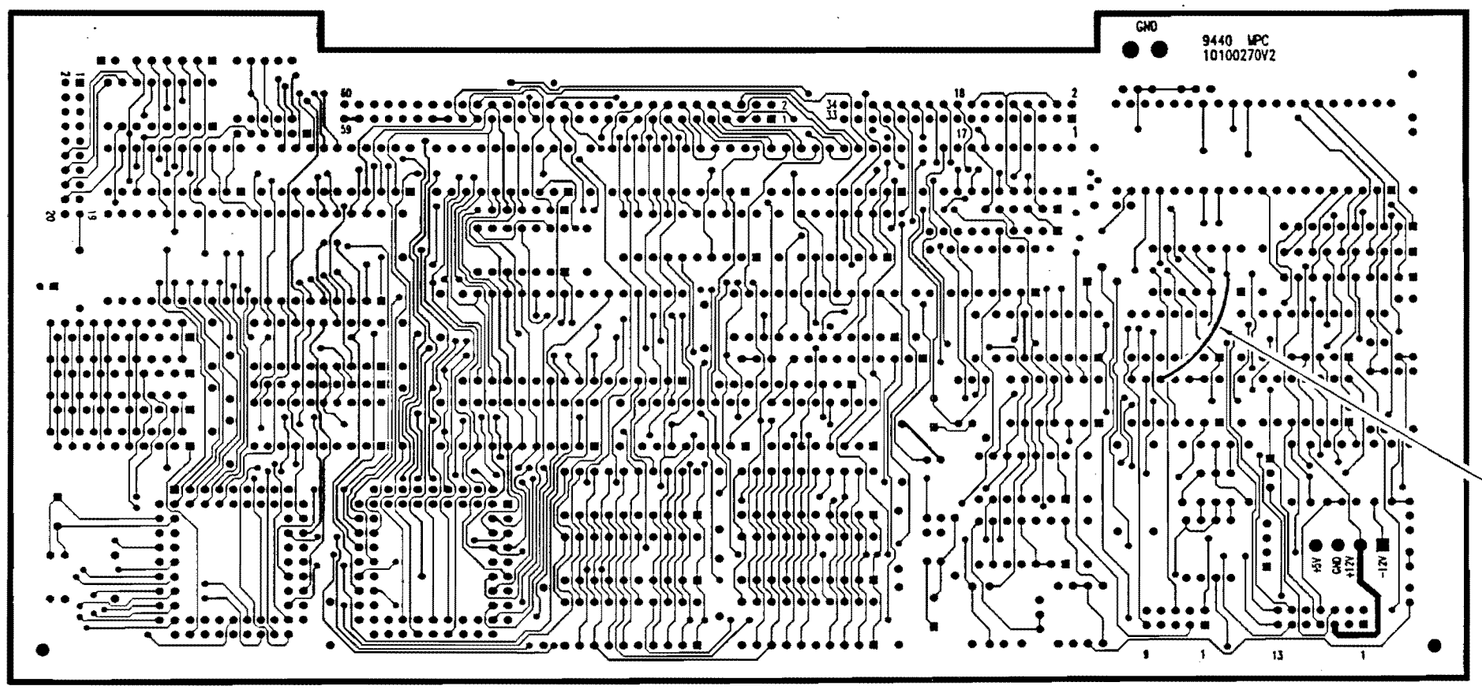
COMPONENT SIDE

NOTE 1 : CUT TRACE BETWEEN U13 PIN 9 AND U13 PIN 10.

appvd.	change	rev.	iss.
	ECO1328	C	5

title: **MPC PCB ASSEMBLY**	scale: **N/A**	dwn: **CHEN 01 FEB 89**	appvd:
	prod: **9440**	chkd:	p.eng:
	proj: **F001**	dwg: **03-100270B**	
Nortel	sht **2** of **3**	rev: **C**	iss: **5**

DWG: **03-100270B**



SOLDER SIDE

NOTE 2

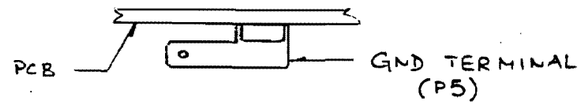
NOTE 2 : CONNECT A JUMPER BETWEEN U13 PIN 10 AND U14 PIN 13.

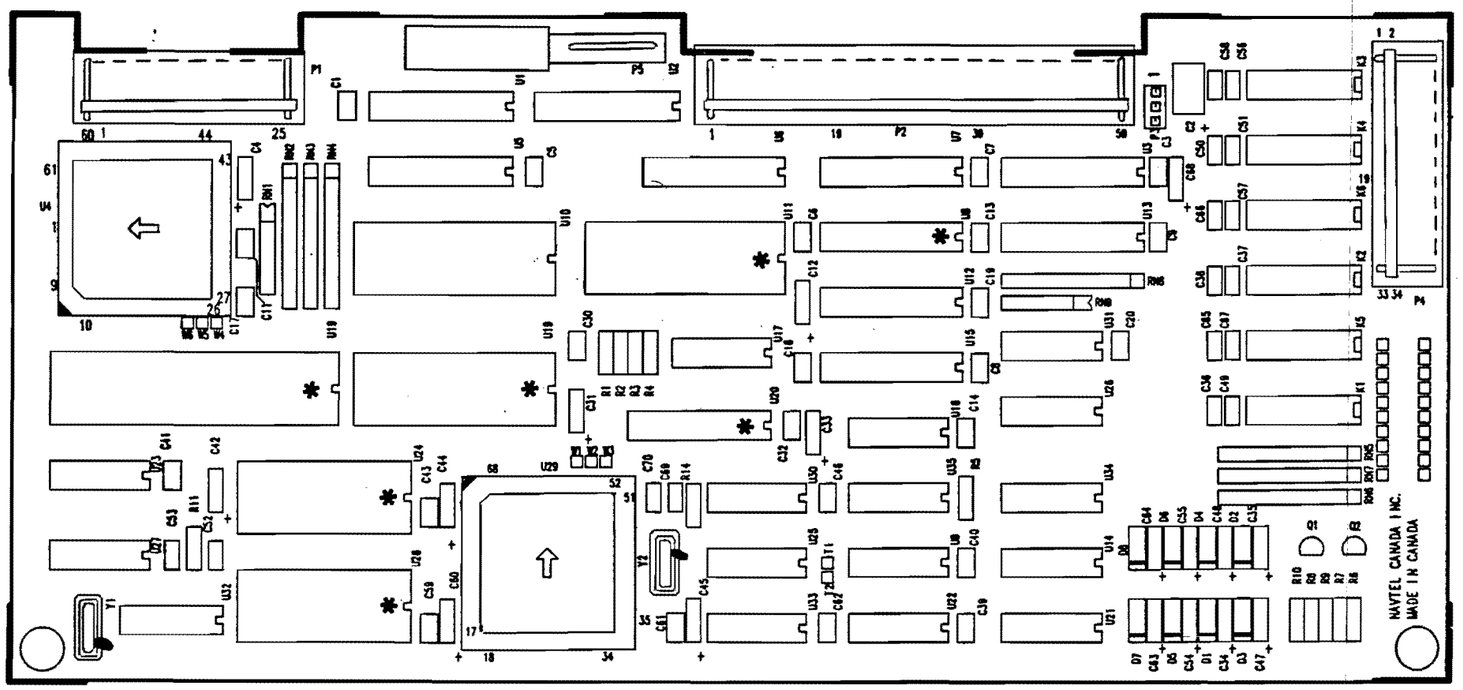
appvd.	change	rev.	iss.
	ECO1328	C	5

title: **MPC PCB ASSEMBLY**	scale: **N/A**	dwn: **CHEN 01 FEB 89**	appvd:
	prod: **9440**	chkd:	p.eng:
	proj: **F001**	dwg: **03-100270B**	
Navtel	sht **3** of **3**	rev: **C**	iss: **5**

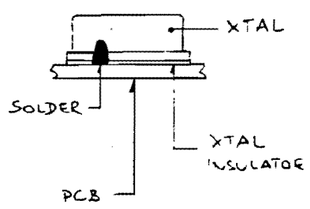
DWG: **03-100271B**

GND TERMINAL DETAIL





XTAL DETAIL



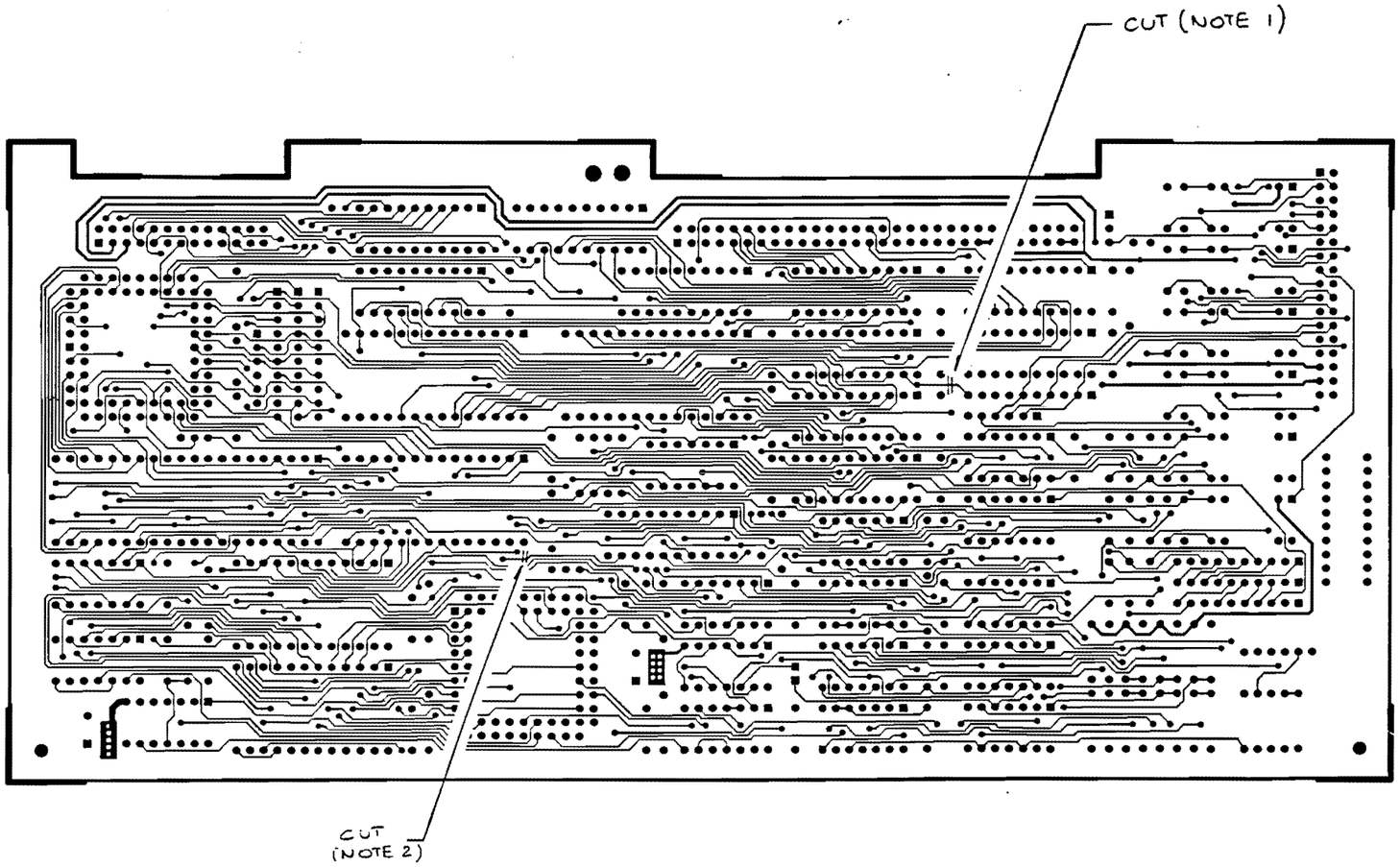
*** ALL THESE SOCKETS TO BE REMOVED AFTER THE PILOT RUN**

appvd.	change	rev.	iss.
J.A	ECO1268	D	4
	ECO1227	C	3
	ECO1162	B	2
	ECO 1162	B	1

title: **DLC PCB ASSEMBLY**	scale: **NA**	dwn: **CP 23 SEP 88**	appvd:
	prod: **9440**	chkd: 28.9.87	p. engr
	proj: **F001**	dwg: **03-100271B**	
Navtel	sht **1** of **3**	rev: **D**	iss: **4**

DWG: **03-100271B**

COMPONENT SIDE VIEW



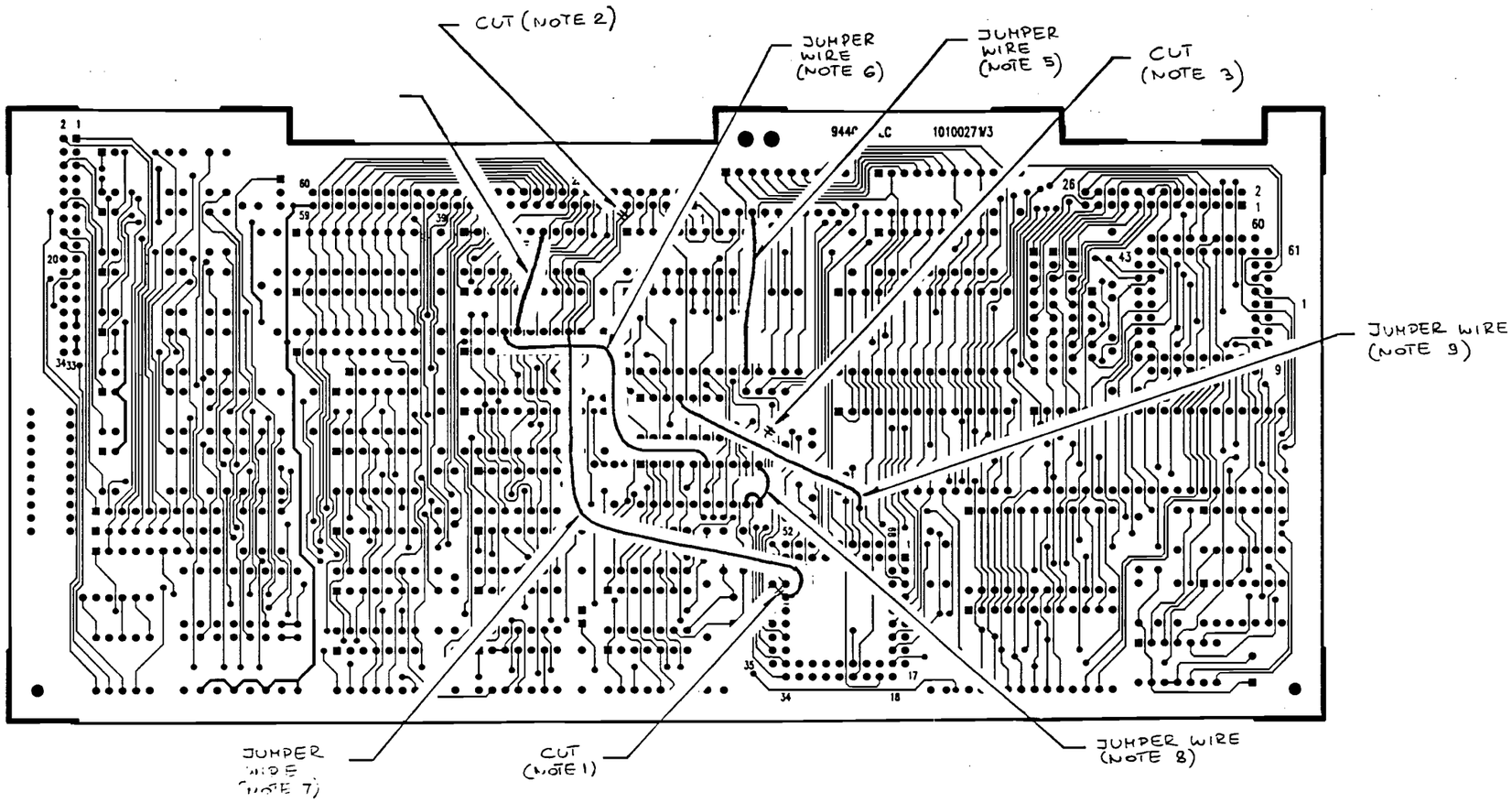
ON COMPONENT SIDE:

1. CUT TRACE BETWEEN RN8 PIN 10 AND FEED THROUGH (FROM U8 PIN 19).
2. CUT TRACE BETWEEN U20 PIN 12 AND FEED THROUGH

appvd.	change	rev.	iss.
J.H.	ECO 1268	D	4
AH	ECO 1227	C	3
DSD	ECO 1162	B	2
	ECO 1162	B	1

title: **DLC PCB ASSEMBLY**	scale: **NA**	dwn: **CP 23 SEP 88**	appvd:
	prod: **9440**	chkd: RSW 28.9.88	p.eng:
	proj: **F001**	dwg: **03-100271B**	
Navtel	sht **2** of **3**	rev: **D**	iss: **4**

DWG: **03-100271B**



SOLDER SIDE VIEW

ON SOLDER SIDE:

1. CUT TRACE BETWEEN U29 PIN 46 AND U29 PIN 47.
2. CUT TRACE BETWEEN U8 PIN 12 AND P2 PIN 11.
3. CUT TRACE GOING INTO U20 PIN 11.
4. ADD JUMPER WIRE BETWEEN U7 PIN 7 AND U8 PIN 16.
5. ADD JUMPER WIRE BETWEEN U2 PIN 18 AND U11 PIN 19.
6. ADD JUMPER WIRE BETWEEN U8 PIN 17 AND U20 PIN 6.
7. ADD JUMPER WIRE BETWEEN U29 PIN 46 AND U8 PIN 12.
8. ADD JUMPER WIRE BETWEEN U20 PIN 10, U20 PIN 11 AND U20 PIN 12
9. ADD JUMPER WIRE BETWEEN VIA AS SHOWN AND U17 PIN 4

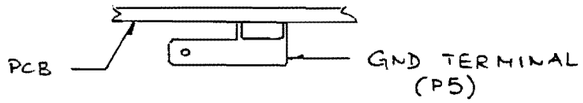
EACH JUMPER WIRE SHOULD BE GLUED TO THE BOARD.

appvd.	change	rev.	iss.
	ECO 1268	D	4
	ECO 1227	C	3
	ECO 1162	B	2
	ECO 1162	B	1

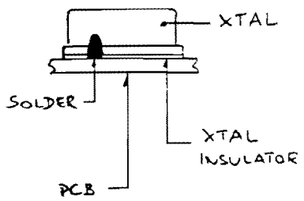
title: **DLC PCB ASSEMBLY**	scale: **NA**	dwn: **CP 27 SEP 88**	appvd:
	prod: **9440**	chkd:	p.eng:
Navtel	proj: **F001**	dwg: **03-100271B**	
	sht **3** of **3**	rev: **D**	iss: **4**

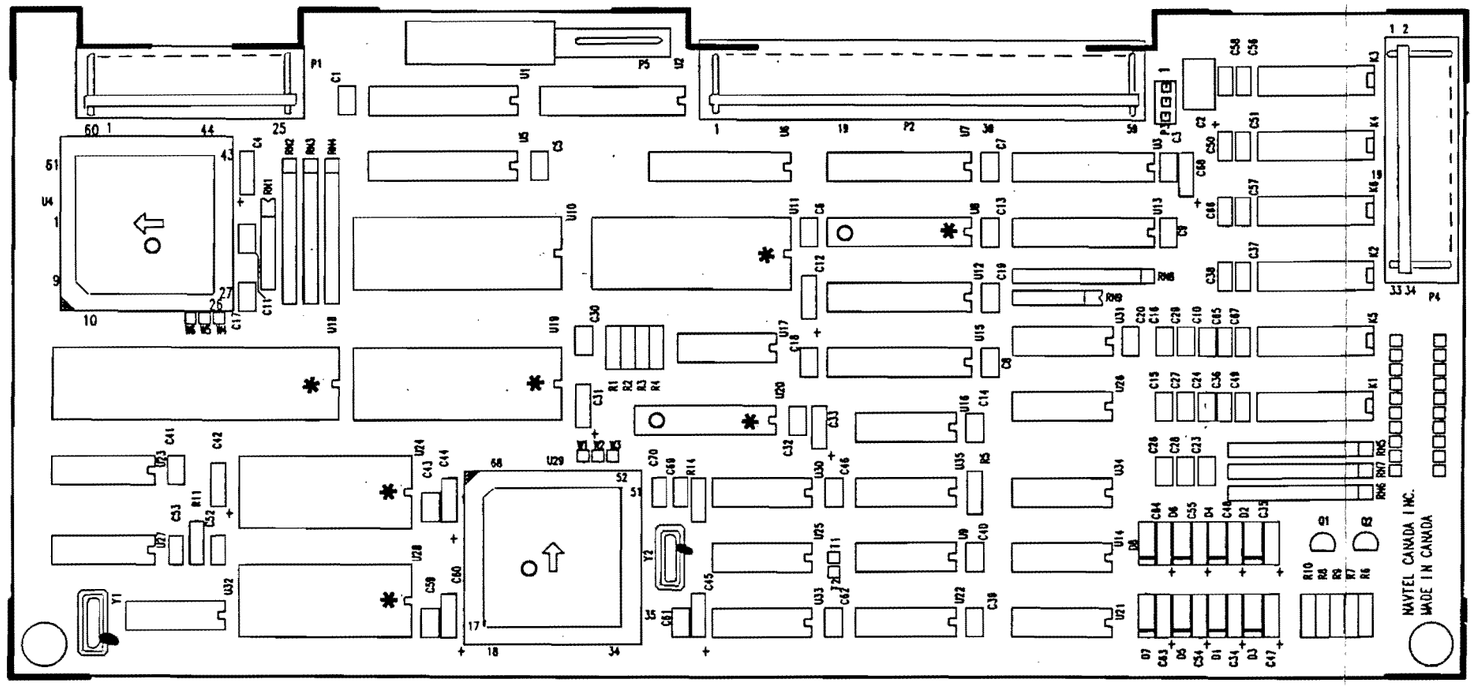
DWG: **03-100271B**

GND TERMINAL DETAIL



XTAL DETAIL





*** ALL THESE SOCKETS TO BE REMOVED AFTER THE PILOT RUN**

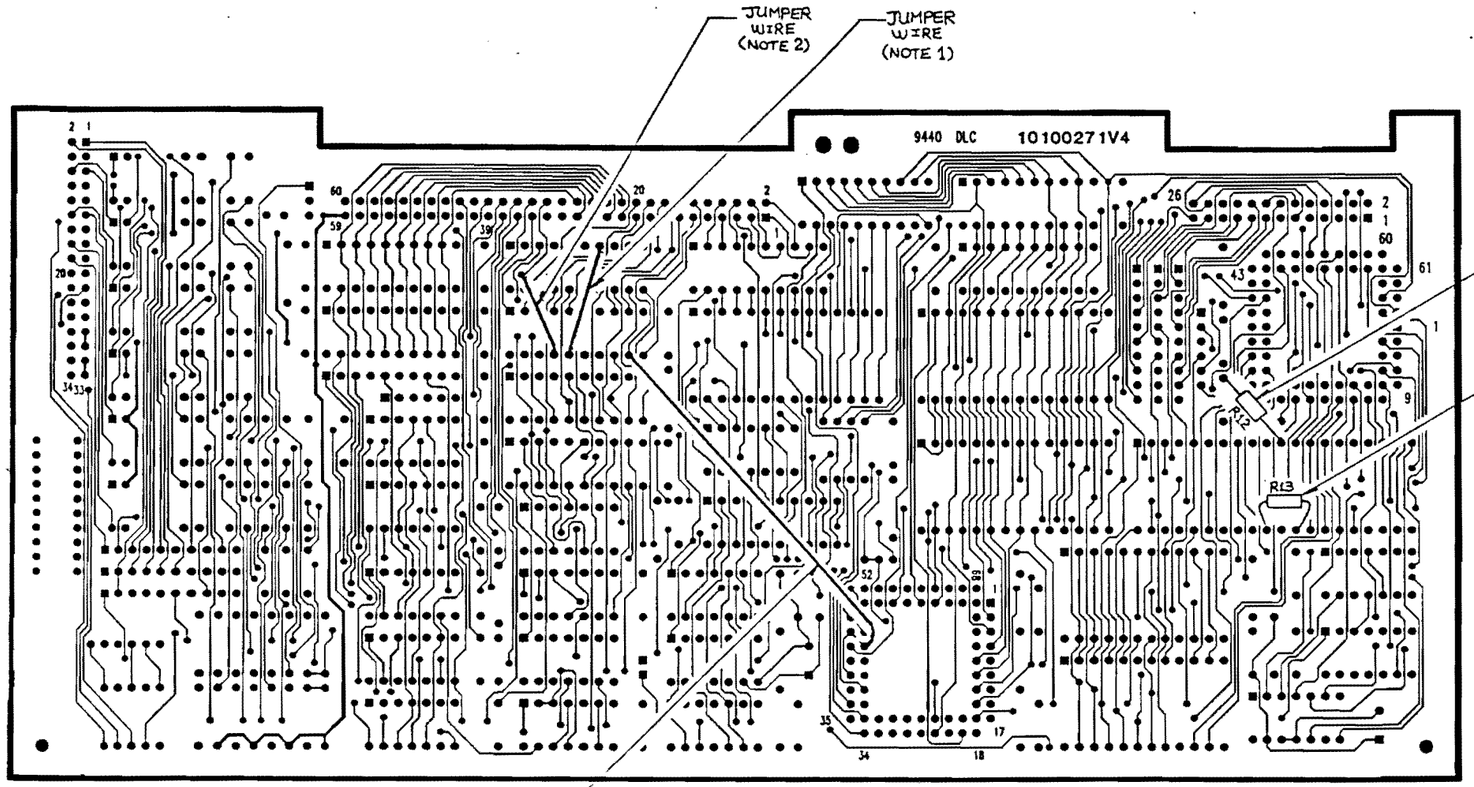
O SHOWN FOR REFERENCE ONLY-PART OF FINAL ASSEMBLY

appvd.	change	rev.	iss.
T.H.	ECO1310	E	7
DSW	ECO 1295	E	6
T.H.	ECO 1295	E	5
T.H.	ECO1275	D	4
PH	ECO1227	C	3
DSW	ECO 1162	B	2
	ECO 1162	B	1

NAVTEL #01-100271A

title: 9440 DLC PCB ASSEMBLY	scale: NA	dwn: CP 23 SEP 88	appvd:
	prod: 9440	chkd: DSW 28.9.88	p.engr:
Navtel	proj: F001	dwg: 03-100271B	
	sht 1 of 2	rev: E	iss: 7

DWG: **03-100271B**



SOLDER SIDE VIEW

EACH JUMPER WIRE SHOULD BE GLUED TO THE BOARD.

ON SOLDER SIDE:

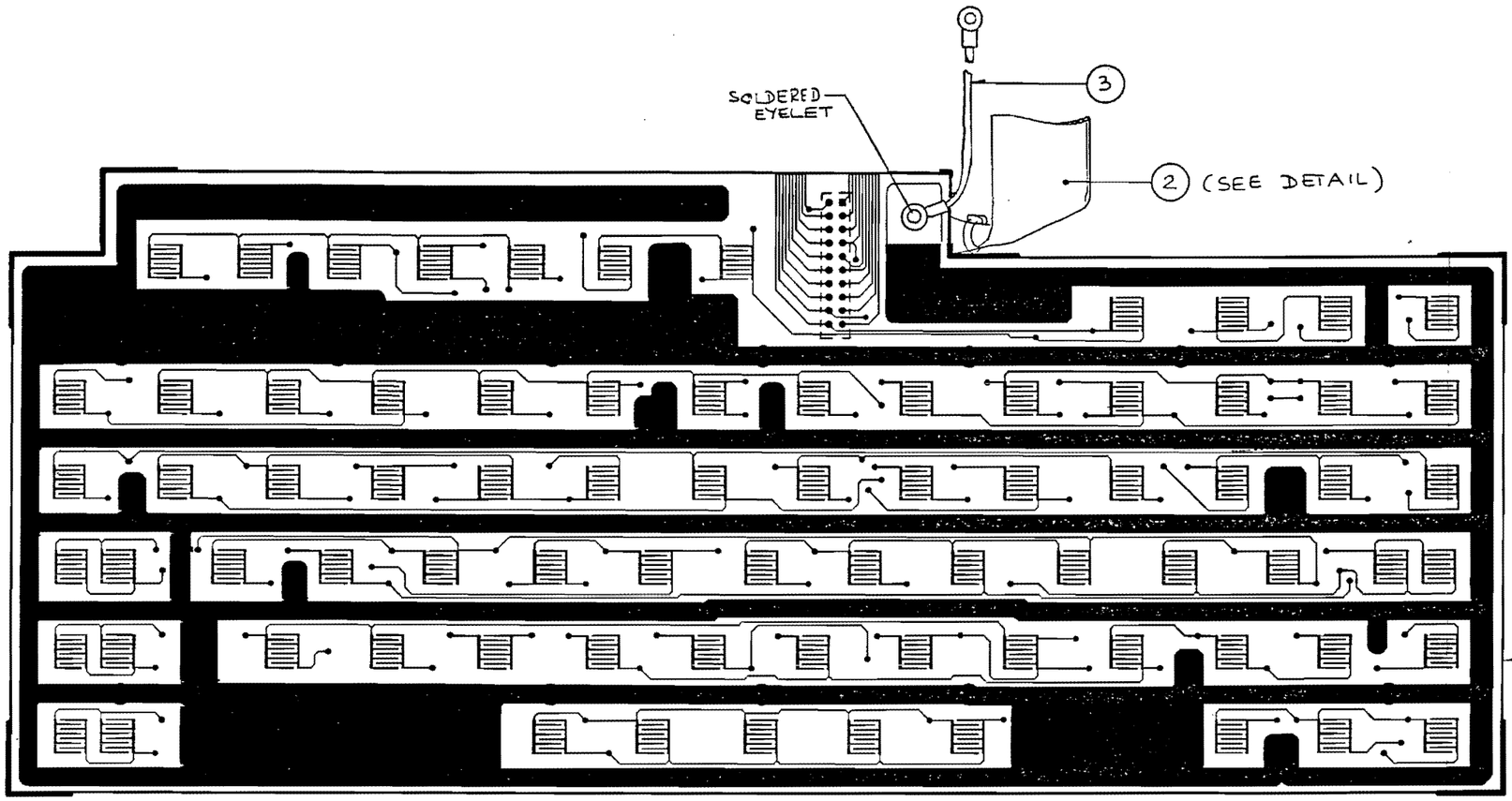
1. ADD JUMPER WIRE BETWEEN U7 PIN 7 AND U8 PIN 16.
2. ADD JUMPER WIRE BETWEEN U8 PIN 17 AND VIA AS SHOWN.
3. ADD JUMPER WIRE BETWEEN U29 PIN 46 AND U8 PIN 12.
4. INSTALL RESISTOR R12 BETWEEN U18 PIN 11 AND CAPACITOR (AS SHOWN) C11 - GND.
5. INSTALL RESISTOR R13 BETWEEN U18 PIN 29 AND U18 PIN 31 - GND. USE TUBE INSULATOR AS REQUIRED.

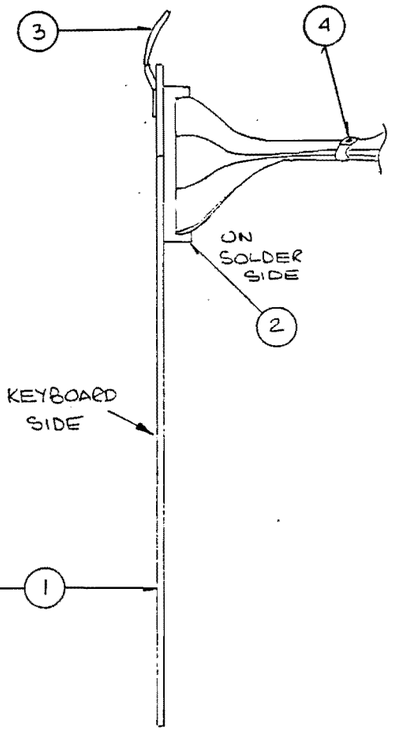
NAVTEL #01-100271A

appvd.	change	rev.	iss.
P.K	ECO1310	E	7

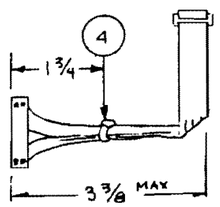
title: **9440 DLC PCB ASSEMBLY**	scale: **N/A**	dwn: **CHEN 16 JAN 89**	appvd:
	prod: **9440**	chkd: RSW 18 JAN 89	p.eng:
	proj: **F001**	dwg: **03-100271B**	
Navtel	sht **2** of **2**	rev: **E**	iss: **7**

DWG: **03-100272B**





VIEWED FROM KEYBOARD SIDE



CABLE FOLDING DETAIL

ITEM	DESCRIPTION	PART #	QTY.
4	CABLE TIE	71-1005394	1
3	GROUND STRAP	59B100511A	1
2	CABLE, MPC TO KEYBOARD	59B100363B	1
1	KEYBOARD PCB	101100272V2	1

appvd.	change	rev.	iss.
	ECO 1165	B	1

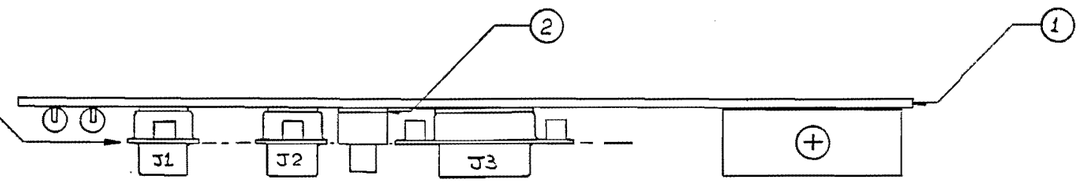
title: **KEYBOARD PCB ASSEMBLY**

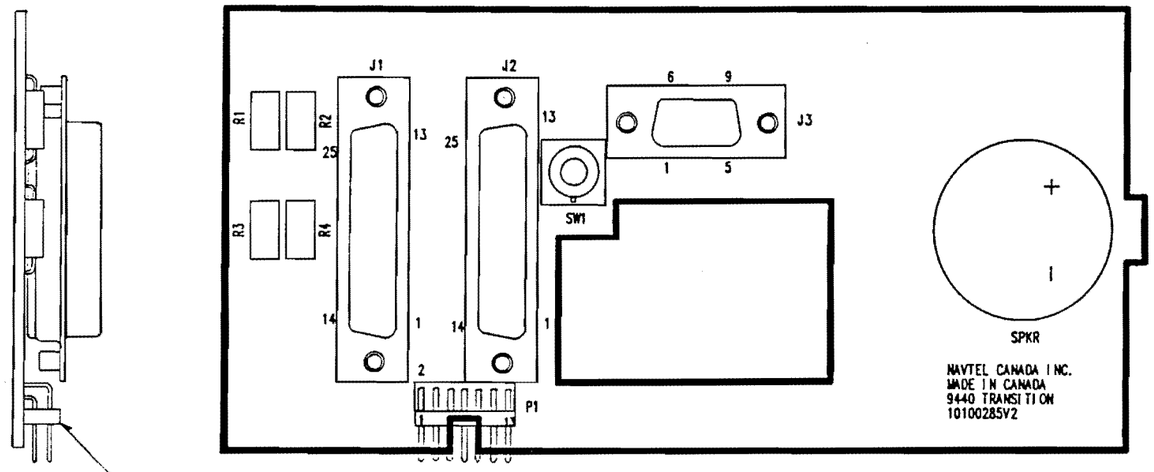
Nortel

scale: **NA**	dwn: **CP 28 SEP 88**	appvd: EB 30-09-88	
prod: **9440**	chkd: 28.9.88	p.eng:	
proj: **F001**	dwg: **03-100272B**		
sht **1** of **1**	rev: **B**	iss: **1**	

DWG: **03-100285B**

THE FLANGES OF D CONNECTORS FOR J1, J2, J3 AND SW1 SHOULD BE MAINTAINED AT SAME LEVEL. (THEY SHOULD BE PUSHED ALL THE WAY DOWN AND FLUSH WITH THE BOARD)





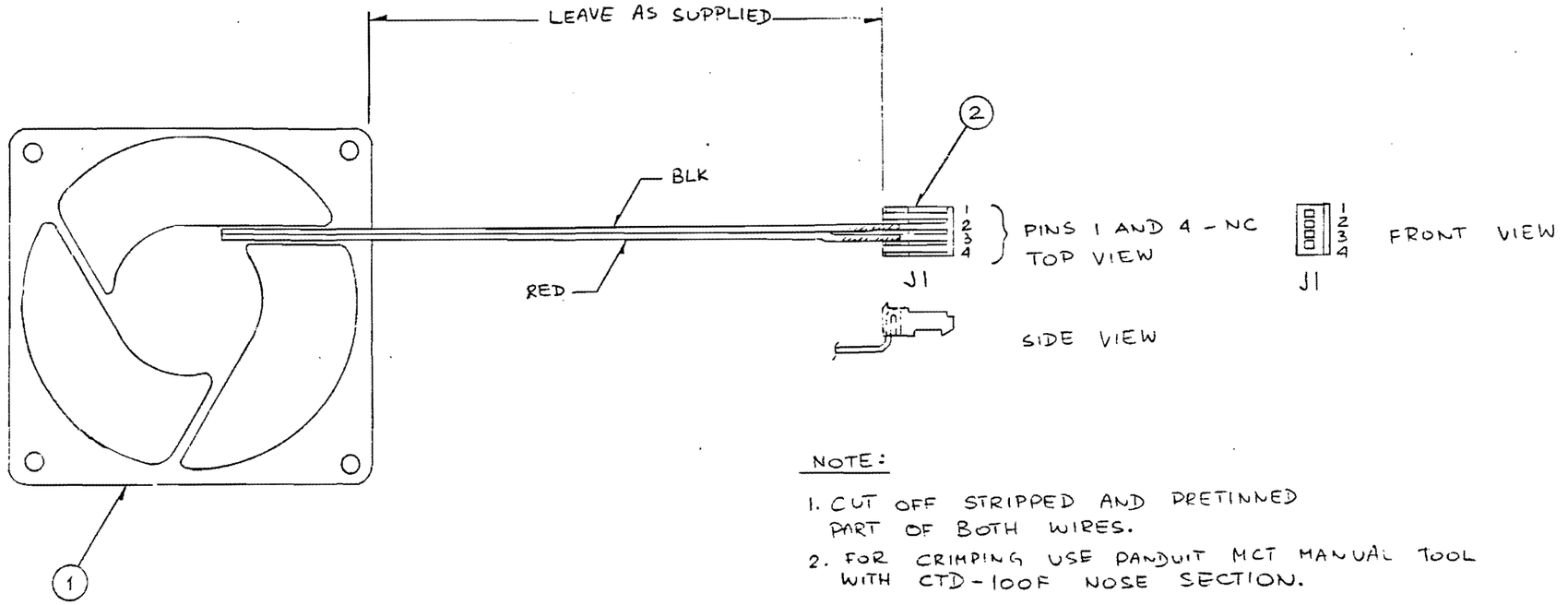
THE PINS OF RIGHT ANGLE HEADER SHOULD BE PERFECTLY PARALLEL WITH THE BOARD.

NAVTEL #01-100285A

ITEM	PART NUMBER	DESCRIPTION	QTY
2	072 116	INSULATOR FOR TO-5 SWITCHES	1
1	10100285V2	PCB, TRANSITION 9440	1

appvd.	change	rev.	iss.
	ECO 1162	A	1

title: 9440 TRANSITION PCB ASSEMBLY	scale: N/A	dwn: CHEN 26 SEP 88	appvd:
	prod: 9440	chkd: DSW 28.9.88	p.eng:
Navtel	proj: F001	dwg: 03-100285B	
	sht 1 of 1	rev: A	iss: 1



NOTE:

1. CUT OFF STRIPPED AND PRETINNED PART OF BOTH WIRES.
2. FOR CRIMPING USE PANDUIT MCT MANUAL TOOL WITH CTD-100F NOSE SECTION.

CONNECTION TABLE		
FROM	COLOUR	TO
FAN-RED	RED	J1-3
FAN-BLK	BLACK	J1-2

ITEM	DESCRIPTION	PART #	QTY.
2	TERMINAL HOUSING .1, WITH PRELOADED TERMINALS	54-100162A	1
1	FAN, 12 VDC	45-100410A	1

change	rev	iss
ECO 1273	A	3
ECO 1074	1	2

title: **FAN ASSEMBLY**

Navtel

scale: NA	dwn: CP 26 FEB 88	appvd: M. Wing 27 May 88
prod: 9440	chkd:	D. eng: 31 May/88
proj: F001	dwg: 03-100417B	
sht 1 of 1	rev: A	iss: 3

dwg#: 04-100041B iss: 9

60-100481A
113V AC
CONNECTOR/SW.

59B100361B

59B100511A

KEYBOARD
01-100272A
P1

CRT
35-100280A
P1

(PART# T3A)
DISK
P2 P1

59-100806A

TRANSITION
PCB
01-100285A

SPEAKER

SW1 RESET

2X10
59B100363B

01-100364A
(59B100364B)

J22
2X5

J21
1X4

J20
2X17

59B100365B

59B100366B

J14
2X10

J12
2X5

J9
2X17

J10
1X4

J25 J26
1X4

J15
1X4

E J1
POWER
SUPPLY
45-100279A

J4 J3 J2

P1

+12V
+5V
GND

-12V
+12V
GND
+5V
P6

P1 P4 P5

MPC-4
01-10042A

P3

J7
2X7

J2
2X7
P1

J1
DCE
PRINTER
PORT (D25S)

J2
DTE
EMCRT/REMOTE
PORT (D25S)

59B100368B

P8 P9

TURBO PWR

P7

P2
TEST

J6
2X30

59B100369B

FUTURE OPTIONS

59B100362B

59-100718A

59-100805A

A

J16
2X30

J17
2X17

P5

P2

FAN

01-100417A

59B100283B

P4

2X17

P3

J19
2X13

P1

PIM PORT
(ID26P)

59B100284B

P2

DLC-4
01-100043A

P3
1X3
TEST

J5

DTE
TEST PORT
(D25S)

59B100281B 2X13

P2

SIB-2
01-100045A

59-100282B

DCE
TEST PORT
(D25S)

P1

2X13

J23

STATUS
INDICATOR
BREAKOUT BOX

59-100873A

B

ECO1318	D	9
change	rev	iss

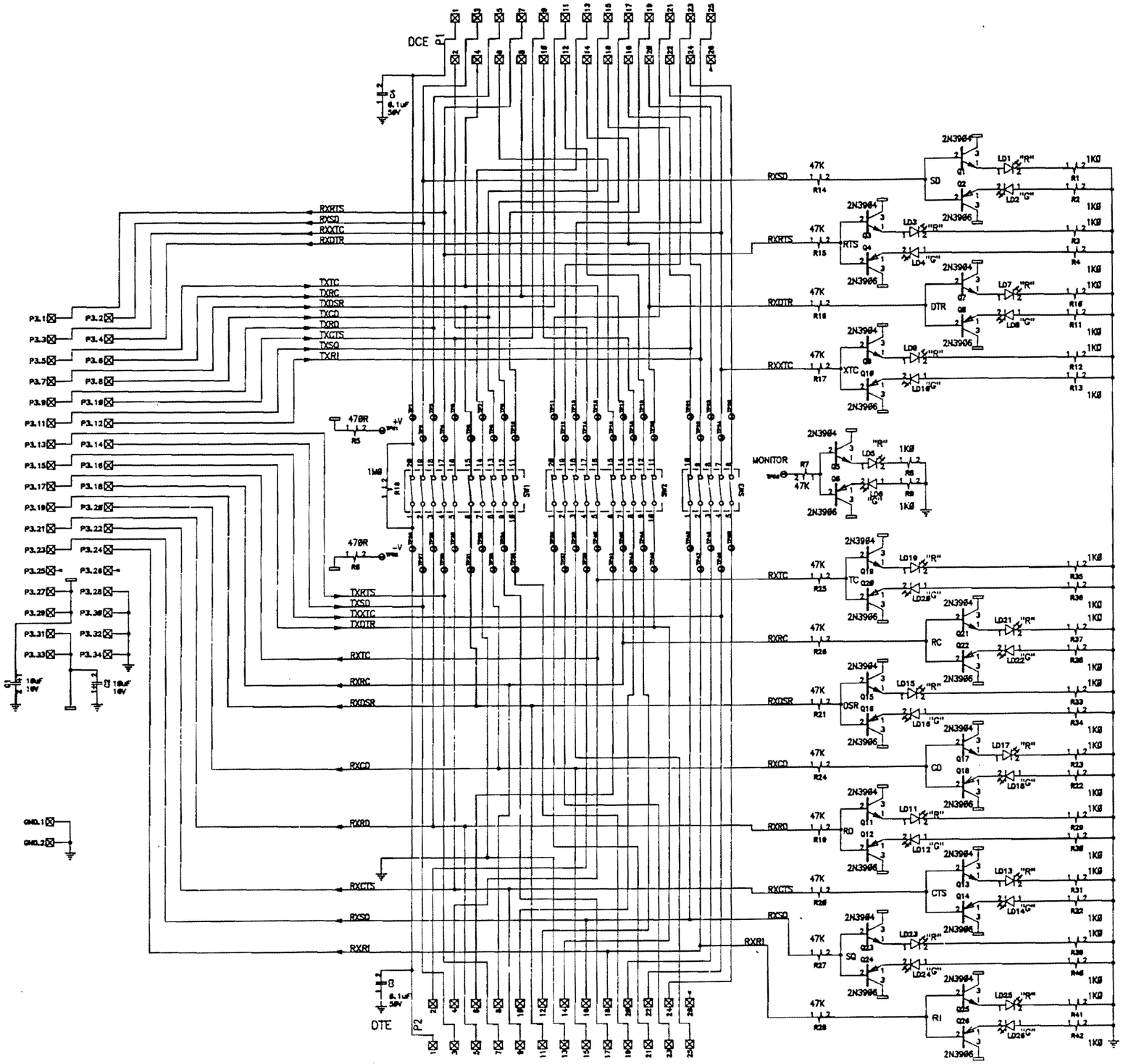
title: 9440 SYSTEM BLOCK DIAGRAM

Navtel

scale: NONE	dwn: CHEN	appvd:
prod: 9440	chkd:	p.eng:
proj: F001	dwg: 04-100041B	
sht 1 of 1	rev: D	iss: 9

PCAD\04100041

REV	DESCRIPTION	DATE
B:2	ADDED C1, C2, C3, C4.	19 JAN 89



eco 1318	B	2	title: 9440 STATUS INDICTOR BOARD	assist: NONE	draft: P.H.	approval:
change	rev	iss	NAVTEL	proj: 9440	engr:	p.engr:
				proj: F001	dwg: 04-100045C	
				sht 1 of 1	rev: B	iss: 2

PCAD\84100045

REV	DESCRIPTION	DATE
C:3	R25 WAS 10K Ω	01 FEB 89

OPTIONAL POWER ON INDICATOR

1K

GND CLIP HOOP

GND TAB

8256 U2

80C188-12 U1

74HC138 U6

HCT244 U39

U40

U41

U3 NCTS8256

74AC573 U4

74AC573 U5

HC132 U9

HC14 U12

HC04 U10

11x10k

TO KEYBOARD

TO TRANSITION BOARD

NTURNON

TEST ENG PORT

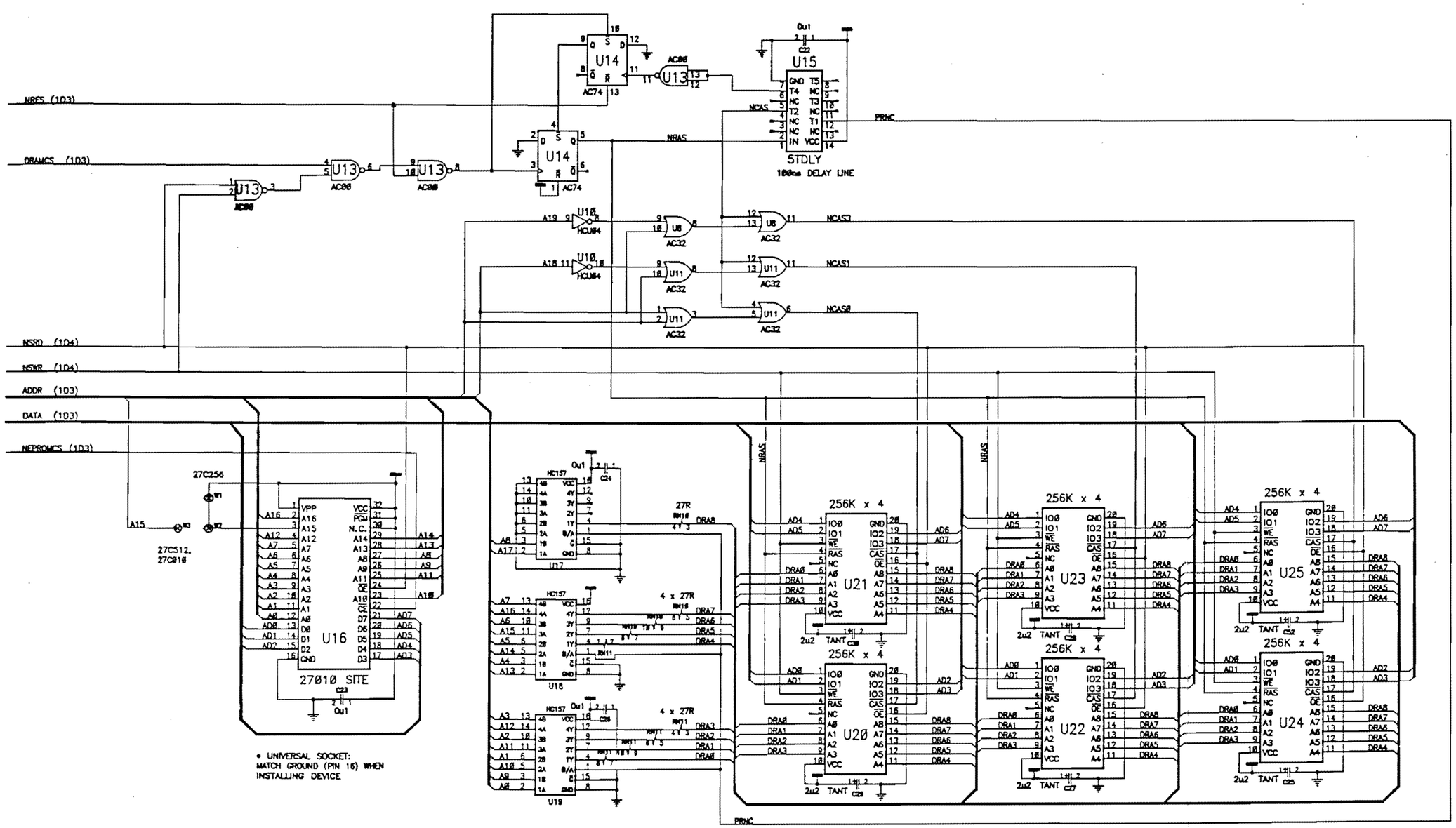
DSXCHG (4D3)
DR0Ø (4D3)
DR01 (5D2)
FDCINT (4D3)
S2XCLK (5D2)
SINT3 (5D2)
RDYNWT (5D2)
DS0 (4D3)
DS1 (4D3)
VSDDRDY (3D4)
NHSYNC (3D4)
NVSYNC (3D4)
INTENS (3D1)
VIDEO (3D1)

NEPROMCS	(2A3)
NA16VSDD	(3A3)
DRAMCS	(2A2)
DATA	(2A2),(3A3),(4A1),(5A2)
ADDR	(2A2),(3A3),(4A1),(5A1)
ALE	(3A3),(5A3)
SNPCS5	(5A4)
SNPCS4	(5A4)
H	(3A2)
V	(3A2)
NRES	(2A1),(5A3)
NDATAEN	(5A3)
NPCS2	(4A1)
MIO	(5A3)
RESET	(3A3),(4A2)
NSWR	(2A2),(3A3),(4A1),(5A2)
NSRD	(2A2),(3A3),(4A1),(5A2)
BACKPLANE SIGNAL BUS	(5A2)
NDRV1	(4A3)
NDRV0	(4A3)

MODEL 9448 (MPC)		DWG NO. 04-100270C	
DESC. CPU, KEYBOARD, AND PORT INTERFACE		REV -C	ISS: 3
SCALE NONE	SHT 1 OF 5	DRN P. HWANG	
CKD	APP.	DATE 10/13/88	Navtel

1328 C:3
ECO REV

REV	DESCRIPTION	DATE
C:3	U13 PIN 6.9.10 WAS CONNECTED TOGETHER.	Ø1 FEB 89



UNN LOWER BANK UPPER NIBBLE	UNN MIDDLE BANK UPPER NIBBLE	UNN UPPER BANK UPPER NIBBLE
UNN LOWER BANK LOWER NIBBLE	UNN MIDDLE BANK LOWER NIBBLE	UNN UPPER BANK LOWER NIBBLE

MODEL 9448 (MPC)		DWG NO. 04-100270C	
DESC. MEMORY SECTION OF MPC			REV -C ISS: 3
SCALE NONE	SHT 2 OF 5	DRN P. HWANG	Navtel
CKD	APP.	DATE 10/13/88	

REV	DESCRIPTION	DATE

INTENS (1A4)
VIDEO (1A4)

NOTES:
FOR TTL CRT:
DEFAULT
FOR RS-170:
SHORT W4-W5,W6-W7
CUT W7-W8,W9-W10
(EPLD NEEDS TO BE REPROGRAMMED)

W11-W12 FOR ALTERNATE
FUTURE CRTs

TO INTERNAL CRT

H (1D4)
V (1D4)
RESET (1D4)
NSWR (1D4)
NSRD (1D4)
ALE (1D4)
MA16VSDD (1D3)
ADDR (1D3)
DATA (1D3)

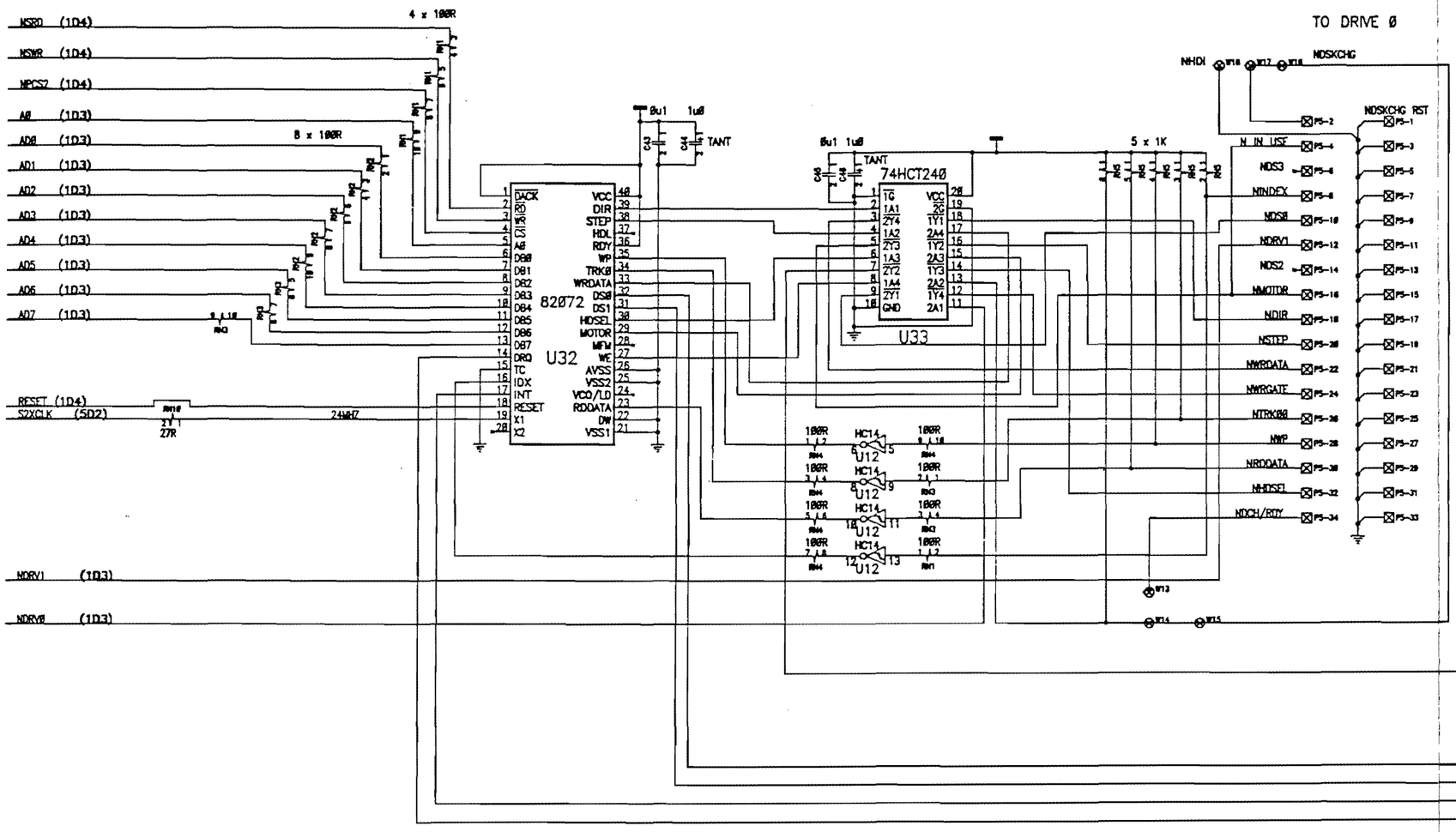
U26
82716

64K x 4 ZIP

VSDDRDY (1A4)
NHSYNC (1A4)
NVSYNC (1A4)

MODEL 9448 (MPC)		DWG NO. 04-100270C	
DESC. VIDEO SECTION OF MPC			REV -C ISS: 3
SCALE NONE	SHT 3 OF 5	DRN P. HWANG	Navtel
CKD	APP.	DATE 10/13/88	

REV	DESCRIPTION	DATE



CONNECTIONS FOR
SONY MP-F17W-50L:
DEFAULT
EPSON SMD-440L:
SHORT W13-W14, W17-W18
CUT W16-W17, W14-W15

MODEL 9440 (MPC)		DWG NO. 04-100270C	
DESC. FLOPPY DISK SECTION OF MPC			REV -C ISS: 3
SCALE NONE	SHT 4 OF 5	DRN P. HWANG	Navtel
CKD	APP.	DATE 10/13/88	

REV	DESCRIPTION	DATE

ADDR (1D3)

BACKPLANE SIGNAL BUS (1D3)

DATA (1D3)

NDATAEN (1D4)

MIO (1D4)

ALE (1D4)

NRES (1D4)

SNPCS4 (1D4)

SNPCS5 (1D4)

NDEN (1A2)

DTR (1A2)

NSRD (1D4)

NSWR (1D4)

NLOCK (1A2)

INT1 (1D4)

INT2 (1D4)

SNPCS4

SNPCS5

U34 74AC245

U35 74AC245

U36 74AC245

U37 74AC245

U38 74AC245

U16 HCU04

1MB

XTL1 24MHz

C1 22pF

C2 22pF

1K R26

4 x 18K

SDRQ1

SINT1

SINT2

SINT3

DRQ1 (1A1)

SINT3 (5D2)

S2XCLK (1A2),(4A2)

RDYNWT (1A4)

68 PIN CON

P7

4 PIN CON P6

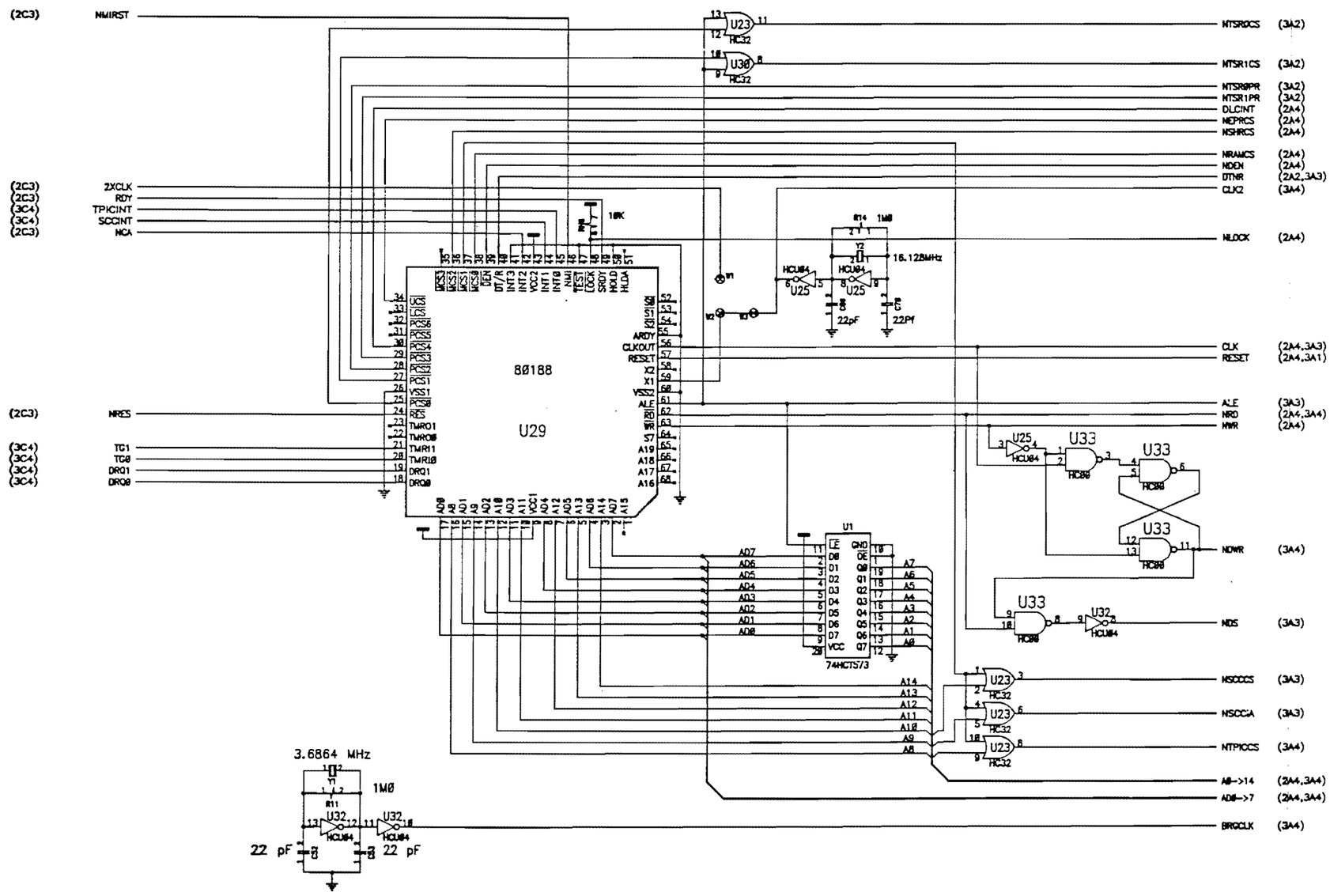
POWER SUPPLY CONNECTOR TO BASE UNIT POWER SUPPLY (0.100")

4 PIN CON P8

POWER SUPPLY CONNECTOR TO TURBO POWER SUPPLY (0.156")

MODEL 9440 (MPC)		DWG NO. 04-100270C	
DESC. CONNECTOR ON MPC (TO DLC)			REV -C ISS: 3
SCALE NONE	SHT 5 OF 5	DRN P. HWANG	Navtel
CKD	APP.	DATE 10/13/88	

REV	DESCRIPTION	DATE
D:3	NO CHANGE ON THIS DRAWING	14 DEC 88
D:4	CHANGE ONLY ON SHEET 2 OF 5.	03 JAN 89
E:5	CHANGE ONLY ON SHT. 3 & SHT. 4	17 JAN 89



NOTE:

FOR 8 MHz: SHORT W2 AND W3 (DEFAULT)
FOR 12 MHz: CUT W2 AND W3
SHORT W1 AND W2

CHANGE	REV	ISS
ECO 1356	E	5
ECO 1291	D	4
ECO 1275	D	3
ECO 1217	C	2

MODEL 9440		DWG NO. 04-100271C	
DESC. DLC MPU CORE			REV - E ISS: 5
SCALE NONE	SHT 1 OF 5	DRN PLICHOTA	Navtel
DES	APP.	DATE 11/10/88	

PCAD\04A00271

REV	DESCRIPTION	DATE
D:3	U20 PIN 11,12 CONNECTED TO GROUND.	14 DEC 88
D:4	U20 WAS GAL16V8	03 JAN 89

U12 74HCT245 — A14 A13 A12 A11 A10 A9 A8 → SHA14 SHA13 SHA12 SHA11 SHA10 SHA9 SHA8

U5 74HCT245 — A7 A6 A5 A4 A3 A2 A1 A0 → SHA7 SHA6 SHA5 SHA4 SHA3 SHA2 SHA1 SHA0

U2 74HCT245 — AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 → SHD7 SHD6 SHD5 SHD4 SHD3 SHD2 SHD1 SHD0

U11 62256 — SHA14 SHA13 SHA12 SHA11 SHA10 SHA9 SHA8 SHA7 SHA6 SHA5 SHA4 SHA3 SHA2 SHA1 SHA0 → SHD7 SHD6 SHD5 SHD4 SHD3 SHD2 SHD1 SHD0

U7 74AC245 — SHA14 SHA13 SHA12 SHA11 SHA10 SHA9 SHA8 → SA14 SA13 SA12 SA11 SA10 SA9 SA8

U6 74AC245 — SHA7 SHA6 SHA5 SHA4 SHA3 SHA2 SHA1 SHA0 → SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0

U3 74AC245 — SHD7 SHD6 SHD5 SHD4 SHD3 SHD2 SHD1 SHD0 → SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0

U13 74HCT245 — SD7 SD6 SD5 SD4 SD3 SD2 SD1 SD0 → SA7 SA6 SA5 SA4 SA3 SA2 SA1 SA0

U20 16CV8P-25 — VCC NBGTR NSHWR NSHRD NBGT1 ROYNWT NSHDWR DRDY IN CLK IN IN IN IN IN IN IN GND

U8 GAL16V8 — IN GND IN IN IN IN IN IN IN IN VCC CLK

SA10 SAT1 NWIRST NSALE13 SIR115 DLCINT NSWR MCA NSSBRQ

U17 AC74 — U35 AC08 — U30 HC32 — U25 HCU04

U10 27C256 — A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 → AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

U19 62256 — A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 → AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

NSSHRRQ NSLOCK NSHRCS NLOCK NRAMCS NEPRCS NRD NWR

100R R5

68 PIN CON — P2

SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 SA19 SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 NSDEN SDTNR NSRD NSWR SWNIO SALE S2XCLK ROYNWT NSLOCK NRES SDRQ SIR1 SIR2 SIR3 NPCS4 NPCS5 P12V P5V N12V GND

2XCLK (1A2) NRES (1A2) NCA (1A2) RD/ (1A2) NWIRST (1A1)

P5 GND TAB

DTNR (1C1)

(1C4) A8-->14
(1C4) AD8-->7
(1C1) NEPRCS
(1C2) NRD
(1C2) NWR
(1C1) NRAMCS
(1C1) NSHRCS
(1C1) DLCINT
(1C2) CLK
(1C2) NDEN
(1C2) RESET
(1C2) NLOCK

NOTES:
1) U35 SHOULD BE CHANGED TO A 74AC02 IN THE NEXT REVISION

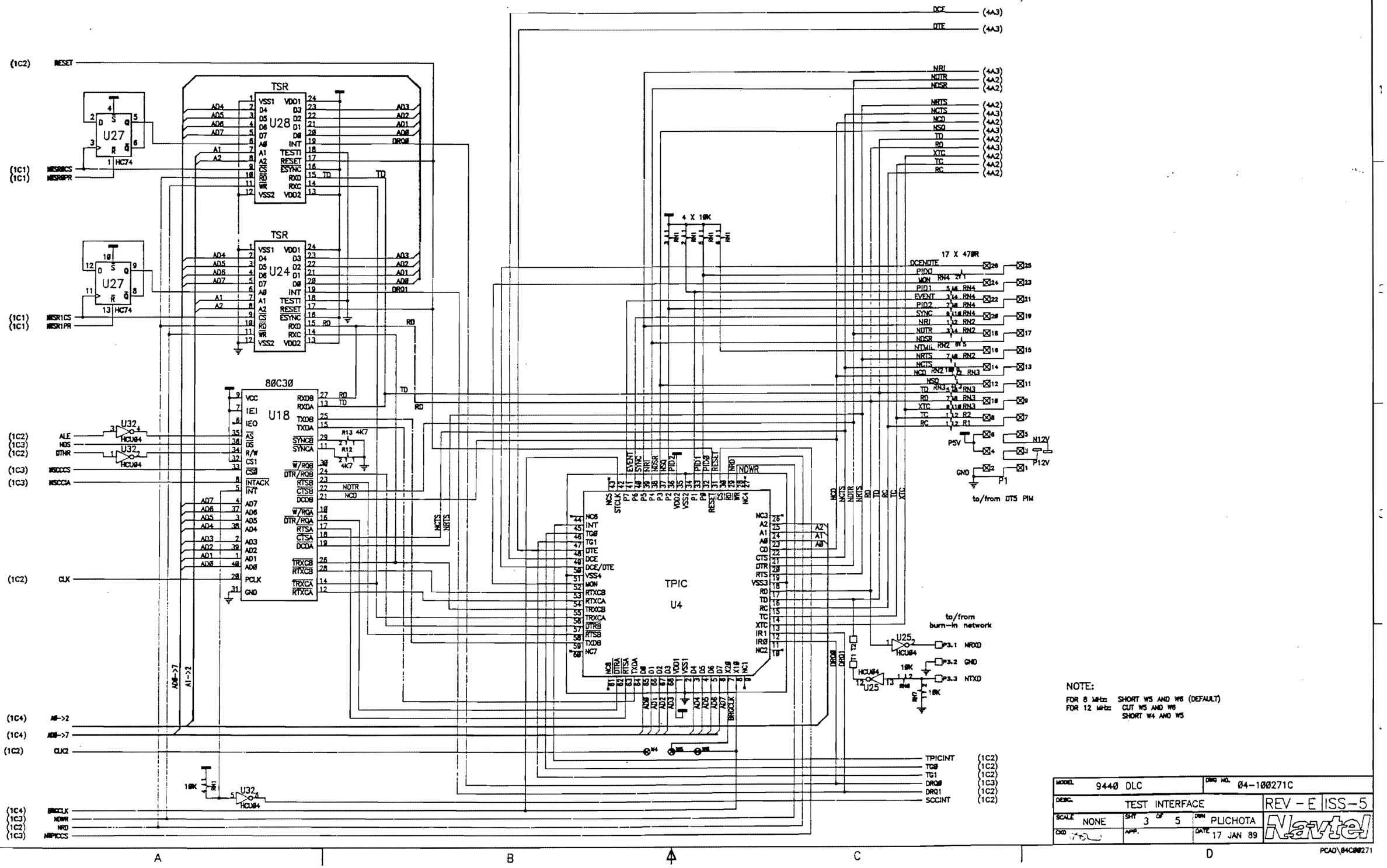
ECO 1504	E	5
ECO 1251	D	4
ECO 1175	D	3
ECO 1227	C	2
change	rev	iss

title: 9440 DLC RAM & MPC I/F
NAVTEL

board: NONE — draw: M.P.
proj: 9440 — check: — p. engr:
proj: F001 — dwg: 04-100271C
sht 2 of 5 — rev: E — iss: 5

PCAD\04100271

REV	ISS	DESCRIPTION	DATE
D	3	RN7 PIN 1&2 WAS 100K OHM. (ECO1275)	14 DEC 88
E	5	ADDED R12, R13 (4K7 Ohm). (ECO1318)	17 JAN 89



MODEL 9440 DLC		DWG NO. 04-100271C	
DESC. TEST INTERFACE		REV - E	ISS-5
SCALE NONE	SHT 3 OF 5	DRN PLICHOTA	Nortel
CKD	APP.	DATE 17 JAN 89	

PCAD\84C00271

REV.	ISS.	DESCRIPTION	DATE
D	3	REMOVED CAPACITORS C10,15,16,21-29. RN7 & RN8 WERE 10BK Ohm. U9 & U18 WERE 74HC14,	14 DEC 88
E	5	ADDED CAPACITORS C10,15,16,21-29. (ECO1319)	17 JAN 89

(3C1) TD
(3C1) NRTS
(3C1) NDTR
(3C1) XTC
(3C2) RC
(3C2) TC
(3C1) NCD
(3C1) NDSR
(3C1) NCTS
(3C1) RD
(3C1) NRI
(3C1) NSD
(3C1) DTE
(3C1) DCE

U21 1488 U26 1488 U31 1488 U34 1488 U14 HC125 U22 HC02 U15 74HC245

K1 K2 K3 K4 K5 K6 RBM RELAY

RXRTS RXSD RXDTC RXDTR TXTC TXRC TXDSR TXCD TXRD TXCTS TXSD TXRI TXDTR TXSD TXDTC TXDTR RXTC RXRC RXDSR RXCD RXRD RXCTS RXSD RXRI

P4.1 P4.2 P4.3 P4.4 P4.5 P4.6 P4.7 P4.8 P4.9 P4.10 P4.11 P4.12 P4.13 P4.14 P4.15 P4.16 P4.17 P4.18 P4.19 P4.20 P4.21 P4.22 P4.23 P4.24 P4.25 P4.26 P4.27 P4.28 P4.29 P4.30 P4.31 P4.32 P4.33 P4.34

P12V

EC01318	E	5	
EC01275	D	3	
EC01227	C	2	
change	rev	iss	

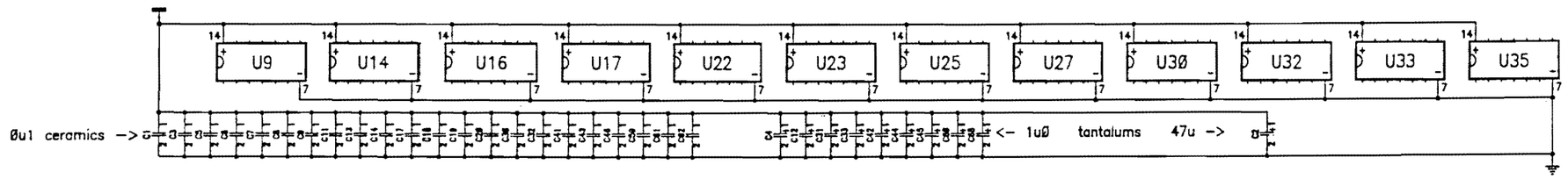
titles: TEST INTERFACE BUFFERS

Navtel

scales: NONE		drwn: M.P.	appvd:
proj: 9440		origin:	s. engr:
proj: F001		dwg: 04-100271C	
sht 4 of 5		rev: E	iss: 5

PCAD\8408271

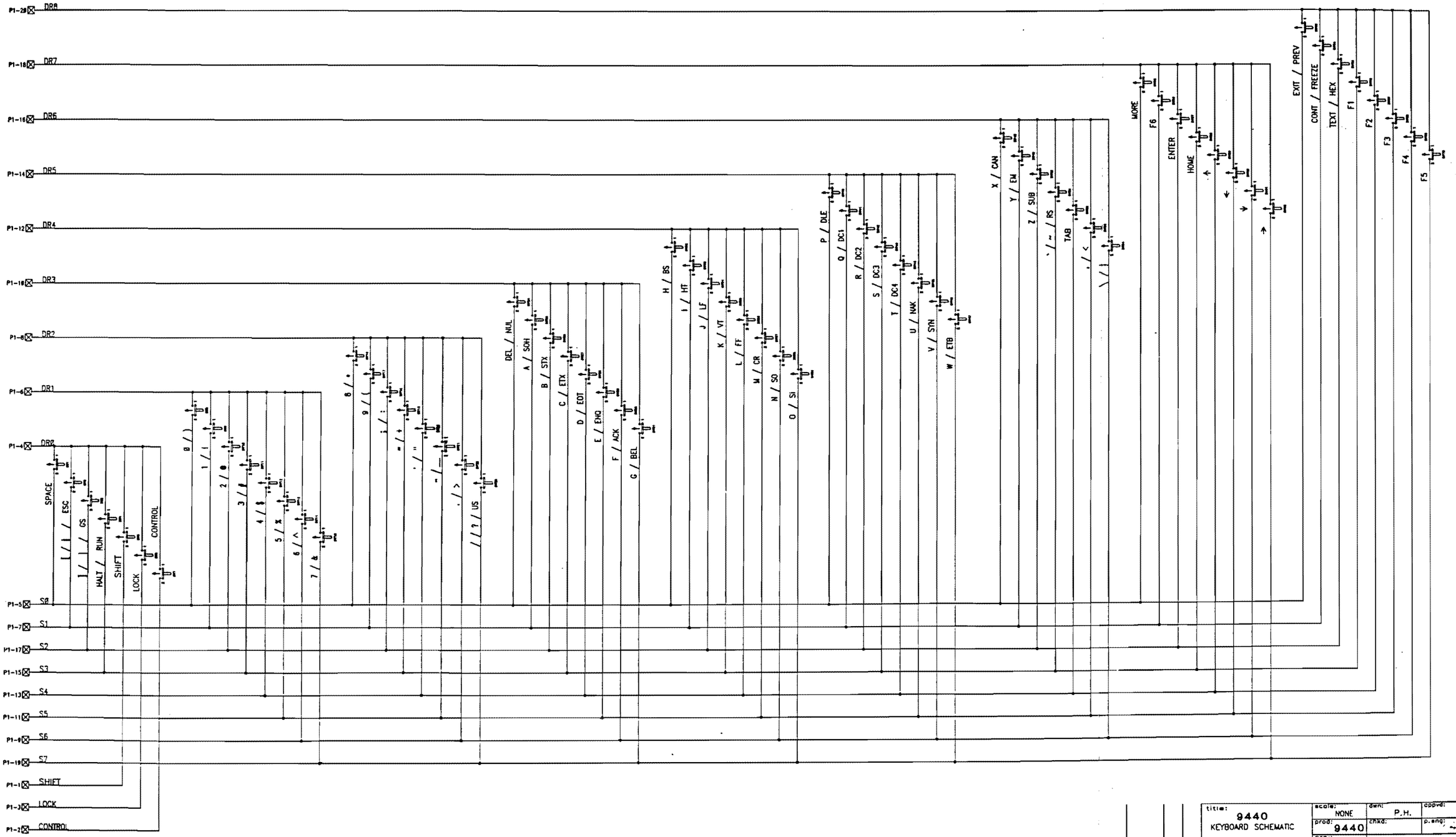
REV	DESCRIPTION	DATE
D:3	NO CHANGE ON THIS DRAWING.	14 DEC 88



ECO#310	E	5	title: PEGASUS DLC P/S & DECOPLING	assy: NONE	draw: M.P.
ECO#251	D	3		proj: 9440	chkd: PM
ECO#275	D	3	NAVTEL	proj: F001	dwg: 04-100271C
ECO#327	C	2		sht 5 of 5	rev: E
change	rev	iss			iss: 5

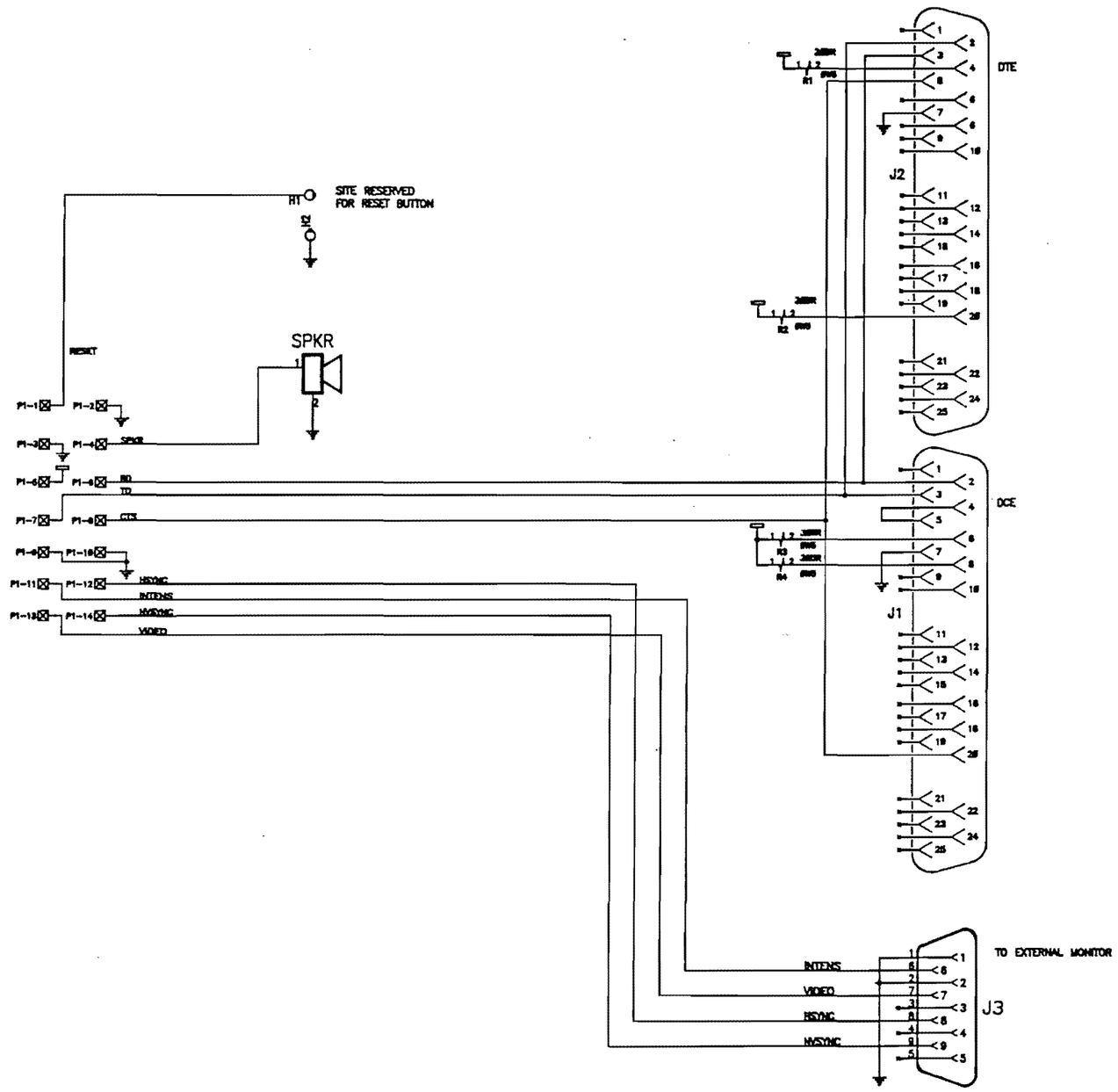
PCAD\04E00271

ISS.	DESCRIPTION	DATE
A:2	CHANGED TITLE NAME FROM "DT4" TO "9440"	09 FEB 83

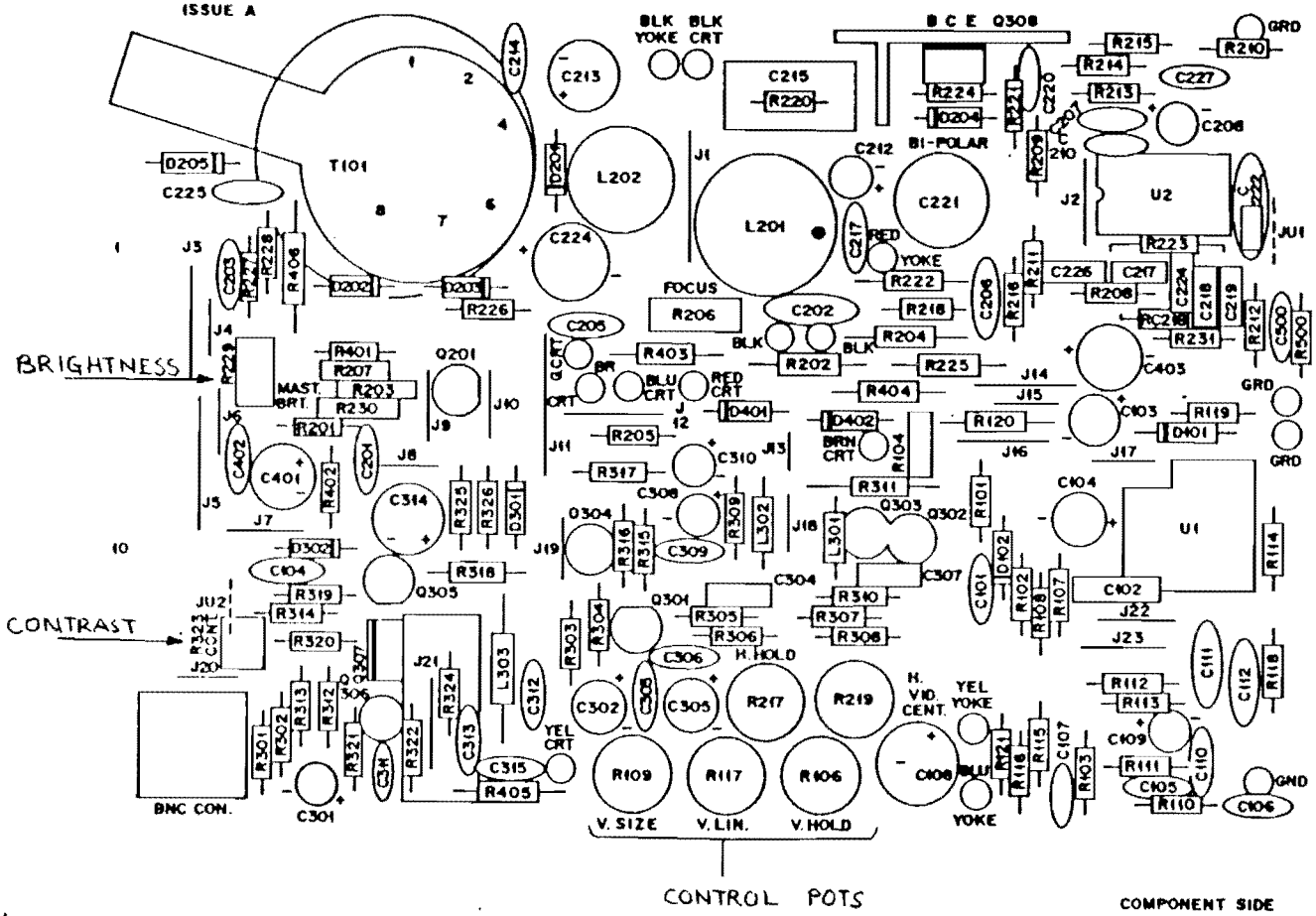


title: 9440 KEYBOARD SCHEMATIC		scale: NONE	dwn: P.H.	appvd:			
		prod: 9440	chkd:	p.eng:			
ECO 1185	A	1	proj: F001	dwg: 84-100272D			
change	rev	iss	sht 1 of 1	rev: A	iss: 2		

REV	DESCRIPTION	DATE



1185	A	1	title: 9448 TRANSITION BOARD	scale: NONE	date: P.H.	approved:	
change	rev	iss	NAVTEL	proj: 9440	drawn:	p. engr:	
				prod: 9448	dwg: 94-1882858		
				shtt 1 of 1	rev: A	iss: 1	



change	rev	lss	title: 5" CRT COMPONENT LEGEND	scale: N/A	dwn: Paul Soong	appvd:
				prod: 9440	chkd:	p.eng:
			Navtel	proj: F001	dwg: 35-100280A	
				sht of	rev:	lss: 5