AD-3524
AD-3525
FFT ANALYZER

MAINTENANCEMANUAL

maintenance-AD-3524/25-V.1.a-90/04/20

A&D Company, Limited

CONTENTS

CHAPTER 1 OVERVIEW

In order to carry out maintenance and calibration of the high-accuracy portable FFT analyzer, this maintenance manual describes its functionings, adjustment, and inspection as simply as possible for each board and an entire instrument. Maintenance procedures are described using the flow charts, centering around replacement of the board, so that you can see which board is defective.

Note : There are some high-voltage parts inside the FFT. Be fully careful when you touch inside.
When you noticed a trouble with the FFT during its operation, turn off power immediately.

CHAPTER 2 DESCRIPTION OF FUNCTIONINGS

2-1 Overall Functionings

2-1-1 Overall Functionings

An analog signal inputted to this instrumententers the A/D board PZ:2351 (new)/PZ:2066 (old), where it is converted into a 14-bit digital signal.

Converted data enters the main logic board PZ:2055 and is stored in the internal memory or optional memory board PZ:2060A/B.

The data stored in the memory is FFT-computed at the CPU or optional high-speed operation board PZ:2065 to create screen data.

The screen data is sent to the CRT control board PZ:2058 for storage.

This stored data is sent at a CRT timing to display it on the screen.

The screen data displayed on the CRT can be printed to the printer through the printer driver board PZ:2062 and printer extension board.

For setting of measuring conditions, etc., their data are inputted from the panel key board PZ:2056 and soft key board PZ:2057.

Panel setting data, A/D data, and screen display data can be stored in a floppy disk through the floppy disk controller board PZ:2063.

They can be also stored in a CMOS memory card.

All the software for this instrument is contained in the ROM board PZ:2059.

Power input from an AC line is converted into a DC voltage required for each board at the power board PZ:2067/2068.

The SG board PZ:2046 converts computed data into analog data through a D/A converter for output.

2-3 Functionings of Each Board

2-3-1 A/D Board PZ:2066

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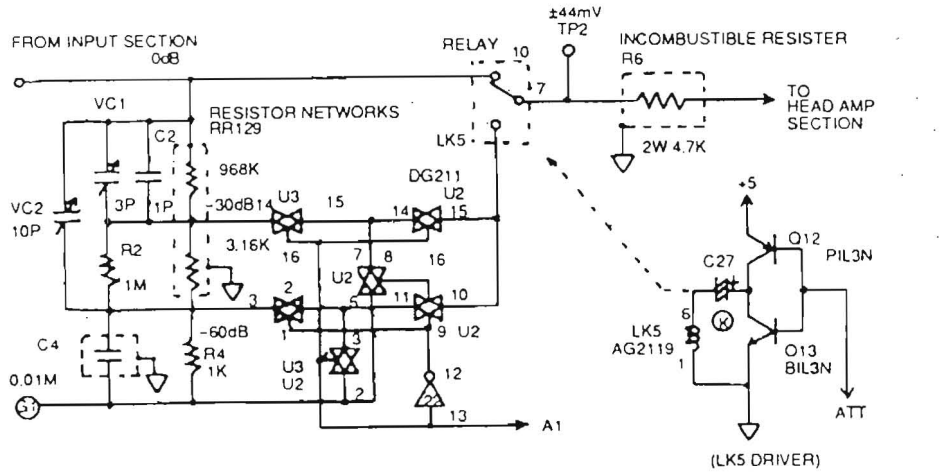
1. Outline

This board largely consists of a block which processes an analog input signal and attenuates (or amplifies) it to the input level of an A/D converter, filter (anti-aliasing filter) which removes frequency components outside the band of the signal, analog OVER detector which informs that an excessive input single has been applied, controller which control these front-end circuits, and A/D converter which finally digitalize the analog input signal to output it as digital data.

4. Attenuator Circuit



This circuit is designed to attenuate an input signal to within the input range of the head amplifier (max. 44mV). It attenuates the input signal to 0dB, -30dB, and -60dB by the relay K5 and analog switches U2 and U3.

The variable trimmers VC1 and VC3 are to compensate a change of frequency characteristic at the attenuator circuit ; VC1 makes compensation for ATT-30dB (input sense : 0 to -20dB), and VC2 makes compensation for ATT-60dB (input sense : +30 to +10dB).

R6 is a nonflammable fuse resistor and protects internal circuits against excessive input.

The table on the next page shows degrees of attenuation by a combination of control signals ATT and AI.

Table 1

SENSE RANGE	CONTROL		TOTAL ATTENUATION
	ATT	AI	
+30dB	1	1	-60dB
+20dB	1	1	-60dB
+10dB	1	1	-60dB
0dB	1	0	-30dB
-10dB	1	0	-30dB
-20dB	1	0	-30dB
-30dB	0	0	0dB
-40dB	0	0	0dB
-50dB	0	0	0dB
-60dB	0	0	0dB

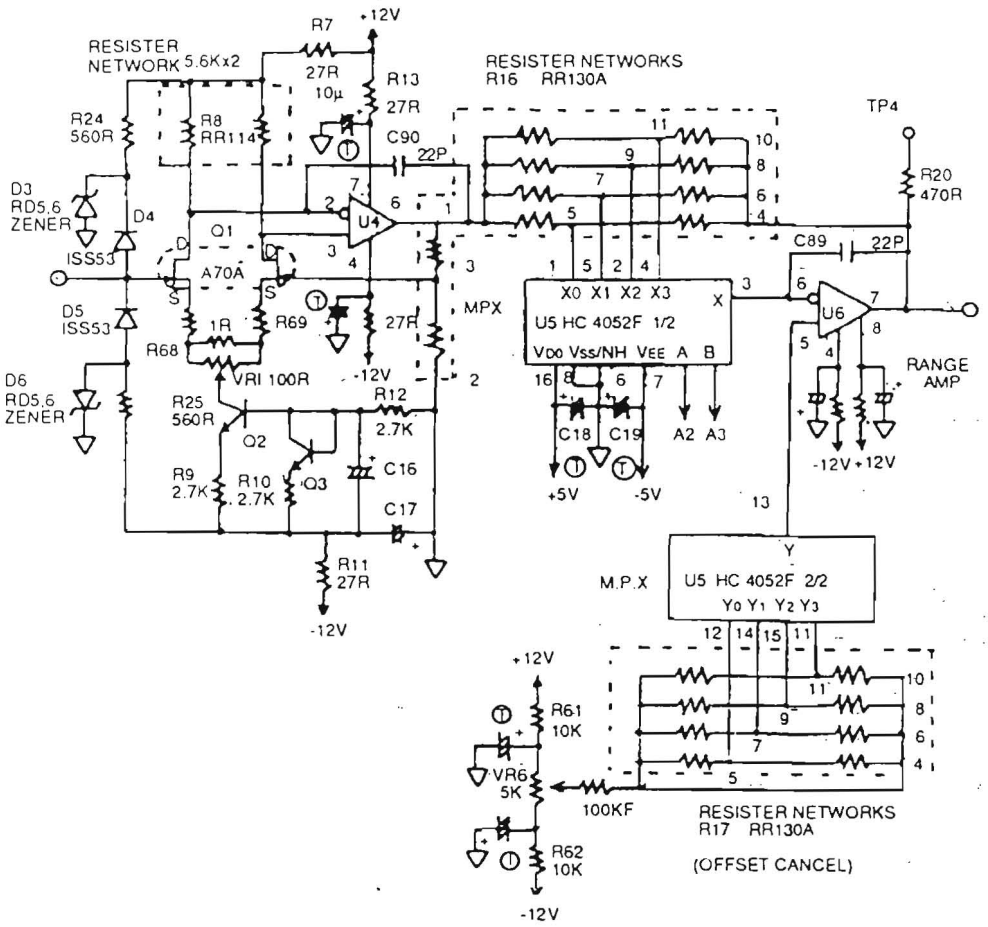
-30dB for ATT "1"
0dB for ATT "0"

Change over
by the relay LK5

-60dB for AI "1"
-30dB for AI "0"

Change over
by the analog switches U2 and U3

5. Head Amplifier and Range Amplifier Section



These circuits amplify (or attenuate) the signal attenuated by the attenuator to an appropriate signal level (±0.224V).

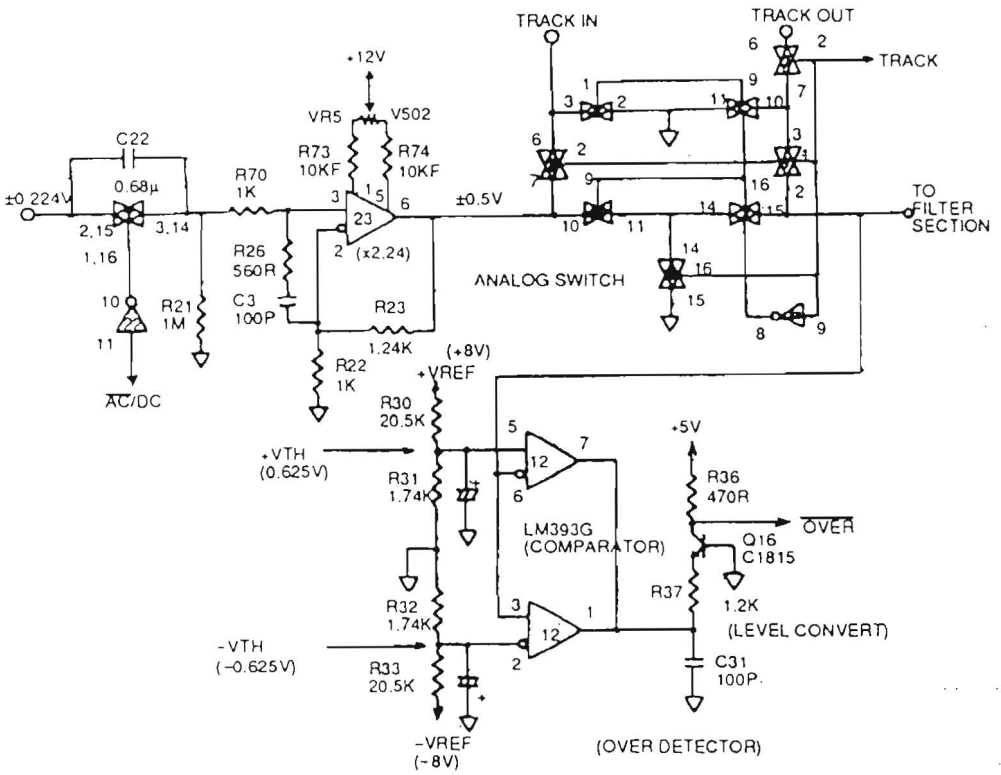
The head amplifier (U4) has its amplification factor fixed at +30dB, and the range amplifier (U5, 6) is a programmable gain amplifier.

The table for the range amplifier is shown on the next page.

SENSE RANGE	CONTROL		AMPLIFIER
	A2	A3	
+30dB	1	1	-16dB
+20dB	0	1	-6dB
+10dB	1	0	+4dB
0dB	1	1	-16dB
-10dB	0	1	-6dB
-20dB	1	0	+4dB
-30dB	1	1	-16dB
-40dB	0	1	-6dB
-50dB	1	0	+4dB
-60dB	0	0	+14dB

The circuit connected to the non-inverting terminal of U6 is to override the offset caused by the input bias current of U6.

6. OVER Detector Circuit



This circuit changes over AC/AD coupling after the range amplifier, provides a connection to the option-09 (tracking card), and makes OVER detection.

With a reference voltage (±Vref) given from the A/D module, the OVER detector circuit generates a threshold voltage VTH for the analog comparator.

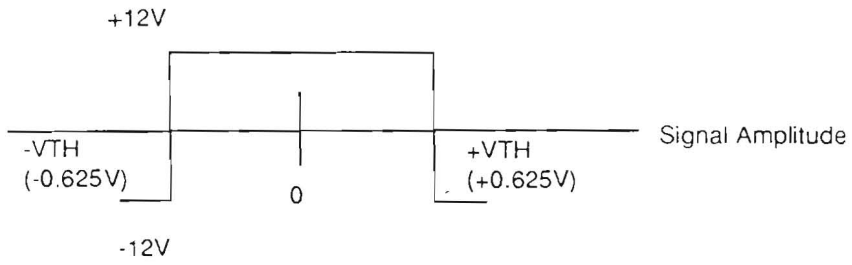
The threshold voltage has been set to ±0.625 which is 125% larger than the maximum voltage of ±0.5V here. (Amplification of the amplifier U23 is 2.24 times, where ±0.224V changed to ±0.5V)

When signal amplitude is within a range of ±VTH, comparator output is High (+12V). When exceeding ±VTH, however, it is Low (−12V).

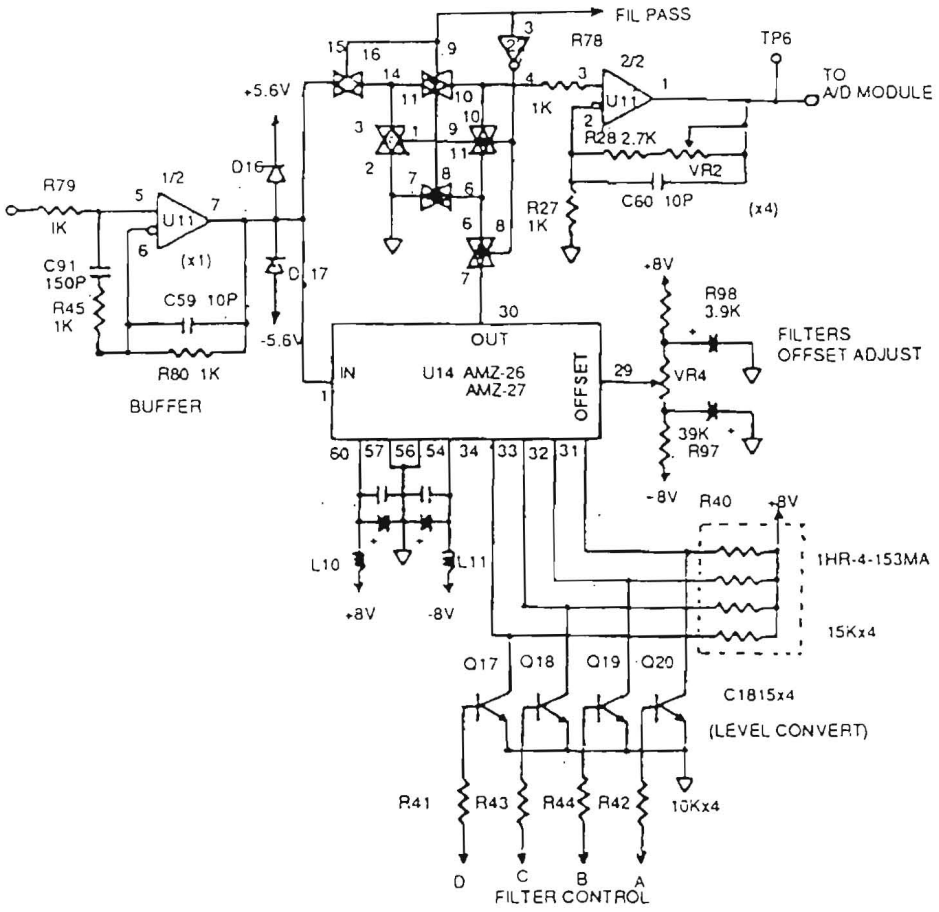
In this state, however, it is not available as a logic signal.

Therefore, the following circuit (Q6) converts it to the TTL level for output.

Comparator Output Compared with Input Signal Amplitude



7. Filter Circuit



This circuit turns on/of the anti-aliasing filter. The filter module used has an octonary simultaneous Chevishev characteristics. With a 4-bit control signal, it changes over a 10-point cut-off frequency between 100k and 100Hz for AMZ-27 (AAD11900) and 20k-20Hz for AMZ-26 (AAD12009) in 1-2-5 sequence, respectively.

The filter is turned on/off by the analog switches U9 and U10; the filter is off when FILTPASS = 1, and is on when it is 0.

The 2/2 of U11 is an amplifier to adjust analog signal amplitude to the full scale of the A/D module; its gain is about 4-fold.

(finely adjustment by VR2) Signal amplitude of ±0.5V is turned to ±2V here and outputted to A/D module.

The offset of the filter module is adjusted by VR4.

Relations between Input Sense Ranges and Respective Sections.

SENSE RANGE	ATT SECTION	BUFFER AMP SECTION	RANGE AMP SECTION	FUNCTION FILTER SECTION	TOTAL GAIN
+30dB	-60dB	+30dB	-16dB	+19dB	-27dB
+20dB	-60dB	+30dB	-6dB	+19dB	-17dB
+10dB	-60dB	+30dB	+4dB	+19dB	-7dB
0dB	-30dB	+30dB	-16dB	+19dB	+3dB
-10dB	-30dB	+30dB	-6dB	+19dB	+13dB
-20dB	-30dB	+30dB	+4dB	+19dB	+23dB
-30dB	0dB	+30dB	-16dB	+19dB	+33dB
-40dB	0dB	+30dB	-6dB	+19dB	+43dB
-50dB	0dB	+30dB	-4dB	+19dB	+53dB
-60dB	0dB	+30dB	+14dB	+19dB	+63dB

The total gain as far as the A/D section is +3dB at the sensoe range of 0dB. This is to adjust to FS (= ±2V) of the A/D module.

For A/D input, it is ±2V (+3dB) at ±1.411V input time. This is for the basic sense range of 0dB. In other sense ranges, the amplification factor changes in an increment (decrement) of +10dB (-10dB) against +3dB.

PIN CONNECTION

PIN NO		PIN NO	
1	INPUT	60	+8V
2	GND	59	N.C
3	N.C	58	N.C
4	N.C	57	GND
5	N.C	56	GND
6	N.C	55	N.C
7	N.C	54	-8V
8	N.C	53	GND
9	GND	52	N.C
10	N.C	51	N.C
11	N.C	50	N.C
12	N.C	49	N.C
13	N.C	48	N.C
14	N.C	47	N.C
15	N.C	46	GND
16	N.C	45	N.C
17	GND	44	N.C
18	N.C	43	N.C
19	N.C	42	N.C
20	N.C	41	N.C
21	N.C	40	N.C
22	N.C	39	N.C
23	N.C	38	GND
24	GND	37	N.C
25	N.C	36	N.C
26	N.C	35	N.C
27	N.C	34	D
28	N.C	33	C CONT
29	OFFSET ADJ	32	B
30	OUTPUT	31	A

Filter Module Control

Logic Binary Code Negative Logic "1" : øV (GND)
"ø" : 8V or OPEN

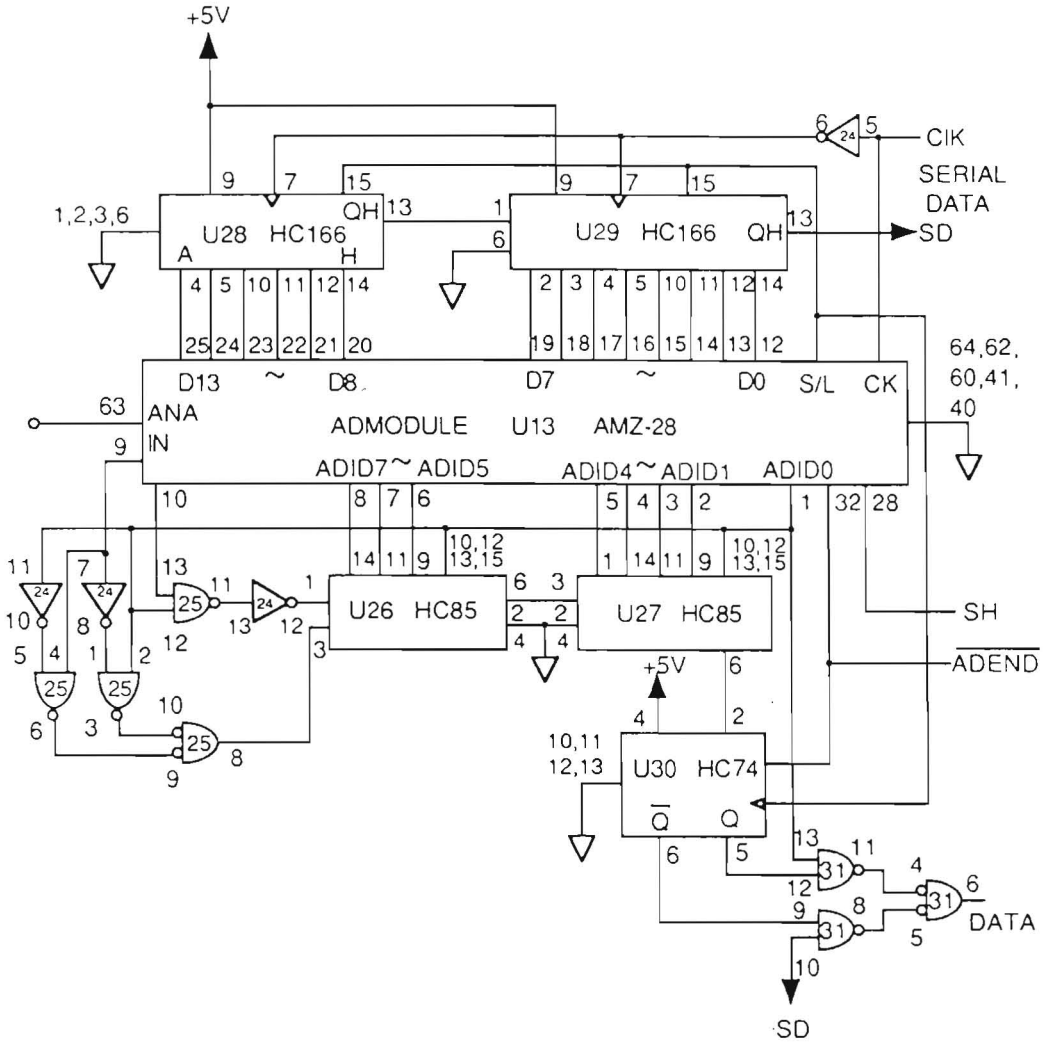
AMZ-27

FC	Control D C B A
100KHz	0 1 0 0
50KHz	0 1 0 1
20KHz	0 1 1 0
10KHz	0 1 1 1
5KHz	1 0 0 0
2KHz	1 0 0 1
1KHz	1 0 1 0
500Hz	1 0 1 1
200Hz	1 1 0 0
100Hz	1 1 0 1

AMZ-26

FC	Control D C B A
20KHz	0 1 0 0
10KHz	0 1 0 1
5KHz	0 1 1 0
2KHz	0 1 1 1
1KHz	1 0 0 0
500Hz	1 0 0 1
200Hz	1 0 1 0
100Hz	1 0 1 1
50Hz	1 1 0 0
20Hz	1 1 0 1

8. A/D Module



This circuit converts an analog signal into a digital signal to output data. U13 is an A/D converter and its peripheral circuit prevents A/D data from being returned when it overflows.

Details are described later.

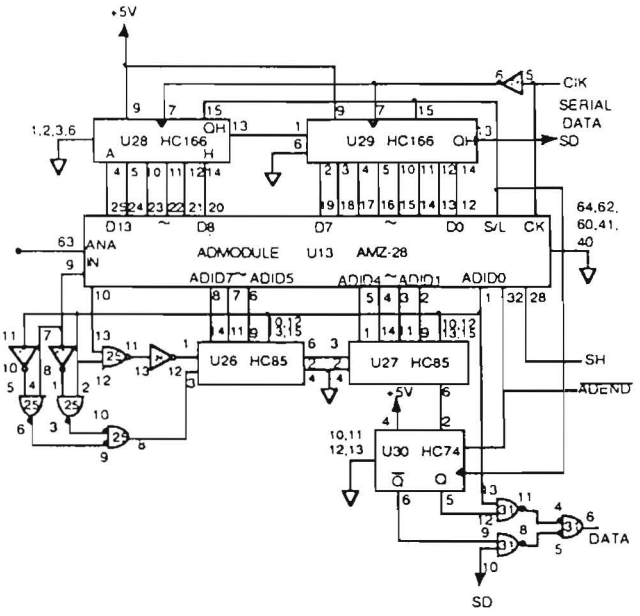
Pin Layout of A/D Module

PIN NO	LOGIC SIDE	PIN NO	ANALOG SID
1	AD1D0	64	A.GND
2	AD1D1	63	ANA-IN
3	AD1D2	62	A.GND
4	AD1D3	61	OFFSET
5	AD1D4	60	A.GND
6	AD1D5	59	N.C
7	AD1D6	58	N.C
8	AD1D7	57	N.C
9	AD2D0	56	N.C
10	AD2D1	55	N.C
11	S/L	54	N.C
12	D0 (MSB)	53	N.C
13	D1	52	N.C
14	D2	51	N.C
15	D3	50	N.C
16	D4	49	N.C
17	D5	48	N.C
18	D6	47	N.C
19	D7	46	N.C
20	D8	45	-REF
21	D9	44	N.C
22	D10	43	+REF
23	D11	42	N.C
24	D12	41	A.GND
25	D13 (LSB)	40	A.GND
26	DATA STROBE	39	N.C
27	N.C	38	+12V
28	S/H	37	N.C
29	N.C	36	+5V
30	CLK	35	N.C
31	N.C	34	-12V
32	A/DEND	33	N.C

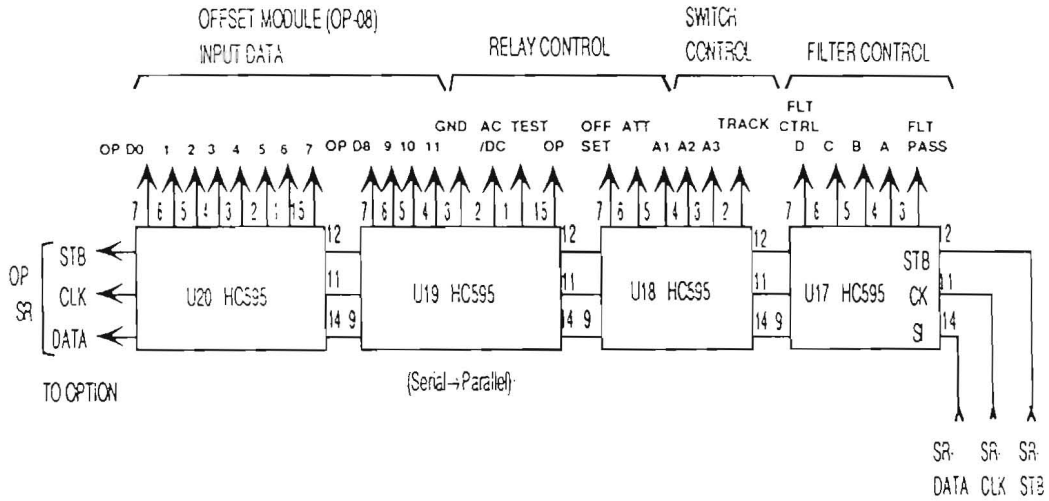
A/D Module Signal Names

- AD1D0-D7
  1st A/D conversion data internal to the module
- AD2D0, D1
  Upper 2 bits of the 2nd A/D conversion data internal to the module
- S/L
  Timing signal to convert A/D conversion data from parallel to serial
- D0-D13
  14bit A/D conversion data (parallel)
- DATA STROBE
  STROBE signal for 14bit A/D conversion data (parallel)
- S/H
  CLK signal given to the sampling/holding circuit inside the module
- ADCLK
  CLK signal given to the timing generator inside the modle
- ADEND
  Timing signal when externally conversion A/D conversion data from parallel to serial
- -12V, +5V, +12V
  Power source used inside the module
- +REF, -REF
  Gives the reference voltage of ±8V to the comparator of the OVER detector circuit of the analog board.
- OFFSET
  Terminal to give offset to the module
- ANA-IN
  Analog input for the module; FS = ±2V

A/D Data Aliasing Detection Circuit



A/D Board Control Circuit



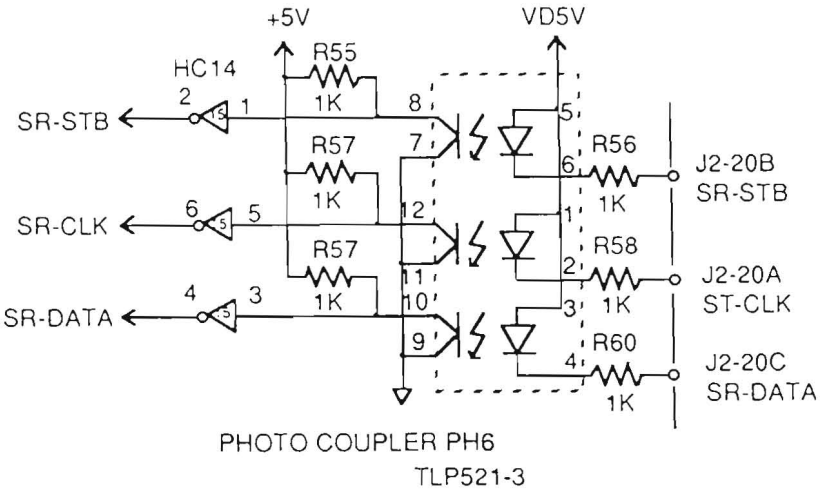
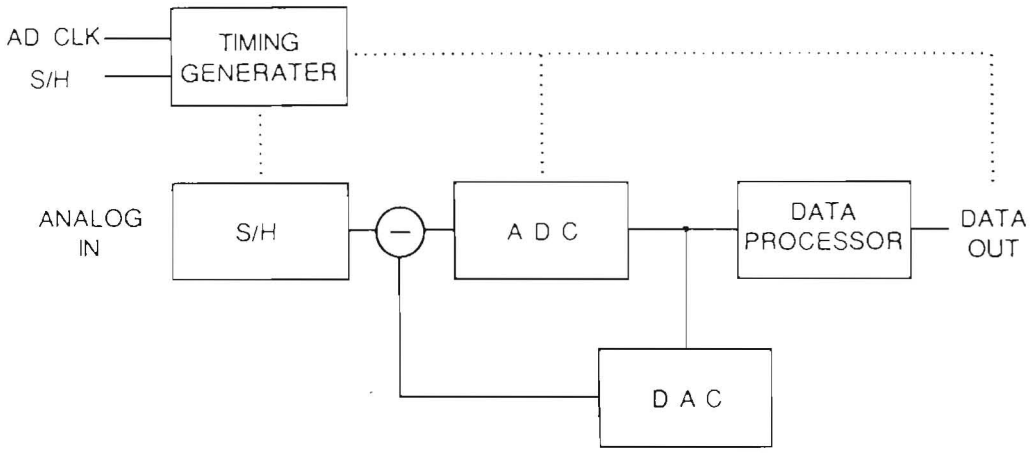
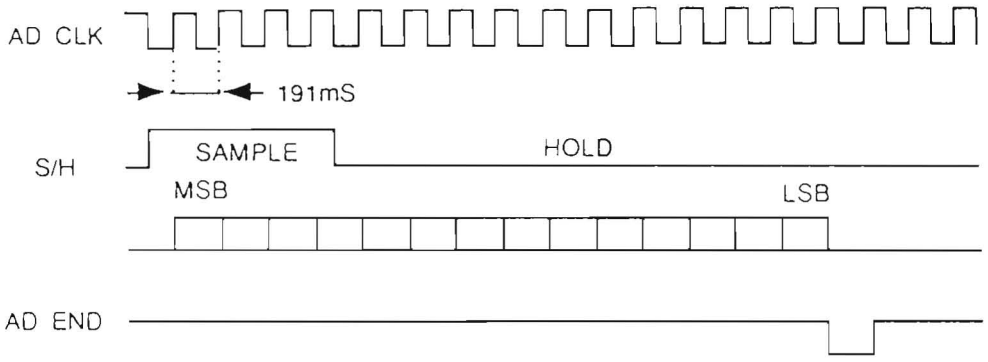


PHOTO COUPLER PH6
TLP521-3

A/D Module Block Diagram



A/D Module Timing Chart



9. A/D Board Control Data

Serial data is 40 bits (5 bytes).
A transfer order os common for both A and B channels

OP-08 OFSET MODULE
INPUT DATA (12bit)

ANALOG OPTION DATA
OP-10, TRACKING FILTER CARD
12, ENVELOPE CONVERSER CARD
11, CONDENSOR MICROPHONE CARD
16, SENSOR POWER CARD
etc.

Transfer Direction ↓

SIGNAL	PI.NO
DONT CARE	ø
	1
	2
FILPAS	3
FIL, 1	4
FIL, 2	5
FIL, 3	6
FIL, 4	7
	8
	9
TRACK	10
A3	11
A2	12
A1	13
ATT	14
OFFSET	15
OP	16
TEST	17
ACIDC	18
GND	19
OP D11	20
10	21
9	22
8	23
7	24
6	25
5	26
4	27
3	28
2	29
1	30
ø	31
OP, 7	32
6	33
5	34
4	35
3	36
2	37
1	38
ø	39

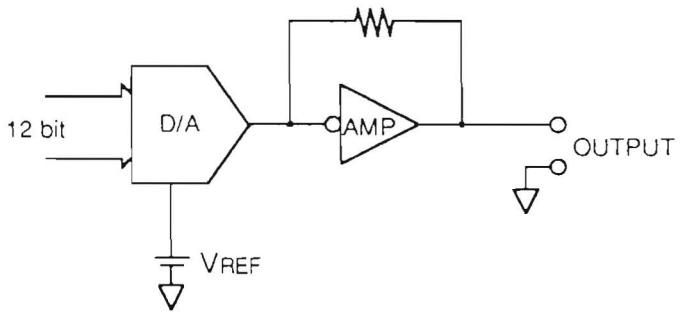
2-3-2 Offset Module (AMZ-29)

This module is a programmable DC generator. When it is attached to the analog board of the main body, it gives an offset voltage to signal source GND. It is a standard attachment for the 100kHz type, and optional one for the 20kHz type.

The output voltage of this module is ±150mV (maximum). The module receives 12bit data and performs D/A conversion inside for out put.

An input data format is offset binary.

LSB LSB	Output Voltage
1111~1	+150mV (+FS)
1øøø~1	+1LSB
1øøø~ø	0V
ø111~1	-1LSB
øøøø~ø	-150mV (-FS)



2-3-3 Main Logic Board PZ:2055

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2. CPU Section

The CPU of this instrument is the 16bit CPU HD68HC000-10 made by Hitachi. It uses 10MHz clock.

All the hardware of this instrument is controlled by this CPU.

Except that the DMAC serves as the bus master at sampling time, it always exists as the BUS master and one CPU takes care of measurement, computation, display, and control.

A CPU clock is input to the CPU at 10MHz by frequency-dividing the output from an quartz oscillator (source oscillation: 40.000MHz).

All the other ICs in the logic section, which require the clock, use the frequency-divided output of this oscillator. However, the sampling system uses the clock of another oscillation source.

The reset circuit has power-on reset and instantaneous stop detecting functions. It outputs a reset pulse of about 200ms at reset time.

Reset output uses the MB3771 made by Fujitsu.

The interrupt circuit has interrupt input with level 7-1 priority and is connected to the interrupt terminal of the CPU through the 8-3 encoder circuit.

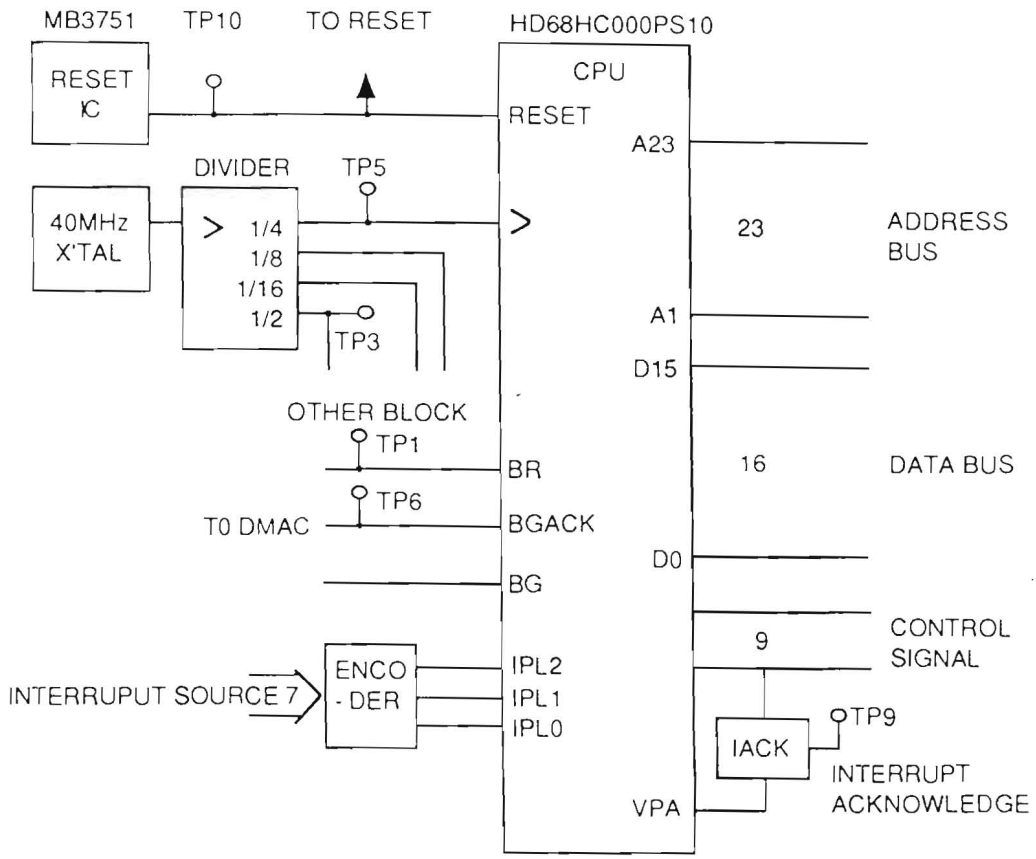
Interrupt priority is as follows:

Priority	Interrupt Source	Meaning	Interrupt Service
7	PFAIL	Signal to be output when the power starts dropping	Auto
6	DMAC	Interrupt signal from the DMA controller	Vector
5	ACRTC	Interrupt signal from the CRT controller	Auto
4	TIMER	Interrupt signal from the timer	Auto
3	KEY	Interrupt signal from key input	Auto
2	GP-IB	Interrupt signal from the GP-IB	Auto
1	FDC	Interrupt signal from the floppy disk	Auto

As shown in Fig. 1 Block Diagram, the logic structure of this instrument directly connects each circuit block via the CPU bus and accesses each circuit as a CPU bus device to control them. Therefore, the bus control line control signals from the CPU are connected to each circuit.

The interrupt acknowledge circuit informs the CPU of responding in the auto vector mode because all the interrupt sources except DMAC are in the auto vector mode.

Fig. 2 CPU Block Diagram



Test Point	Name	Function
1	BR	Low when the DMAC is requesting for A/D data transfer
3	20MHz	20MHz rectangular wave
5	CPUCLK	10MHz rectangular wave
6	BGACK	Bus busy status for the bus slave
9	IACK	Interrupt response signal
10	RES	Reset signal

3. DMAC Section

Since this instrument should transfer various data at a high speed, data transfer is realized by direct memory access through hardware instead of the CPU.

DMA is performed by the DMAC and HD63450PS10 which are the peripheral ICs of the HD68HCOOO series.

The DMAC operates by 10MHz clock synchronized with CPU clock and is directly connected to the CPU bus.

The DMAC incorporates 4 DMA channels, each of which takes care of the following data transfer:

CH0	Pre-trigger sample A/D data transfer
CH1	Post-trigger sample A/D data transfer
CH2	GP-IB data transfer
CH3	FDC data transfer or ACRTC data transfer

Note: The following description takes CH0 of the DMAC as an example.

A/D-converted input data enters the sample controller and a data transfer request is sent from the sample controller to the DMAC.

The DMAC issues a bus request (BR) to the CPU, and when it acquired the CPU bus, it controls the bus in place of the bus master and (D) CPU.

The DMAC, which has acquired the bus, starts a memory read cycle and transfers data from the sample controller to the DMAC internal buffer.

The DMAC starts the next memory write cycle and transfers data from the DMAC internal buffer to the buffer memory.

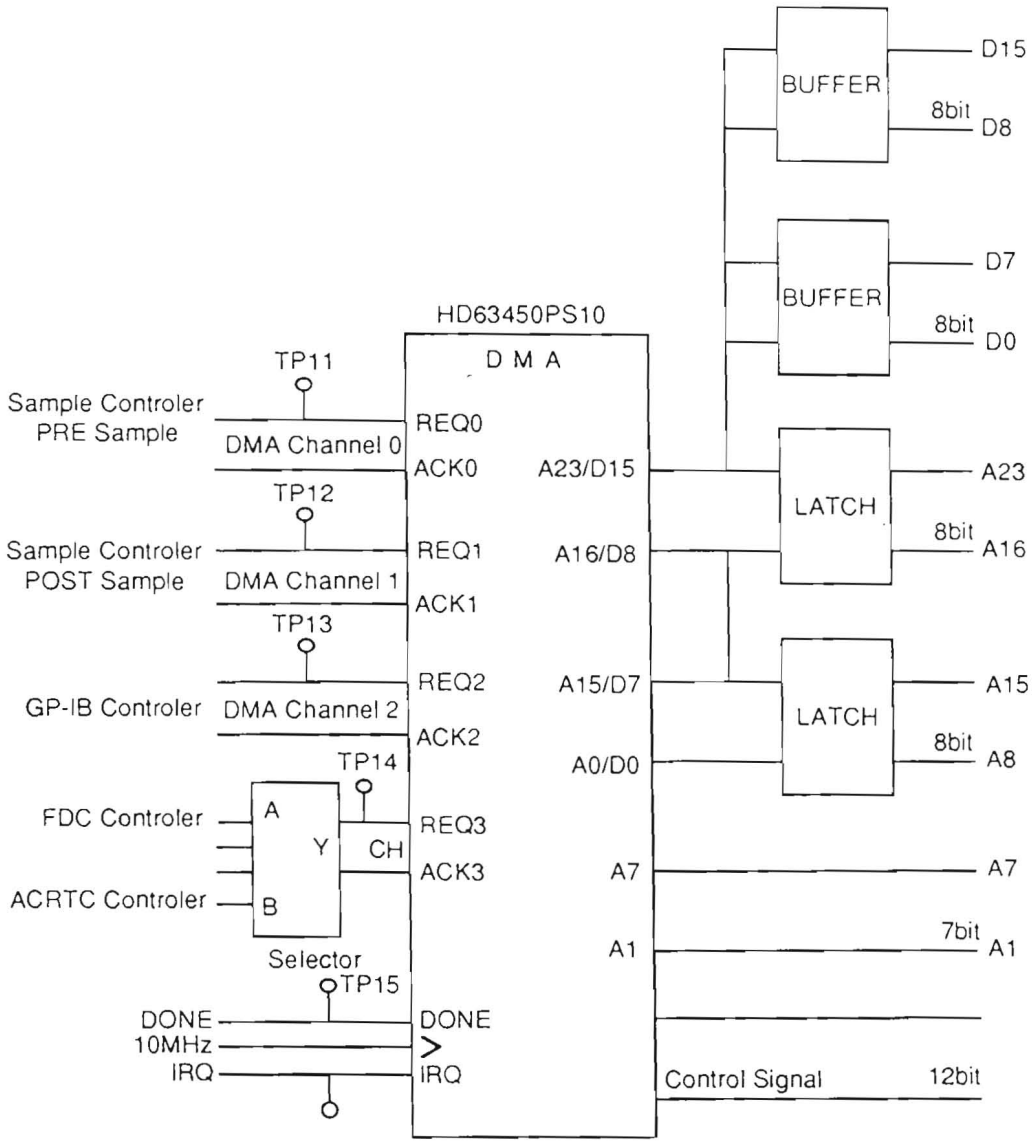
After transferring data from the sample controller to the memory, the DMAC opens the bus to the CPU.

The DMAC performs data transfer in a dual address, cycle steal mode.

Since the DMAC bus is an address-data multiplex bus, the buffer of the DMAC section is used for its seperation.

Only CH3 allows you to select either FDC or ACRTC as a DMA device; a selector has been inserted into the REQ line for that purpose.

Fig. 3 DMAC Section



Test Point No.	Name	Function
11	REQ0	Pre-sample data transfer request signal
12	REQ1	Post-sample data transfer request signal
13	REQ2	Data transfer request signal from the GP-IB
14	REQ3	Data transfer request signal from the FDC
15	DONE	DMA channel operation complete signal
16	IRQ	Service request signal from the DMAC to CPU

4. Address Decoding Section

The address decoding section determines a device's physical address on the CPU memory, accesses the device, and creates a device response signal to the CPU.

Since all the devices are connected on the CPU bus, each of them occupies its independent specific memory area in the CPU memory.

The address decode IC (D65006GF) decodes an encoded CPU address signal to generate a CS (Chip Select) signal. The CS signal is connected to the CS terminal of each device and an arbitrary device is accessed.

Since the CPU bus is asynchronous, it is necessary to return a response signal (DTACK) to the CPU when the device is accessed. This signal is also generated by this section.

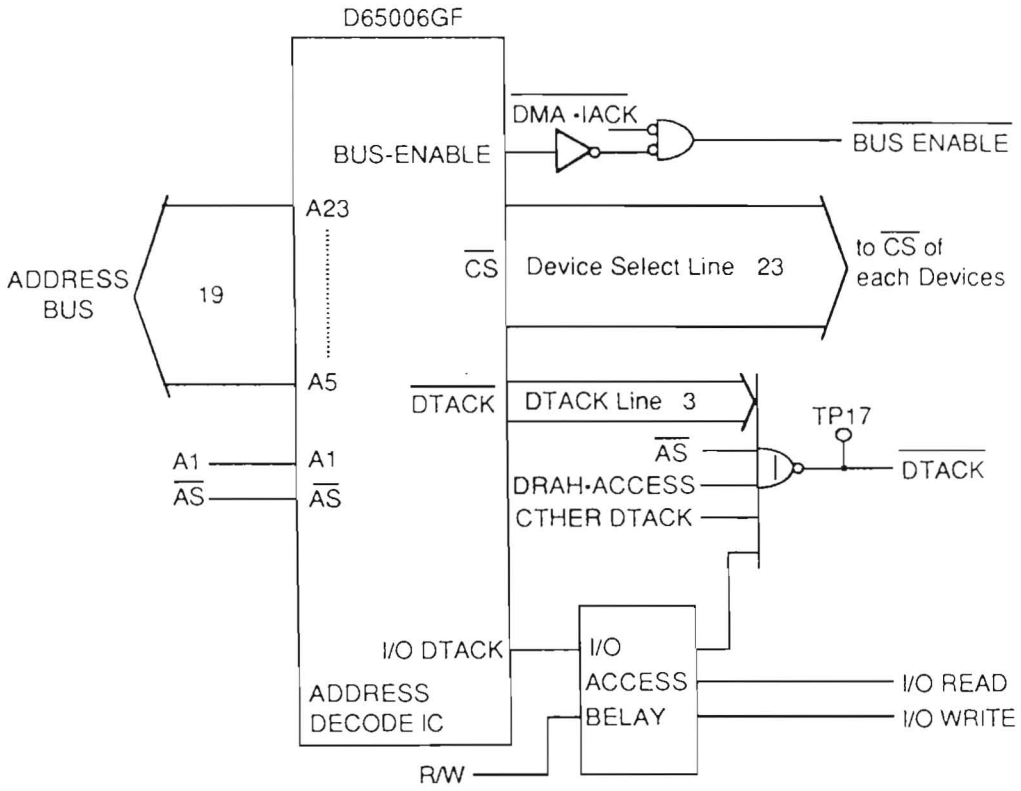
As the I/O devices have a slow access speed, a wait is inserted into the CPU bus cycle. The moment the wait is generated, the I/O access delay circuit generates I/O READ and WRITE signals.

A BUS ENABLE single is used for controlling the buffer of the mother board section; when BUS ENABLE is active, data input/output is done from outside the buffer.

For the memory map and I/O map, refer to Appendixes.

Also, as the BUS ENABLE signal is turned inactive in the DMA IACK cycle, the vector for vector interrupt cannot be generated from outside the bus.

Fig. 4 Address Decoding Section



Test Point No.	Name	Function
17	DTACK	Access Response Signal from Device to CPU

5. Calibration Section

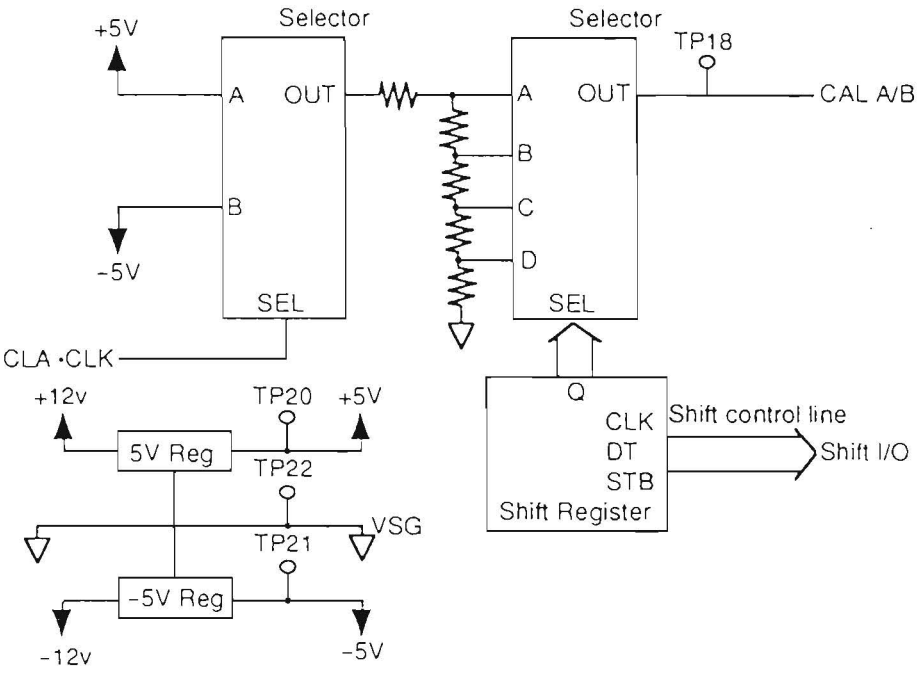
This instrument incorporates a test signal generator circuit for accuracy calibration of the measuring system of the analog block.

The calibration circuit outputs a frequency signal which allows 8 wavelengths of rectangular wave with 1 : 1 duty in the A/D data sample frame.

An output voltage can be selected at 7 levels by changing the attenuator level in accordance with setting from the shift register.

CAL A/B output is connected to the input section of the Ach analog board and Bch analog board via the mother board and is inputted to A/D by changing over the input relay of the analog board.

Fig. 5 Calibration Section



Test Point No.	Name	Function
18	CAL-OUT	Analog calibration signal output
20	+VCAL	+5V for calibration signal
21	-VCAL	-5V for calibration signal
22	VSG	Ground

6. Memory Section

This instrument has 512KW DRAM and 32KW SRAM as standard memories.

The DRAM section has 8 CMOS DRAMs enclosed in 250Kbit x 4bit type ZIP package.

To control DRAM refresh, address multiplex, RAS, and CAS, the DRAM controller MB/430 made by Fujitsu is operated at 20MHz.

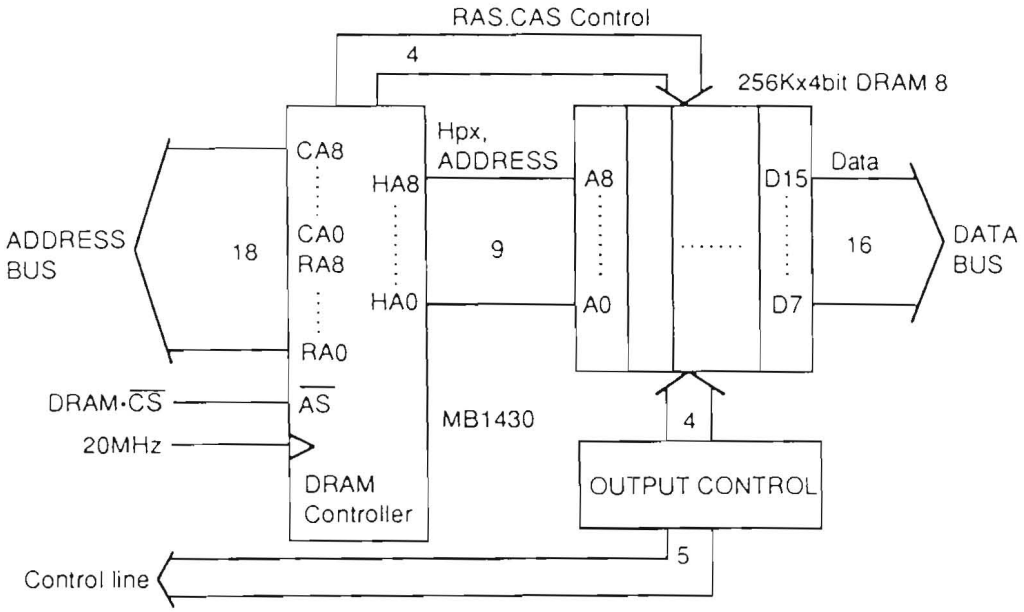
Refresh is of CAS before RAS method and uses no nibble made.

The SRAM section has 2 COMS SRAMs enclosed in 32Kbit x 8bit type SOP package.

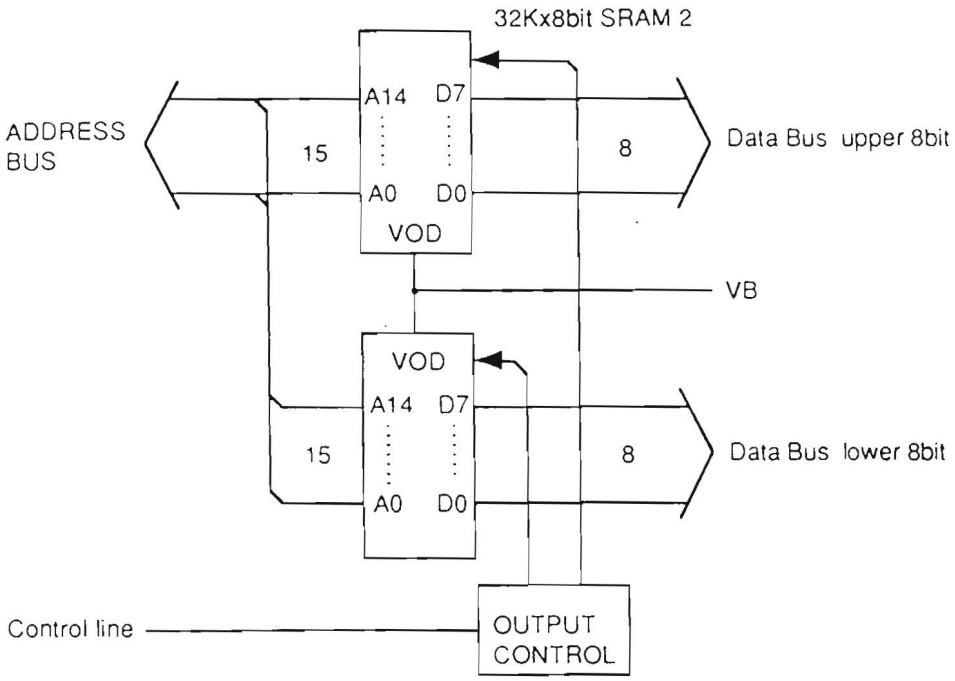
The power source of the SRAM section is backed up by nickel-cadmium battery.

Fig. 6 Memory Section

DRAM Section



SRAM Section



7. Counter Section

This instrument has 6 channels worth of 16-bit counters for generation of various timings and counting. It also has a calendar IC for updating a time and a date.

The counter has 2 Nichiden-made ICs; μPD71054. The functions of each channel are as follows:

IC1	CH0	: Lower side of the counter for counting A/D data sampling times
	CH1	: Upper side of the counter for counting A/D data sampling times
	CH2	: Interval counter for key repeat
IC2	CH0	: Lower side of the frequency-dividing counter for A/D sample timing generation
	CH1	: Upper side of the frequency-dividing counter for A/D sample timing generation
	CH2	: Frequency-dividing counter for calbration test signal generation

CH0 and CH1 of IC1 are turned into a 24-bit counter by combining them and down-counted every A/D data sampling. When A/D data sampling is performed the number of times specified by a preset value, a GATE. 0 signal is turned from Low to High.

Since a GATE signal is used as a trigger signal gate, a presample value at trigger sample time is set to the counters CH0 and CH1.

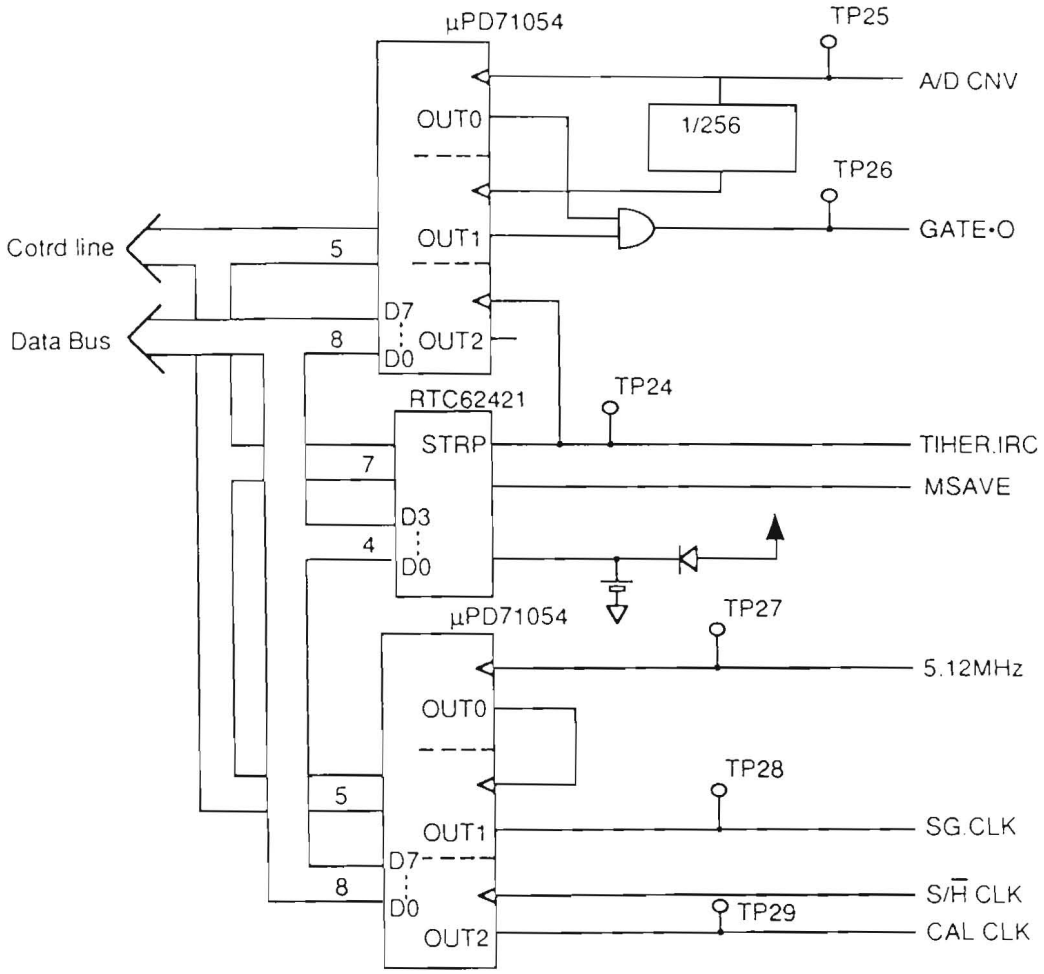
Connected to CH2 of IC1 is STDP output of RTC62421. As this output has an edge every 1/64 second, the counter is down-counted every 1/64 second. A down-count value is used by the CPU for measuring key repeat intervals.

CH0 and CH1 of IC2 are turned into a 32-bit counter by combining them and generates an A/D sampling timing by frequency-dividing 5.12 MHz source oscillation.

CH2 of IC2 generates a rectangular for calibration by frequency-dividing S/H CLK.

RTC62421 stores and updates a time and data. Since the power source is backed up nickel-cadmium batteries, time updating continues even if the system power is turned off.

Fig. 7 Counter Sedating



Test Point No.	Name	Function
24	TIM·IRO	Interrupt per 1/64 second
25	A/D CNV	Sampling timing signal
26	GATE	Trigger enable gate signal
27	5.12MHz	Sampling clock source oscillation
28	SGCLK	Sampling cycle signal
29	CAL·CLK	Calibration test signal source oscillation

8. Sample Controller Section

The sample controller section receives A/D data from the analog board and instructs DMA to transfer data in response to control commands (sample, trigger. etc.) from the CPU.

The A/D data, which is a serial signal, is inputted to the sample controller IC (μPD65031)

Inside the IC, the serial signal is converted into a parallel signal and held there.

There are 2 registers inside the IC to hold 2 data; they stores 2 A/D conversions worth of data.

For free run sampling, when 2 data are stored, 2 data transfer requests are issued to the DMAC for the A/D data in the IC to be transferred to the memory.

In free run sampling, only DMA channel 0 is used for transfer.

For trigger sampling, data is transferred through the DMA channel 0 until a trigger signal enters EXT-TRG input, and immediately after an entry of the trigger signal, data is transferred through the CMA channel 1.

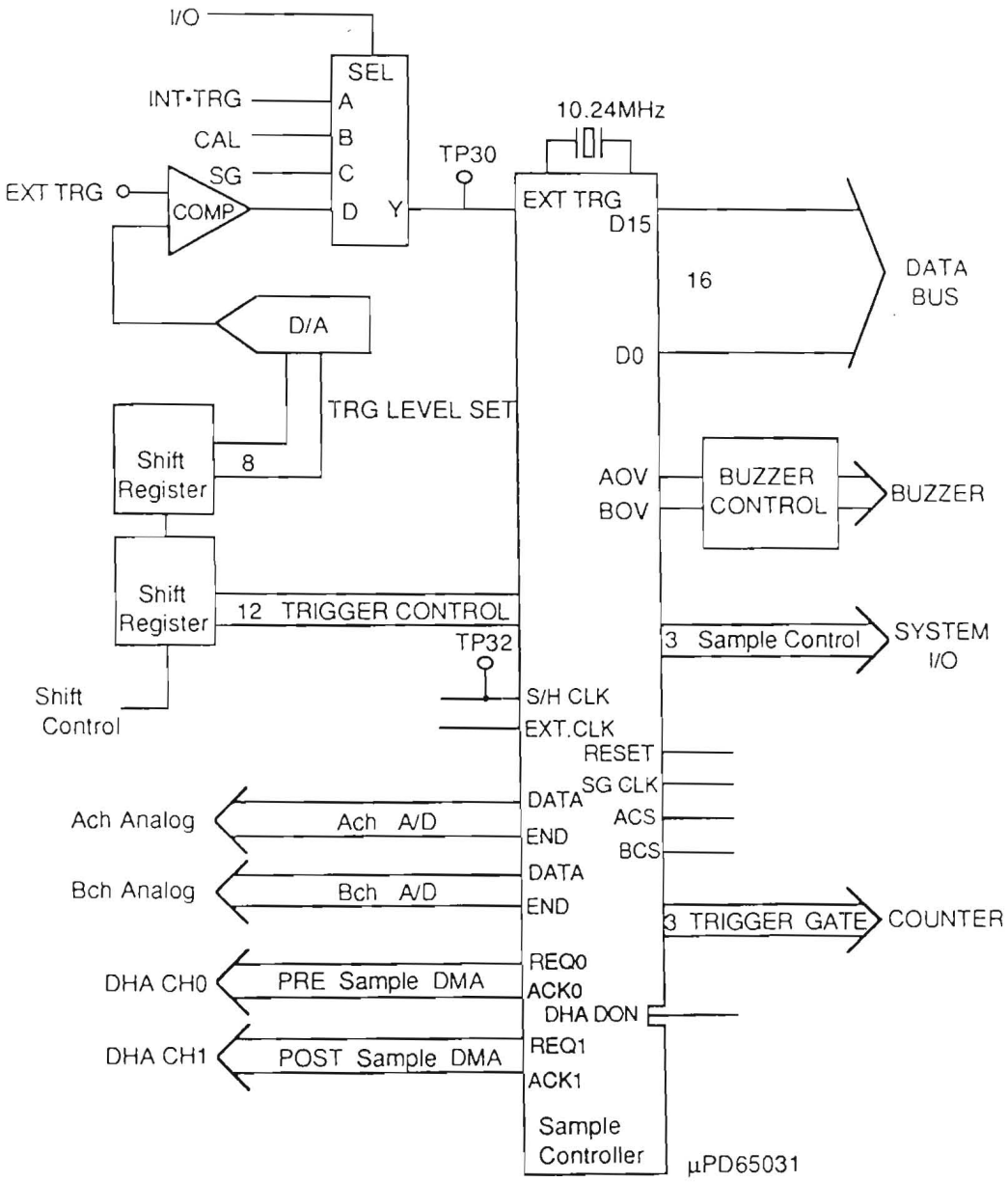
For trigger input, select one out of Internal, External, SG, and CALiBration as a trigger signal.

For both external trigger and internal trigger, the trigger level can be set with 8 bits (±1/128 of F.S. step).

For a trigger position, the μPD71054 of the counter section counts A/D sampling times,and when sampling of set positions is completed, the GATE-0 signal is inputted to the sample controller to enable trigger acceptance.

Fig. 8 Sample Controller Section

Test Point No.	Name	Function
30	TRG IN	Trigger single
32	CLK OUT	Clock synchronized with A/D sampling



9. Video OUT Section

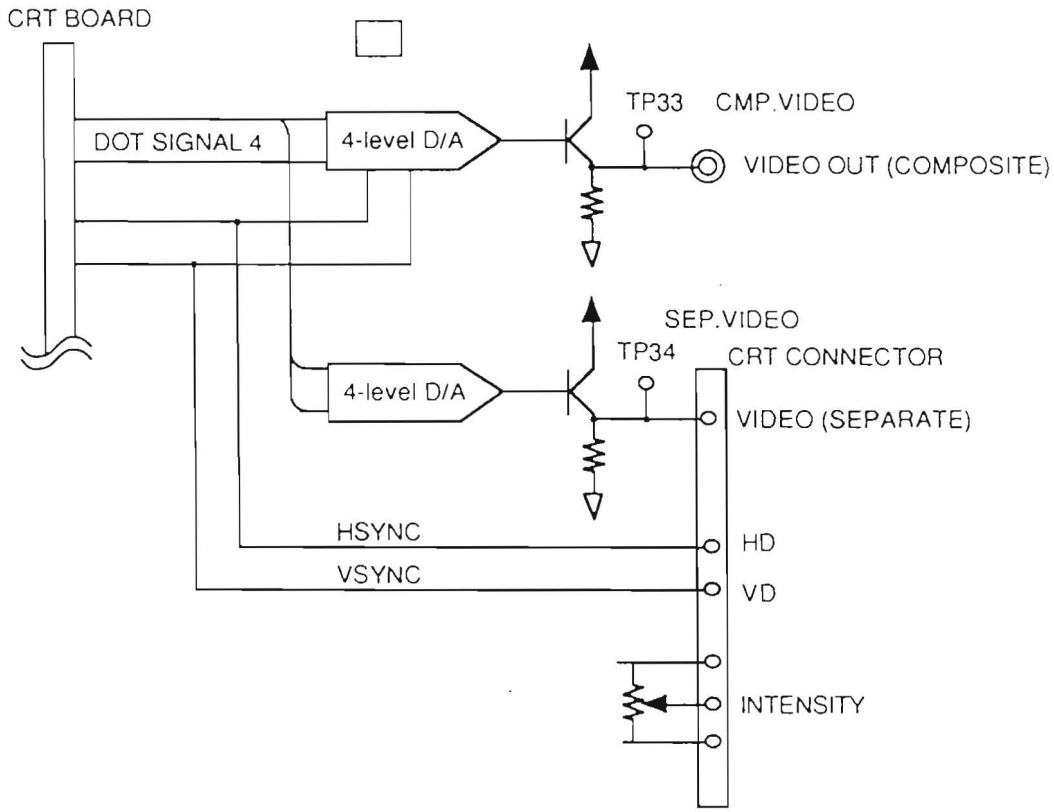
The video OUT section converts a VRAM dot data sent from the CRTC board into a video signal.

Video output is made in the form of seperate video signal at the TTL level for the built-in CRT.

The external CRT uses composite video output.

Since the video signal has 4-stage luminance, the CRT board sends 4 dot signals. They are assumed as voltage changes of the video signal by using 4-level D/A converter.

Fig. 9 Video OUT Section



Test Point No.	Name	Function
33	CMP·VIDEO	Composite video signal
34	SEP·VIDEO	Separate Video signal

10. System I/O Section

The system I/O section consists of two 24-bit parallel I/O ICs, μPD71055, and is used for hardware control.

The first μPD71055 is used for buzzer control, EEPROM control, option status read, external input read, and sample controller control.

The buzzer control circuit consists of two pulse generators, which have different pulse width setting, and buzzer driver. The I/O section controls pulse trigger and buzzer disable.

Since the EEPROM has serial data I/O, it is controlled by DATA, CLOCK, and STROBE signals.

Option status read is connected to each slot of the mother board and is a 4-bit input port to read and option board number.

External input read is connected to the external contact input of the rear panel to read a contact state.

For sample controller control, set commands such as FRRE/TPG, RESET, START, etc. on the sample controller.

The second μPD71055 is used for shift I/O control, LED control, system control, relay contact control, and external contact input control.

shift I/O control serves as a control signal to set data to A/D shift I/O, calibration shift I/O, trigger shift I/O, and SG shift I/O.

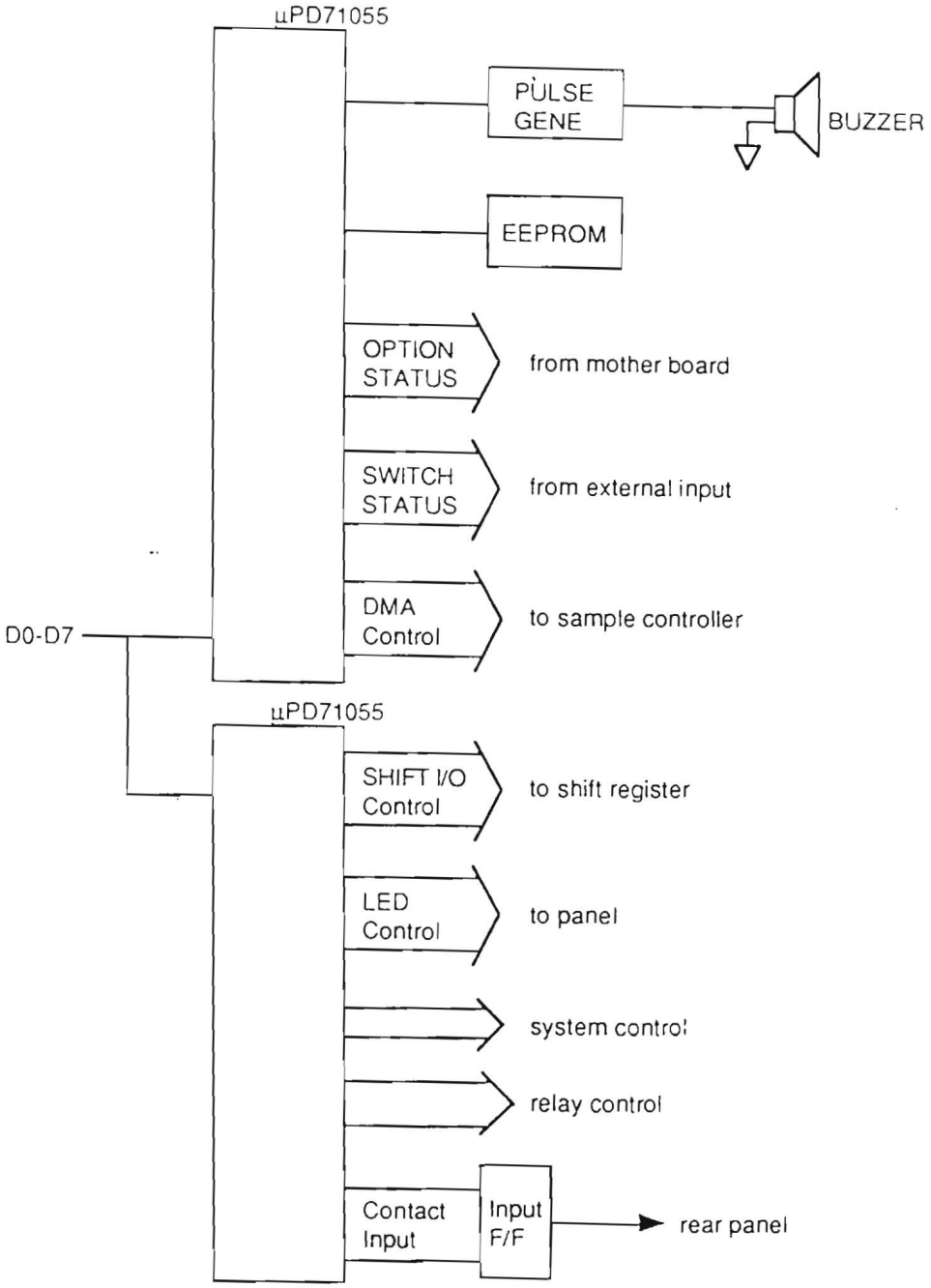
LED control is used for illuminating the LEDs on the panel.

System control sets memory access disable (MSAVE), GP-IB system controller changeover (GPID-S0), and trigger source changeover (TSEL1, TSEL2).

Relay contact control activates a comparator judgment output relay.

Contact input control provides contact input circuit disable/reset control.

Fig. 10 System I/O Section



11. Panel I/O Section

The panel I/O section controls the keys and LEDs on the front panel.

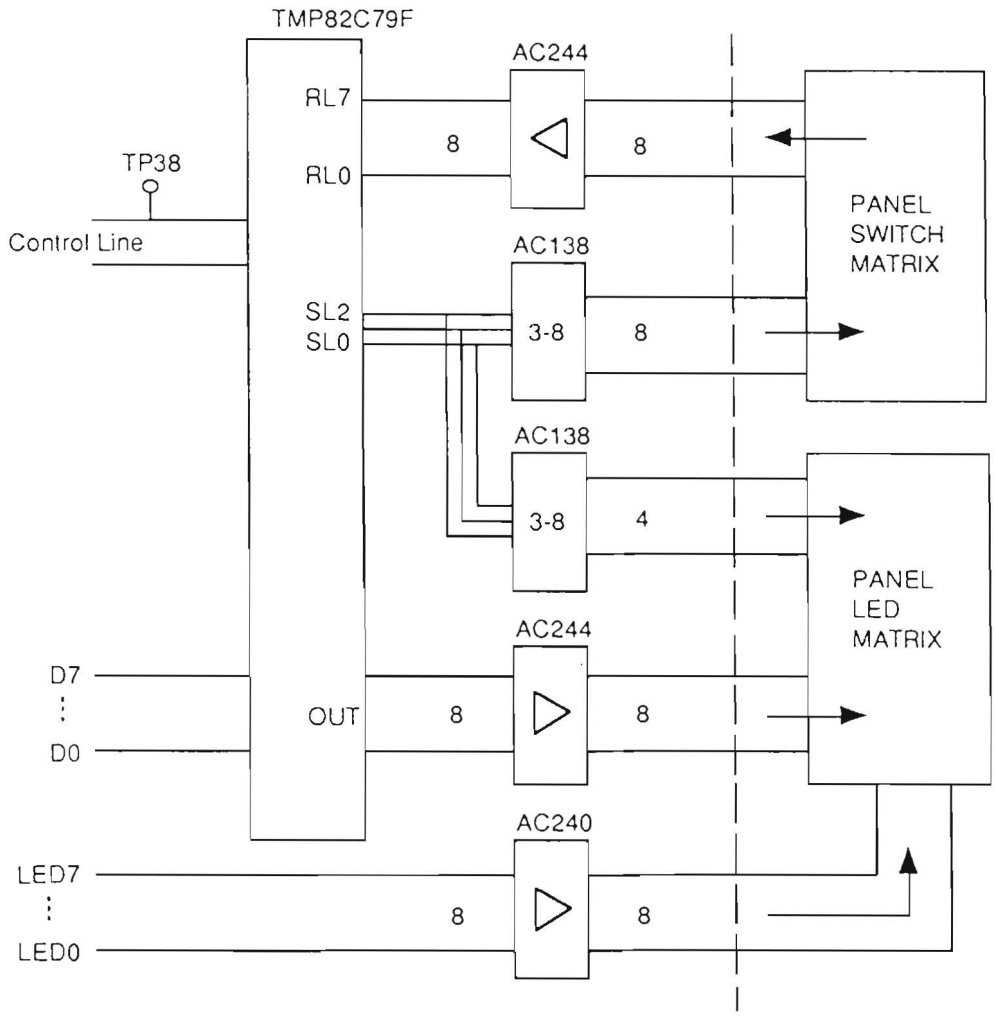
The keyboard controller TMP82C79F made by Toshiba is used to control key input and LED-on/off.

The key are arranged in matrix. The TMP82C79F scans every 8 keys to fetch a contact state, and when the key is pressed, it issues IRQ TO THE CPU to the CPU.

There are 32 LEDs arranged in 8 x 4 matrix, and dynamic lighting is employed to illumiante every 8 LEDs.

Static lighting is applied to 8 LEDs to provide control without going through the TMP82C79F.

Fig. 11 Panel I/O Section



Test Point No.	Name	Function
38	KEY IRQ	Interrupt Signal in Key Input

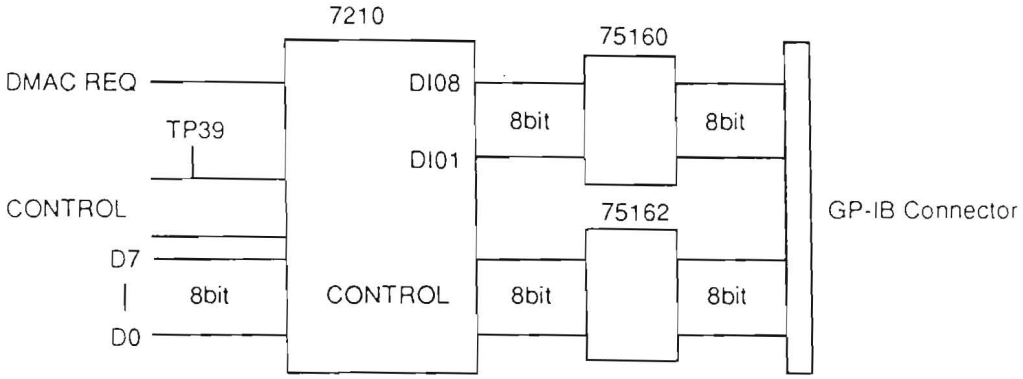
12. GP-IB, FDC Section

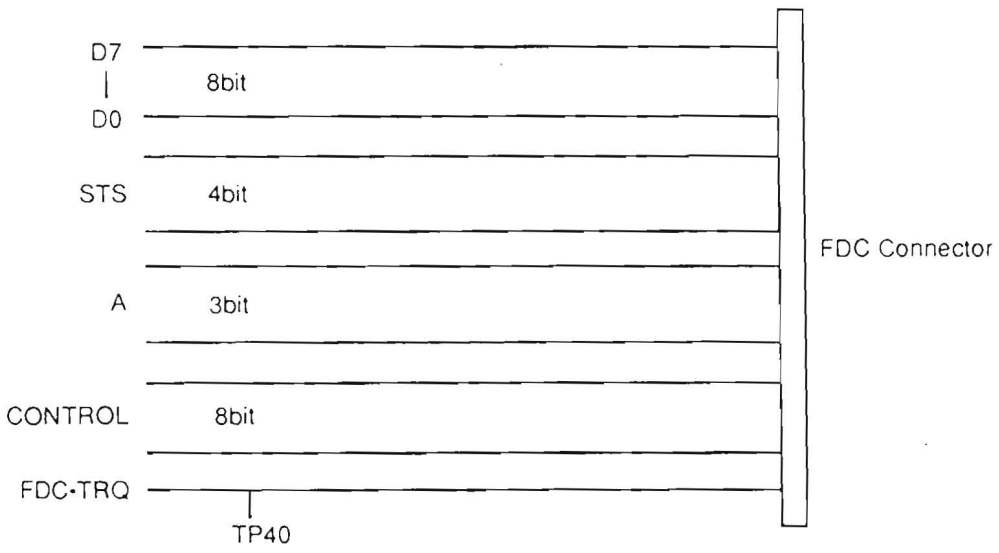
This instrument uses the GP-IB controller PD7210 made by NEC as its GP-IB, and 75160 and 75162 as its GP-IB bus tranceivers.

The DMA is used for data transfer to realize high-speed data transfer.

Since the FDC section is an optional, a CPU bus signal is wired to a connector so that an option board can by connected.

Fig. 12 GP-IB, FD I/F Section





Test Point No.	Name	Function
39	GP-IB·IRQ	Interrupt signal from GP-IB
40	FDC·IRQ	Interrupt signal from FDC

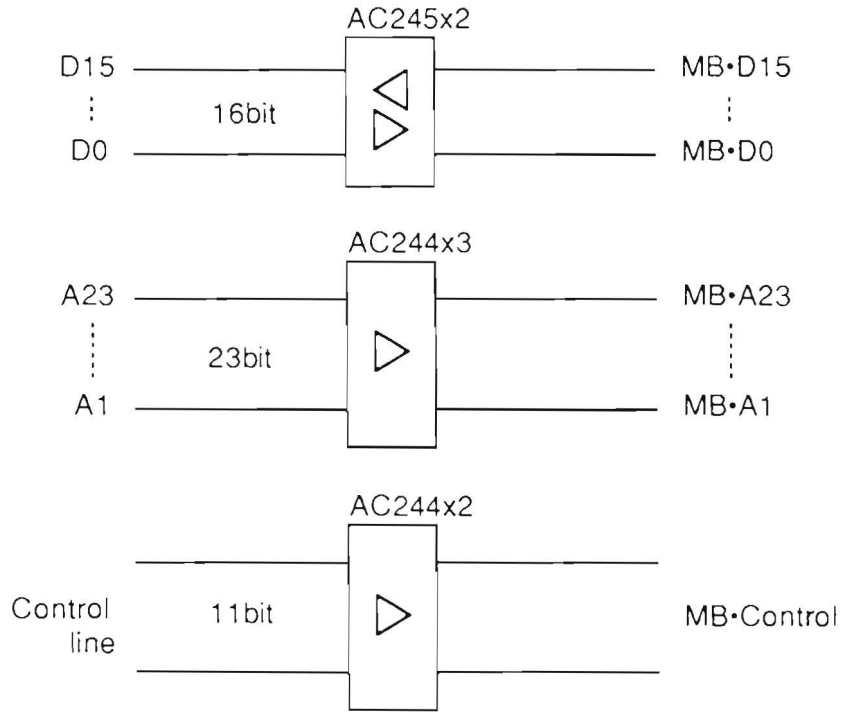
13. Bus Buffer Section

A CPU bus signal is connected to the mother board via the bus buffer.

The buffer becomes active only when 000000-3FFFFF and 600000-FFFFFF are accessed, and it becomes inactive when a vector gets on the bus.

All the signals are buffered by the current driver buffer which contains Schmitt trigger.

Fig. 13 Bus buffer Section



14. Mother Board Section

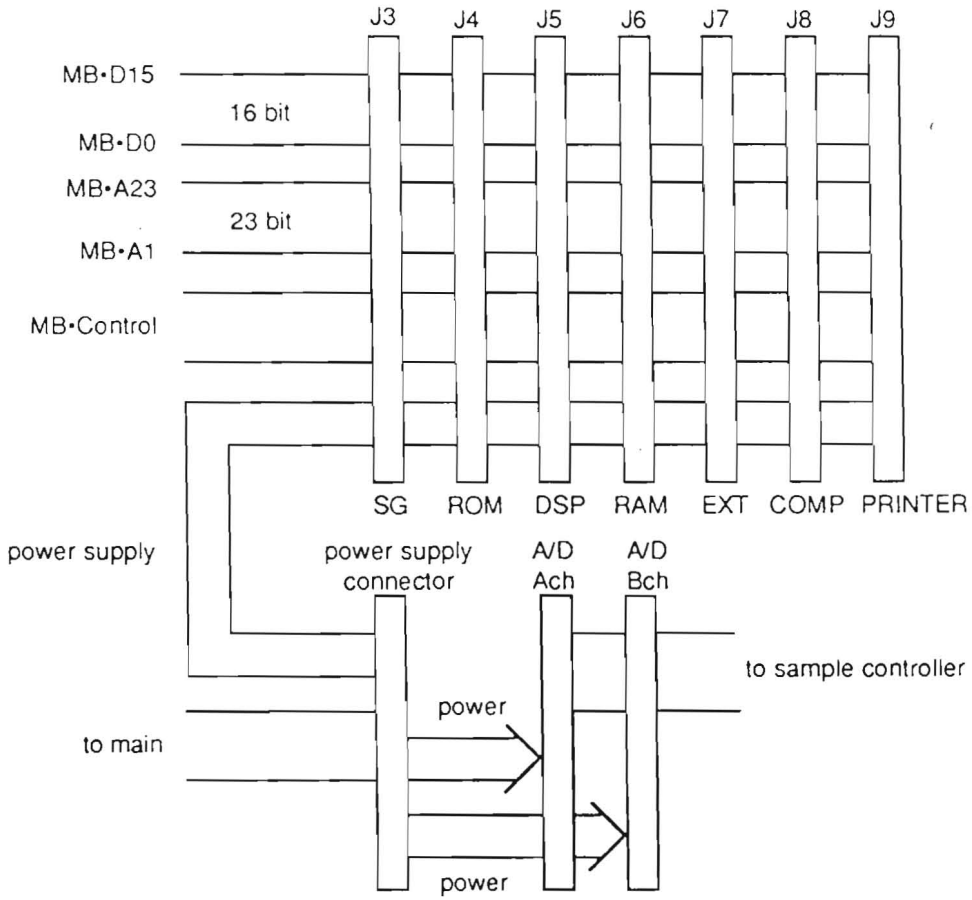
The mother board is used for adding optional devices or mounting the ROM or A/D board.

Devices are assigned to the mother board slots as follows:

J1	A/D-Bch	
J2	AxD-Ach	
J3	Signal generator	
J4	Rom	
J5	DSP	
J6	Extended DRAM	Extended SRAM may be inserted into either
J7	Spare	
J8	Comparator	
J9	Printer	

Each option board has a 4-bit status signal, and when it is inserted into the slot, it sends the status signal to the CPU via the mother board, thus an option type and its existence being confirmed.

Fig. 14 Mother Board Section



15. Appendixes

1. Test Points List

PC : 2055C (Main Board) 1/2

No.	Signal Name	Description
1	BR	Bus request : from the DMAC to the CPU
2	Missing	
3	20MHz	20MHz clock
4	ACRTC.IRQ	Interrupt request from ACRTC to the CPU
5	CPU.CLOCK	10MHz CPU clock
6	BGACK	Bus Grant Acknowledge ; bus acquirement confirmation from the DMAC to the CPU
7	R/W	Read/Write ; bus status issued by the bus master
8	AS	Address Strobe ; bus status issued by the bus master
9	IACK	Interrupt Acknowledge; bus status issued by the bus master
10	RES	Reset ; system reset signal
11	REQ0	A/D data transfer request to the DMAC
12	REQ1	A/D data transfer request to the DMAC
13	REQ2	GP-IB data transfer request to the DMAC
14	REQ3	FD data transfer request to the DMAC
15	DONE	DMAC transfer complete signal
16	DMA.IRQ	Interrupt request from the DMAC to the CPU
17	DTACK	Bus master data confirmation signal
18	CAL-OUT	Calibration signal output
19	CAL+5V	Calibration circuit power
20	VCAL	Ditto
21	-VCAL	Ditto
22	VSG	Ditto
23	VB	Nickel-cadmium battery terminal voltage
24	TIM.IRQ	Interrupt request from the calendar IC to the CPU
25	ADCNV	A/D conversion timing signal
26	GATE	Sample precounter output
27	5.12MHz	A/D conversion timing signal source oscillation
28	SG-CLK	Sampling timing signal
29	CAL-CLK	Calibration clock
30	TRG.IN	Trigger input
31	CLK.IN	Sample clock input
32	CLK.OUT	Sample clock output
33	CMP.VIDEO	Composite video signal output
34	SEP.VIDEO	Separate video signal output
35	VSYNC	Video vertical synchronism
36	HSYNC	Video horizontal synchronism
37	CMP.IRQ	Interrupt request from the external start input to the CPU
38	KEY.IRQ	Interrupt request from the key to the CPU
39	GPIB.IRQ	Interrupt request from the GP-IB to the CPU
40	FDC.IRQ	Interrupt request from the FDC to the CPU

PC : 2055C (Main Board) 2/2

No.	Signal Name	Description
41	+VS12	+12V for the system
42	-VS12	-12V for the system
43	VSG	Ground for 12V
44	+VL5	+5V for the system logic
45	VLG	Ground for the system logic
46	+VC12	+12V for the CRT/printer
47	VCG	Ground for the CRT/printer
48-50	Missing	
51-54	GND	Ground for the system logic

PC : 2058 (ACRT Board)

No.	Signal Name	Description
1	VCC	+5V power
2	GND	+5V power ground
3	2CLK	ACRTC clock, 4.6MHz
4	RAS, A	VRAM RAS signal
5	CAS, A	VRAM CAS signal
6	YADL	VRAM address latch signal

PC : 2060 (Extended DRAM)

No.	Signal Name	Description
1	VCC	+5V power
2	GND	+5V power ground
3	DTACK	Data confirmation signal

PC : 2062 (Printer Board)

No.	Signal Name	Description
1	GND	Power ground
2	HEAD.CLK	Head power-on pulse source oscillation
3	HEAD.STB	Head power-on pulse
4	STEP.RATE	Feed motor drive rate signal

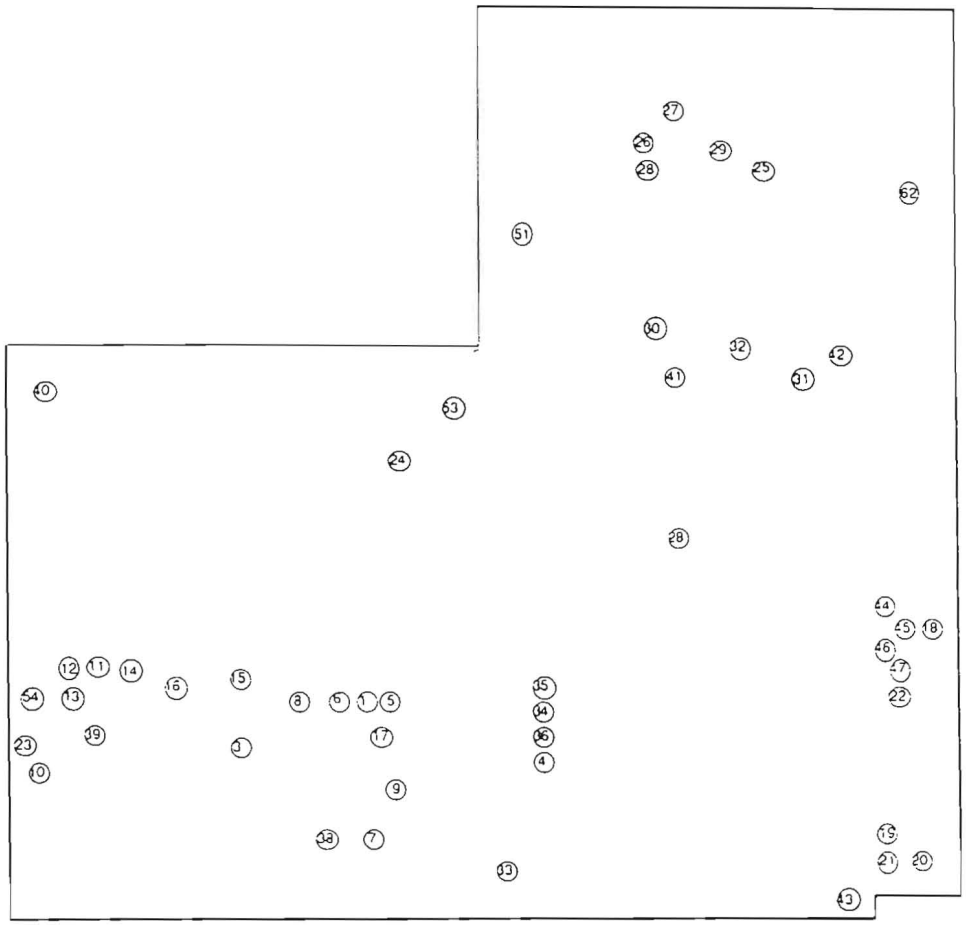
PC : 2063 (Floppy Board)

No.	Signal Name	Description
1	GND	Power ground
2	VCC	+5V power
3	CLK	16MHz clock for the floppy controller

PC : 2170 (Extended SRAM)

No.	Signal Name	Description
1	VCC	+5 Power
2	GND	Power ground
3	DATACK	Data confirmation signal
4	VB	Battery terminal voltage

15-1 PC : 2055 (Main Board) Test Point Map



15-2 Memory MaP

ADDRESS	ASSIGNMENT	BUS
000000	STANDARD ROM AREA FOR EXTENSION	EXTERNAL
100000		
200000		
300000		
400000	I / O AREA	INTERNAL
500000	STANDARD DRAM AREA	
600000	EXTENDED RAM AREA	EXTERNAL
700000		
800000		
900000		
A00000		
B00000		
C00000		
D00000		
E00000	SPARE	
F00000	OPTION I / O AREA	

ADDRESS	ASSIGNMENT
400000 40FFFF	STANDARD SRAM AREA
410000 41FFFF	FOR EXTENSION
4FFF00 4FFF1F	FLoppy Disk Controller
4FFF20 4FFF3F	Key Controller
4FFF40 4FFF5F	GP-IB Controller
4FFF60 4FFF7F	Timer IC
4FFF80 4FFF9F	Counter #1
4FFFA0 4FFFBF	Counter #2
4FFFC0 4FFFDF	PI0#1
4FFFE0 4FFFFF	PI0#2

15-3 Option Status No. Assignment Table

Option	Status No.
OP-01 (Floppy)	0XXX (at #8)
OP-02 (Printer)	1100 (at #7)
DP-03 (Extended RAM1N)	0010 (at #3 or #4)
OP-04 (Extended RAM2M)	0011 (at #3 or #4)
OP-05 (Extended RAM 512K)	0100 (at #3 or #4)
OP-06 (OSP)	0110 (at #3)
OP-07 (SG)	0101 (at #2)

2-3-4 CRT Control Board PZ : 2058

The CRTC section generates video signals to be sent to the CRT or plots display data.

The ACRTC HD6348CP8 made by Hitachi is used to control the CRTC section, eight 256-Kbit DRAMs (64 x 4 type) for the VRAM, and gate arrays for timing generation and P-S conversion.

The CRTC mainly performs two operations by turn ; reading the VRAM to generate a video signal, and plotting display data. Therefore, an ACRT memory access is a dual access.

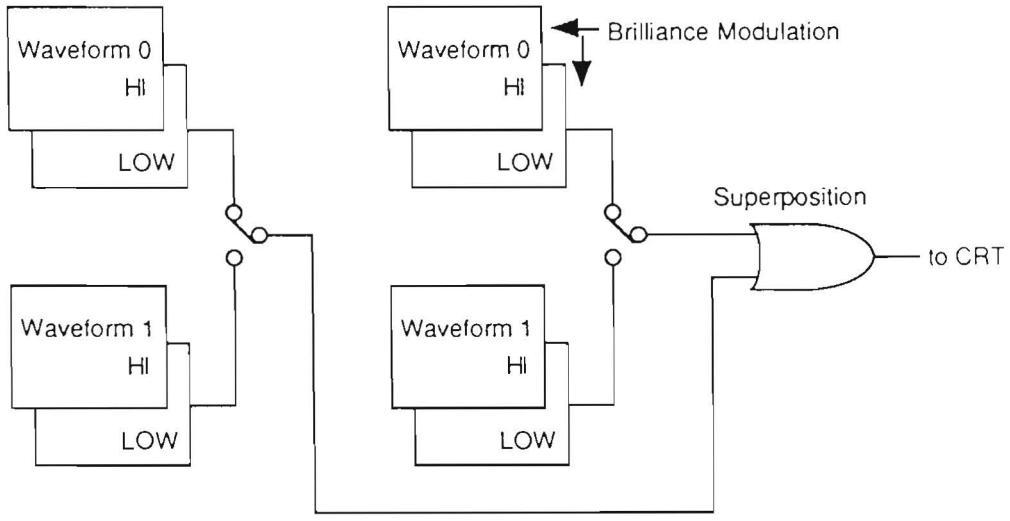
① Reading the VRAM

In this cycle, the ACRTC outputs addresses to sequentially read the VRAM, with which the VRAM are accessed. The read 32-bit data enters the gate array and is turned into a video signal by P-S conversion.

② Plotting the display data

In this cycle, the ACRTC reads the RAM to be plotted in accordance with a plot command sent from the CPU, and after plotting, it writes to the RAM.

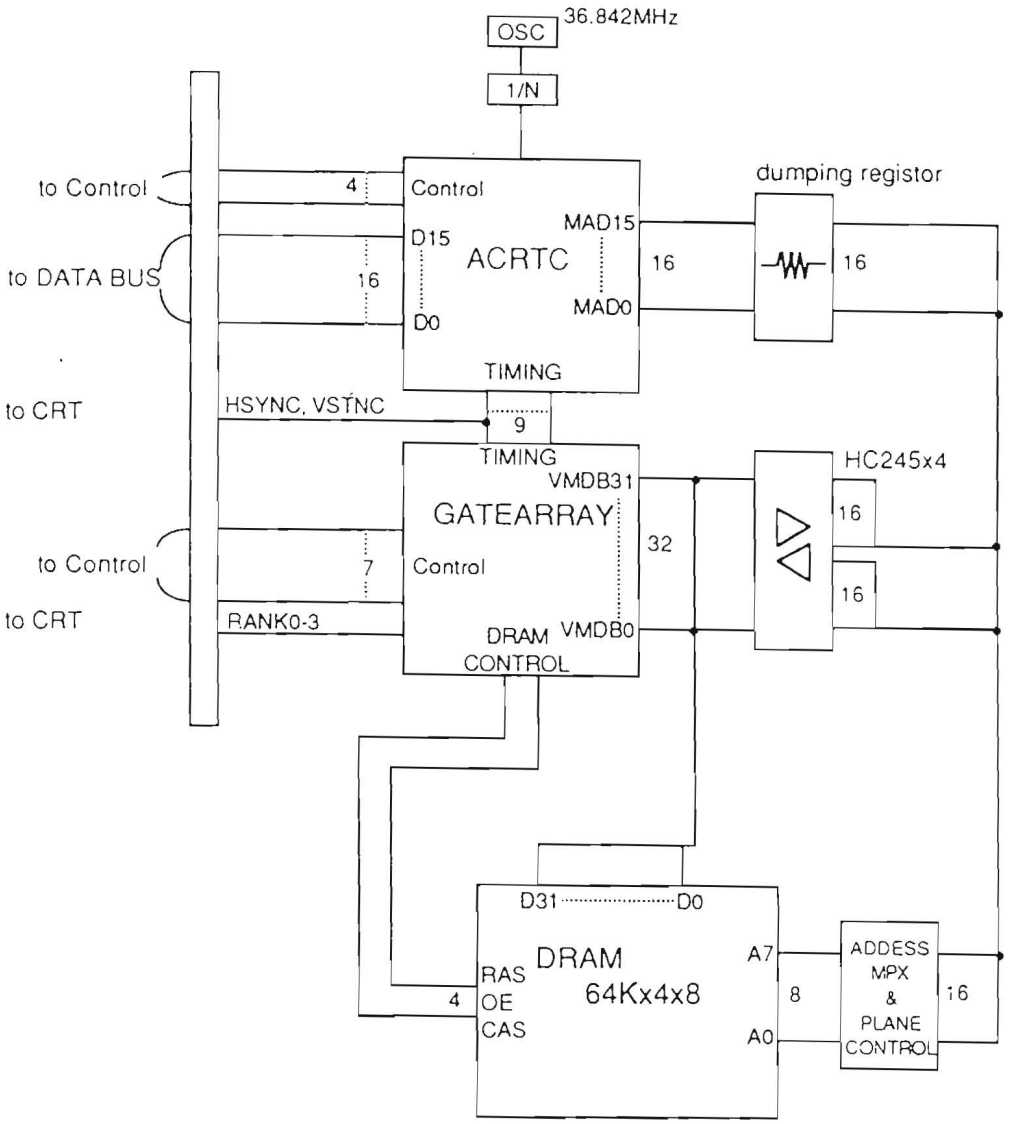
The VRAM has the following configuration to realize brilliance modulation, superposition, high speed, etc.



The dot matrix on the screen is 560 x 400 ; each dot is displayed at 4 gradations.

Since the VRAM is in the address space of the ACRTC, you must access it via the ACRTC from the CPU.

Fig. 16 CRTC Section



2-3-5 ROM Board PZ : 2059

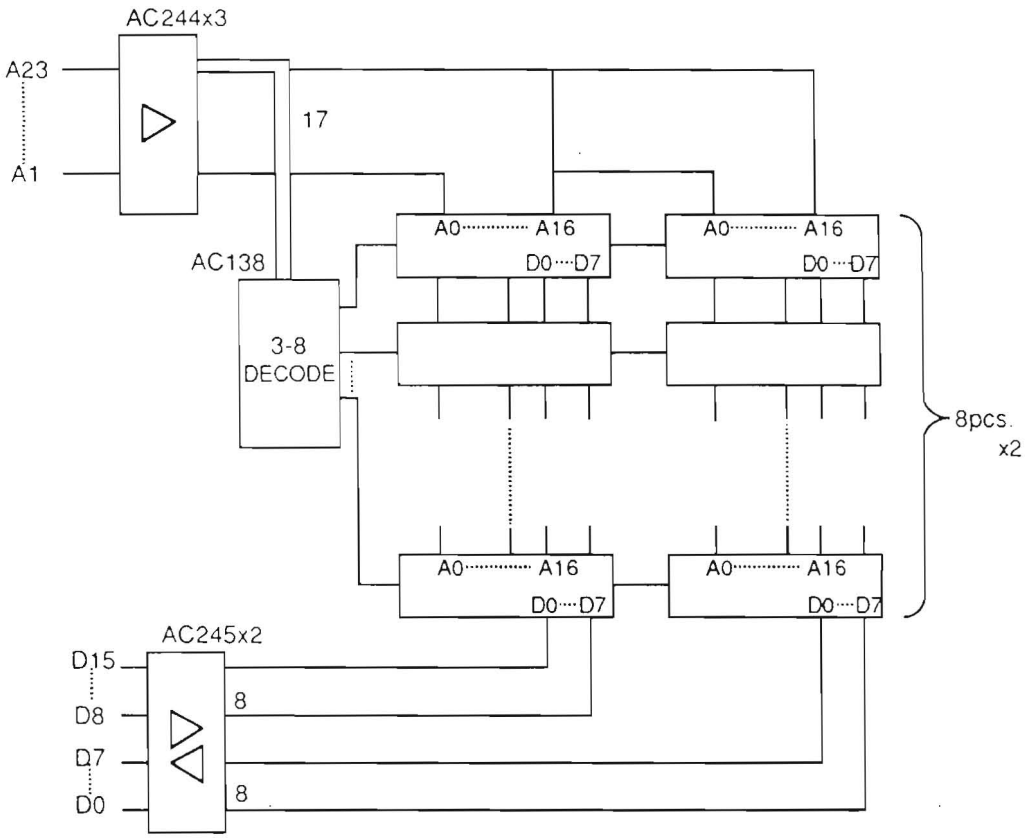
Programs and data are written in the 1 Mbit EPROM-on the ROM board.

The EPROM used is a 1Mbit (128 K 8) type. Up to 16 of them can be mounted on the board. In that case, a ROM capacity is 2 MB.

Since the address space of the board has 4 MB, it is possible to mount up to 4 MB if a jumper wire is changed over by using the 2 Mbit type ROM.

The ROM board does not function unless it is inserted into J4 of the mother board.

Fig. 15 ROM Section



2-3-6 Panel Key and Soft Ley Boards PZ : 2056, 2057

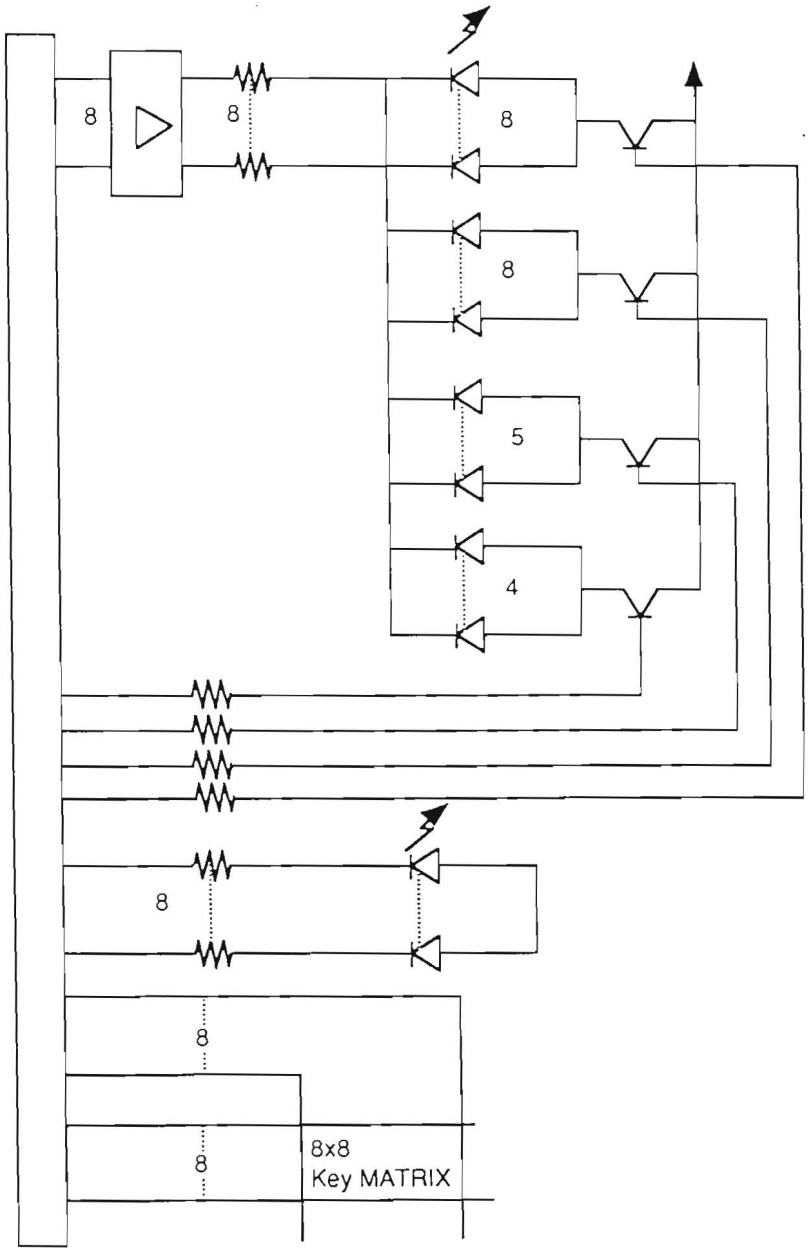
The front panel has 64 keys and 32 LEDs ; they are connected to the main board TMP82C79F.

The keys are arranged in 8 x 8 matrix. They are scanned by the IC and a contact state is taken in.

Of 32 LEDs, 24 of them are of dynamic lighting, and 8 of them are of static lighting .

Dynamic lighting is controlled by the IC.

Fig. 17 Panel Section



2-3-7 CRT Unit

Table of Contents

1. General Description

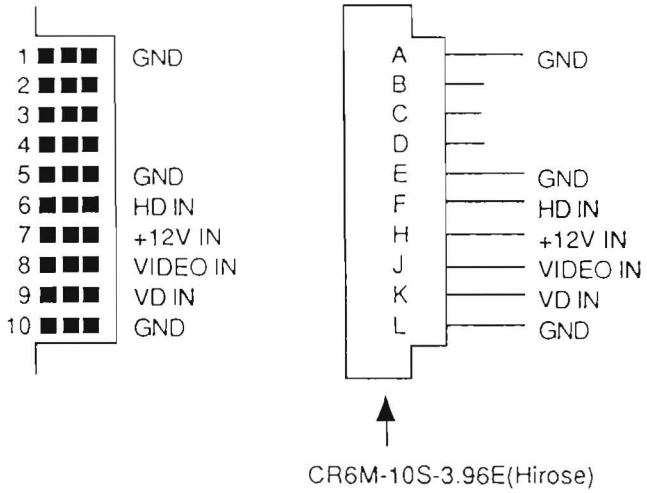
This unit is a chassis type character display monitor which uses 7-inch 90°-deflection P31 non-glare CRT. A supply voltage is DC stabilized +12 V. There are three signals, HD (horizontal drive signal), VD (vertical drive signal), and VIDEO (TTL video signal), to connect to external signals.

2. Specifications

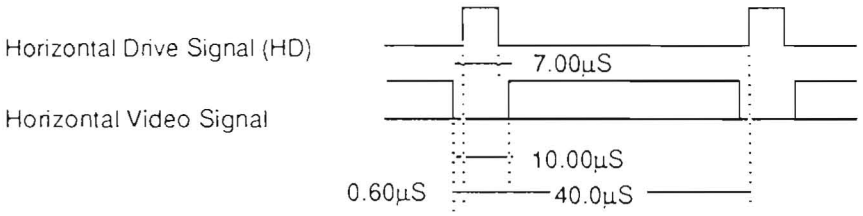
(1) Supply voltage	12V DC ±10% (screen size adjusted at 12V DC), Ripple = 10mVp-p or less
(2) Power consumption	18 W or less
(3) Input signals	
(a) video signal	4V ±1.5V (TTL level, positive polarity), Rise/fall time = 30ns, Input impedance = approx. 4k
(b) Horizontal drive signal	4V ±1.5V (TTL level, positive polarity), Pulse width = 4 to 40µs
(c) Vertical drive signal	4V ±1.5V (TTL level, negative polarity), Pulse width = 60 to 1,400µs, Input impedance = 1kΩ or more
(4) Image amplifier	
(a) Frequency	30MHz ±3dB (100kHz as reference)
(b) Maximum gain	18dB or more
(5) Synchronous signal	
(a) Horizontal scanning frequency	25.00 ±0.3kHz
(b) Vertical scanning frequency	60.00Hz
(c) No. of effective scanning lines	342 lines (non-interlace)
(d) Horizontal blanking period	10.00µs
(e) Vertical blanking period	3.00ms

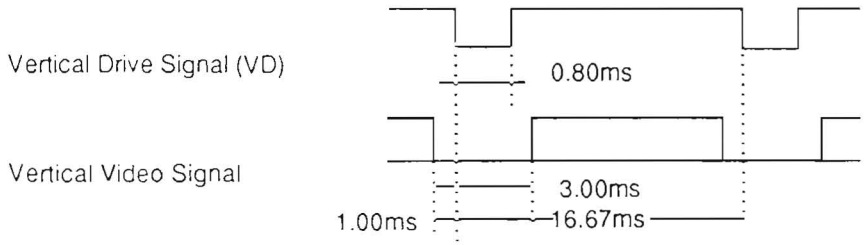
(6) Display screen	
(a) Screen size	126 ± 5mm (horizontal) x 85 ±4mm (vertical)
(b) Display position	±5mm both in the horizontal and vertical directions against the mechanical center of the CRT
(c) Geometrical distortion	Trapezoidal distortion (both horizontal and vertical) 2.5% or less, Vertical barrel and pincushion distortion 2.5% or less, Horizontal barrel and pincushion distortion 2.5% or less
(d) Screen inclination	±3mm or less
(e) Horizontal resolution	700 lines or more (20 ft. at the center at Low)
(f) Linearity	10%
(7) CRT	Type : E2871B31- HT, Phosphor : P31, Fluorescent screen : Non-glare, Anode voltage : Approx.10kV
(8) Ambient conditions	Ambient temperature, (operating) : 0°C to +50°C Ambient temperature, (non-operating) : -30°C to +65°C Ambient humidity, (operating) : 10% to 85% Ambient humidity, (non-operating) : 5% to 95%
(9) Structure	
(a) External dimensions	183mm (w) x 165mm (H) x 233mm (D)
(b) Weight	Approx. 2kg
(c) CRT mounting angle	80° ±1° against the monitor installation surface

3. Connection

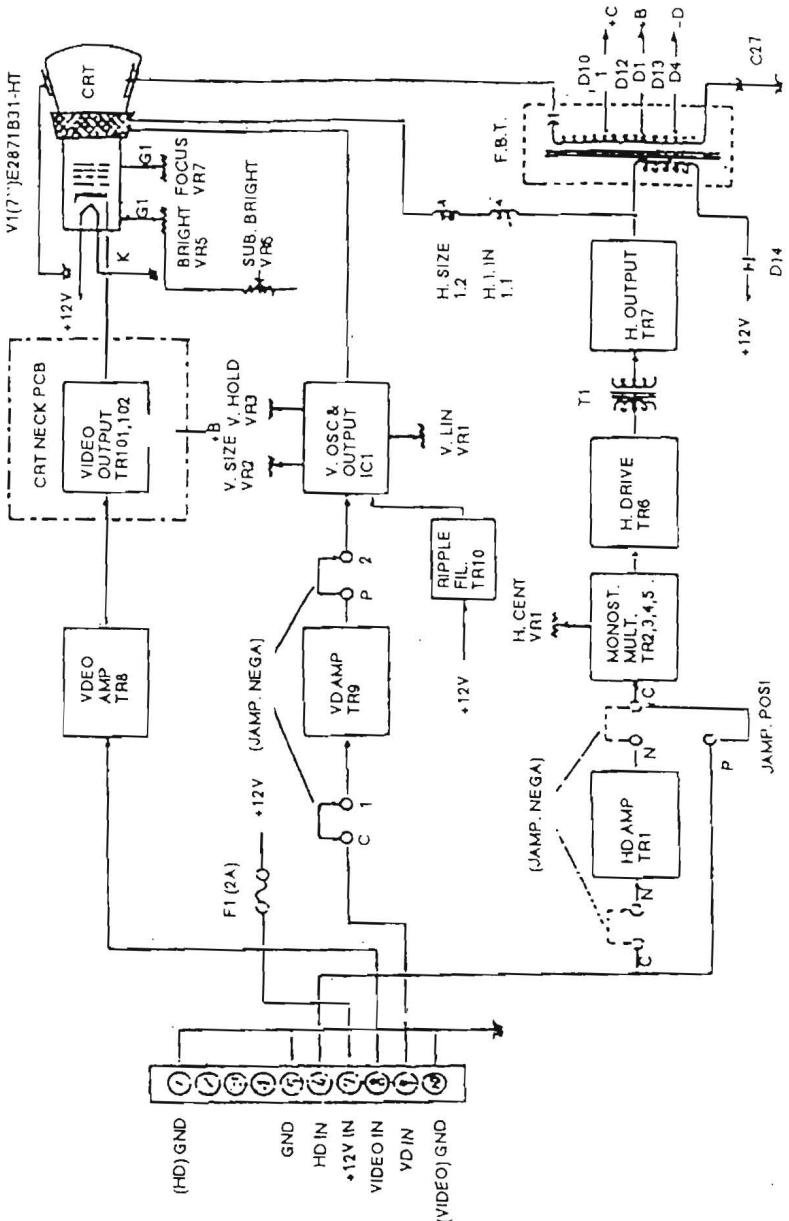


4. Input Signal Timing





5. Block Diagram



6. General Description of Circuits

6-1 Image Amplifier

A video signal, which was applied to the VIDEO INPUT terminal (CNO-8) of the main PCB, is supplied to the CRT neck PCB through the buffer amplifier TR8.

At the CRT neck PCB, it is applied to the cascade amplifier formed by TR102 and TR101 through R105. This cascade amplifier has gain of about 25 dB, and an output signal from the collector TR101 is applied to the cathode of the CRT (pin 2) through R111.

C104, C105, C106, and R108 are tp compensate a frequency characteristic.

6-2 Vertical Deflection Circuit

A vertical synchronizing signal, which was applied to the VD INPUT terminal (CNO-9) of the main PCB, is supplied to the IC1 pin 5 (synchronous pulse input terminal) directly (for positive polarity) or after a waveform is shape by TR9 (for negative polarity).

On the other hand, the IC1 performs internal transmission with the time constant by C36, and is externally synchronized by an external pulse applied to the pin 5. The pulse generated in this circuit becomes a deflection frequency for the vertical deflection section.

A pulse from the internal vertical transmission circuit of the IC is applied to the internal saw-tooth wave circuit of the same IC, and a saw-tooth waveform is generated by C35 externally attached to the pin 4.

This saw-tooth wave is applied to the output stage input terminal of the pin 7 through VR2 (V-size) and R44 and enters the vertical output stage.

The signal, which entered the vertical output stage, is applied from the output terminal pin 1 to the vertical deflection yoke through C31. Since this deflection yoke provides deflection in accordance with a current waveform, a current flowing through this yoke is converted into a voltage waveform at R47 and stabilized by applying feedback to the IC1 pin 9.

6-3 Horizontal Deflection Circuit and High Voltage Generator

A horizontal synchronizing signal, which was applied to the HD INPUT terminal (CNO-6) of the main PCB, is applied to the TR2 base through C3, R8, and D2 directly (for positive polarity) or after a waveform is shaped by TR1 (negative polarity).

On the other hand, TR2 and TR3 build up a signal stabilized multi-vibrator, providing a delay pulse circuit of almost 1/2 cycle (horizontal synchronism). This delay amount is adjusted by VR1 (H. CENT).

When a pulse is applied to the TR2 base, the pulse with almost 1/2 cycle is outputted from the collector TR3 and applied to the emitter TR4 at the next stage.

The TR4 and TR5 from a non-stabilized multivibrator, repeating transmission synchronously with the pulse applied to the emitter TR4.

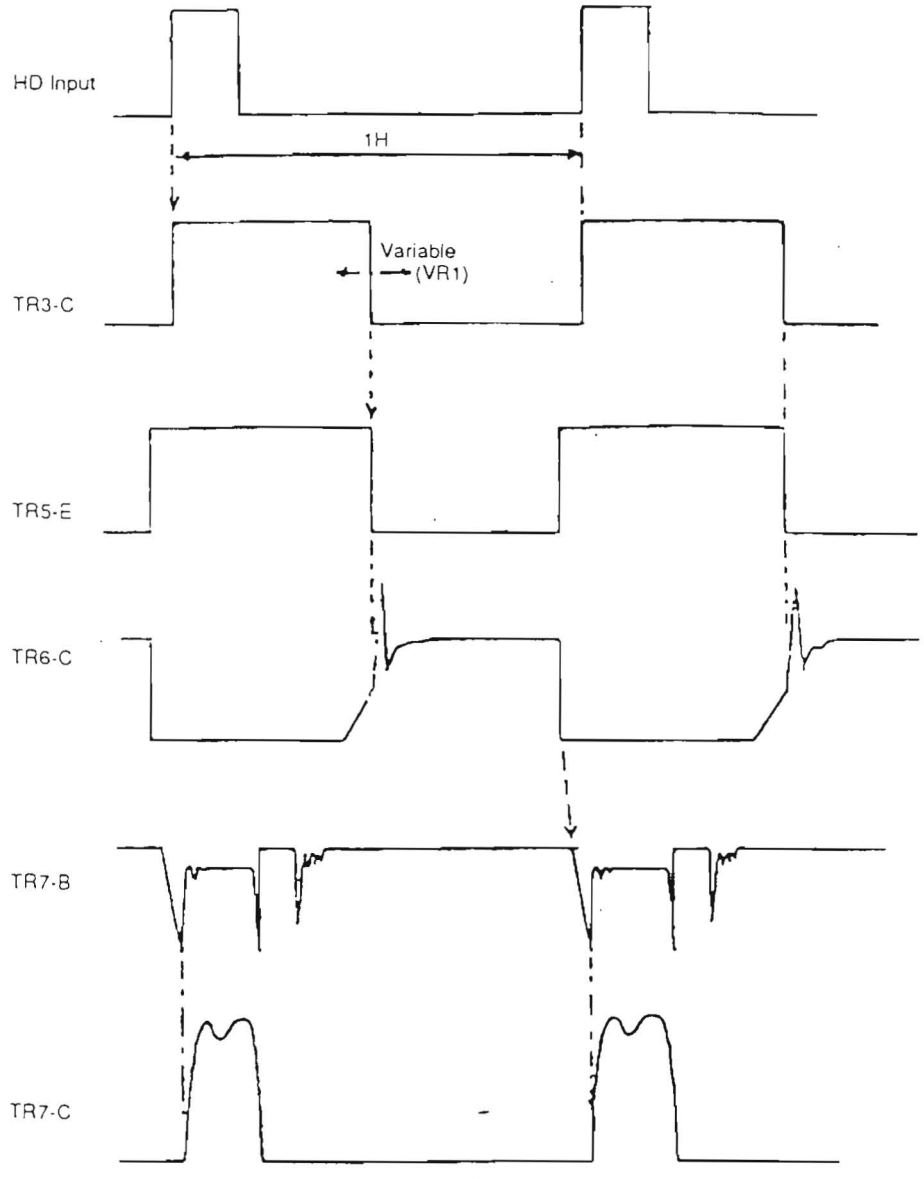
An output from the non-stabilized multivibrator (emitter TR5) enters TR6 and is applied to the base of the horizontal output transistor TR7 through the horizontal drive transformer (T1). This causes TR7 to perform switching.

A defection pulse is generated at the collector TR7 by the transient phenomenon that magnetic energy stored in the flyback transformer (FBT) at TR7 ON time moves to the tuning capacitors (C22, C23) and horizontal deflection coil when TR7 is turned off, and a saw-tooth wave current flows to the deflection yoke.

When this is done, the voltage coiled up by the secondary winding of the FBT is rectified by the rectification diode (for high voltage) and applied to the anode of the CRT.

At the anode, a rectification capacitance is determined by a floating capacitance between the carbon section of the CRT display screen and internal anode.

Fig. 9-1 shows the external timing mentioned above.



2-3-8 Power Unit PZ : 2067/2068

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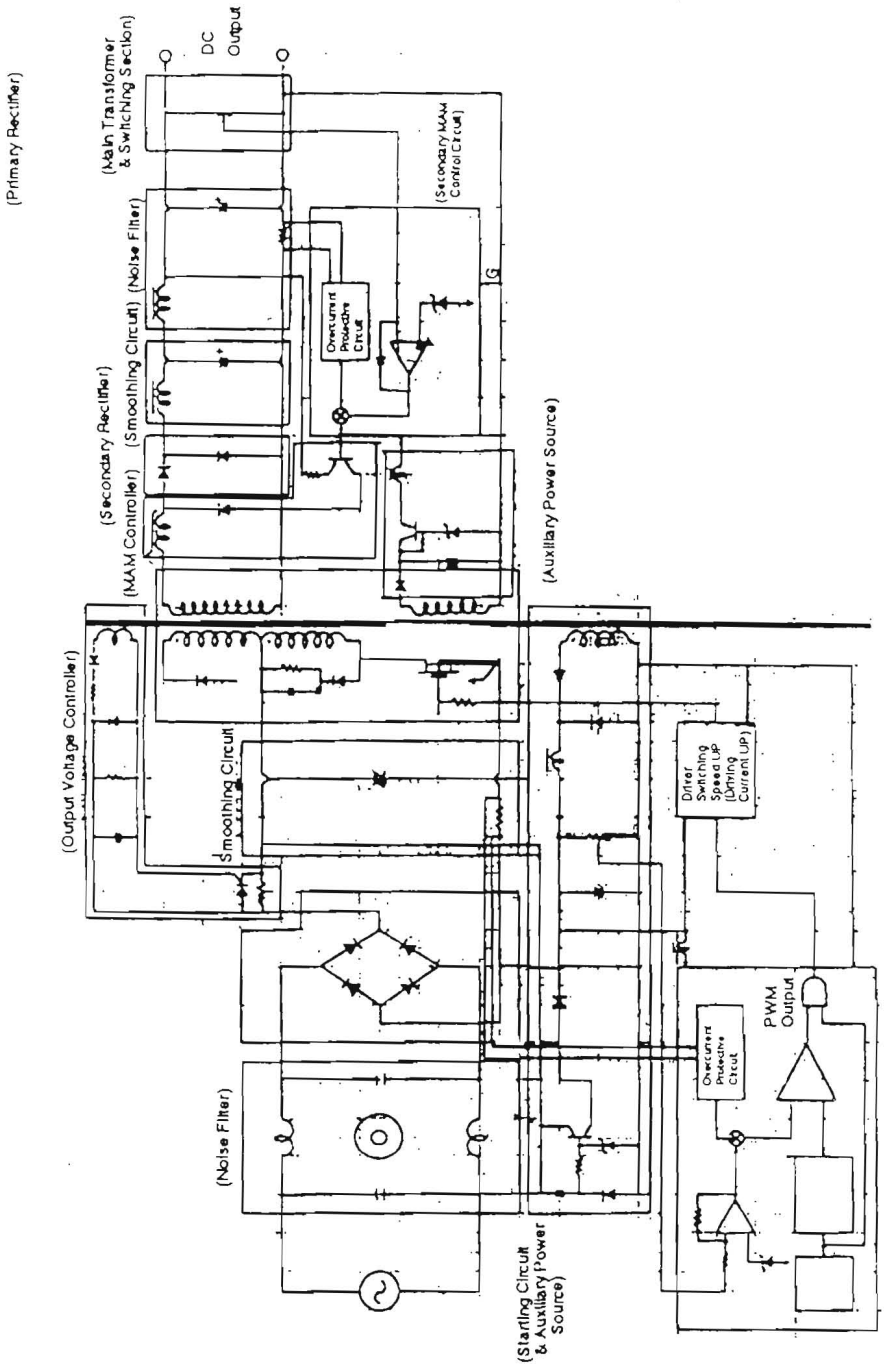
Power Unit Block Diagram



1. General Description

This circuit is a switching power source which generates an output voltage required for operations of this instrument out of an input voltage of 90 V-264 V AC (no switching tap).

As shown in the power source block diagram, this circuit consists of the following components :

2. Input Section

1. Noise filter
2. Rectifier and smoothing circuit
3. Rush current protective circuit
4. Control circuit
5. Auxiliary power circuit for control
6. Drive and switching circuits

3. Output Section

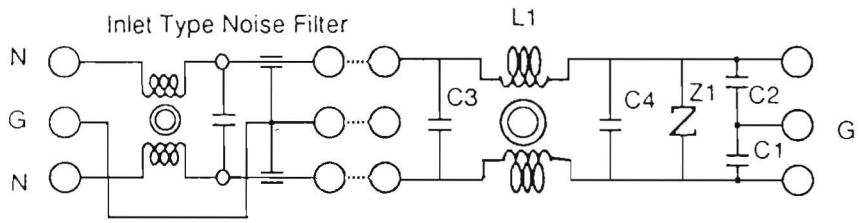
1. Output power circuit
2. Sense amplifier
3. Auxiliary power circuit
4. Overvoltage protective circuit and low battery circuit

2. Input Section

1. Noise Filter

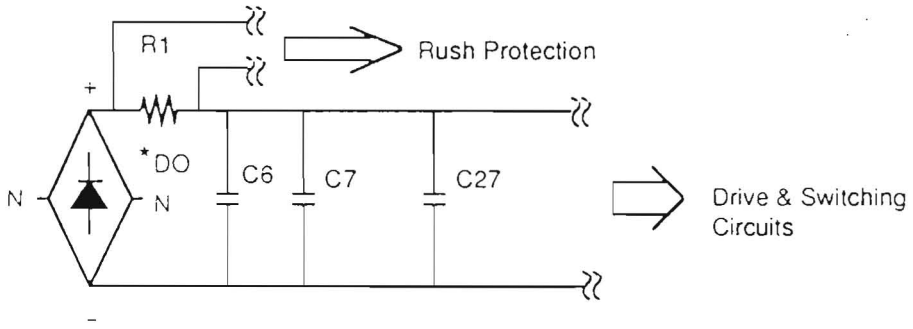
This filter is used to prevent a noise from entering devices from the AC line and a switching noise from leaking from the power source to the line.

This instrument uses an inlet type noise filter attached to an input plug. Noise is suppressed here once, and then, it is further suppressed by the noise filter provided inside the power circuit.



2. Rectifier and Smoothing Circuit

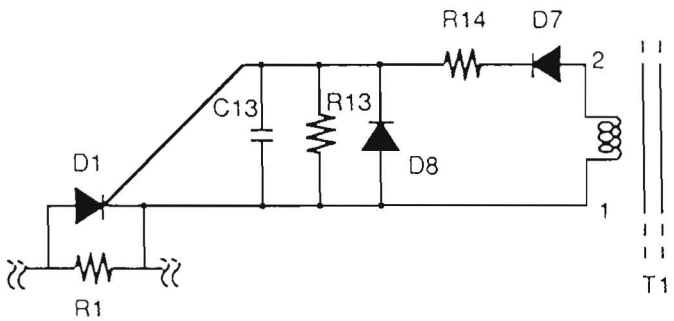
AC (or DC) input is directed into the diode stack D0 to rectify it, and charged to the capacitor C7 to smooth it into a DC voltage.



3. Rush Current Protective Circuit

When the power switch is turned on, a charging current to the voltage smoothing capacitor C7 becomes a large current temporarily. In order to prevent damages on the pattern by this large current, the input current is limited by the resistor R1.

A current flows through this resister, and a lapse of time required for charging the capacitor (when a capacitor voltage increases over a certain level), R1 is short-circuited by a thyristor to eliminate power loss by R1.



4. Control Circuit

The MB3759 P-G is used for a control IC for this power source.

This IC is a generally used for switching regulator control for the moment and is equivalent to the TL494.

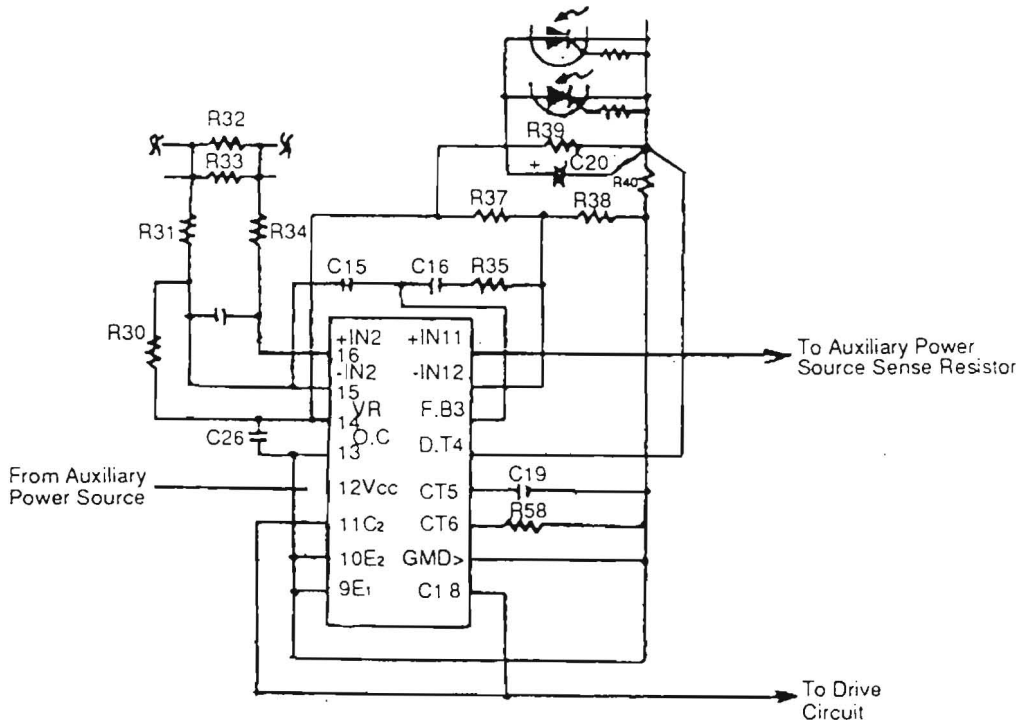
An oscillation frequency for this IC has been set to f = 130 kHz.

The power source for this instrument has 10 output sections, and this IC has only two sense amplifiers for them. For circuit control, therefore, in addition to PWM control, magnetic amplifier control (magnetic PWM control) is used for the secondary side (output side : corresponds to the secondary winding for the transformer).

The MB3759 P-G changes a switching pulse width in accordance with an AC input voltage to make constant an integrated value of voltage time transmitted to the secondary side.

As this suppresses an output change caused by an input voltage change, an output voltage is adjusted by the output circuit to be kept constant, in accordance with an output current change.

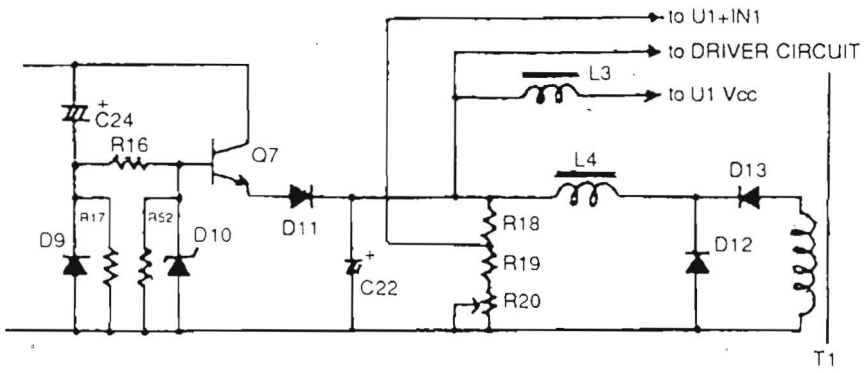
Dead time control is set by an input voltage to the pin 4 (dead time control input) of U1. Its value functions when an input voltage is around 90V AC, and prevents an ON duty value from spreading.



5. Auxiliary Power Circuit for Control

Since the control IC of the switching power source requires a voltage of 7-41 V DC, and FET gate pulse input 5-20 V DC (gate breakdown 20V for K534), an auxiliary power circuit is required to supply those voltages.

Basically, this circuit has only rectification and smoothing circuits; the control IC senses the voltage smoothed there and controls a pulse width in order to keep a constant voltage. Since the IC has not been driven yet at start time, it is necessary to supply power to the control IC until the power circuit starts operating. To this end, a circuit to supply power at start time is connected.

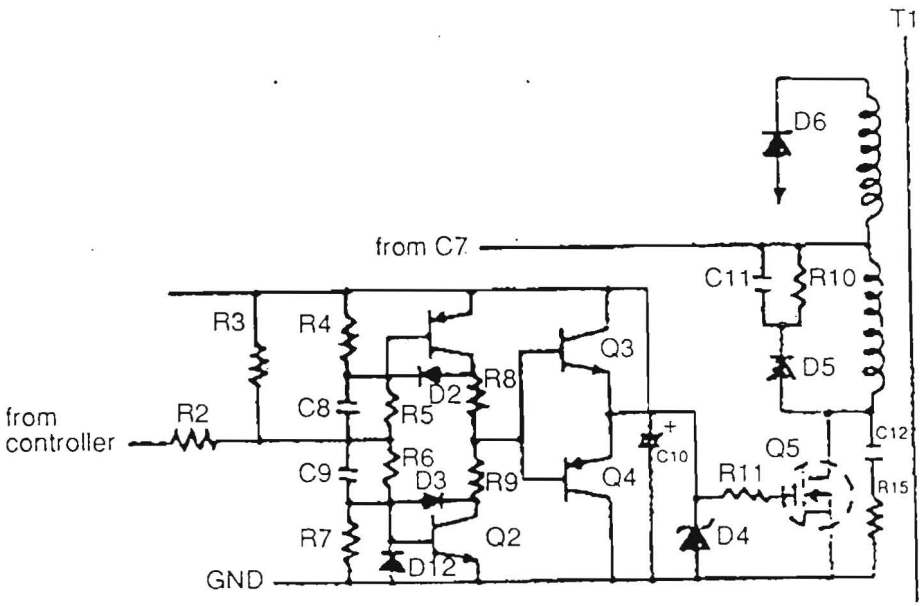


6. Drive and Switching Circuits

In the power MOS FET, switching losses depend on the rise/fall speed at switching ON/OFF time. Therefore, the drive circuit must have high instantaneous power driving capability. There is generally no problem if the control IC has such a driving capability.

However, the MB3759 has the driving capability of only about 250mA; in this case, it is necessary to provide another drive circuit to enhance the current driving capability.

This circuit mainly uses 4 transistors to amplify a current.



3. Output Section

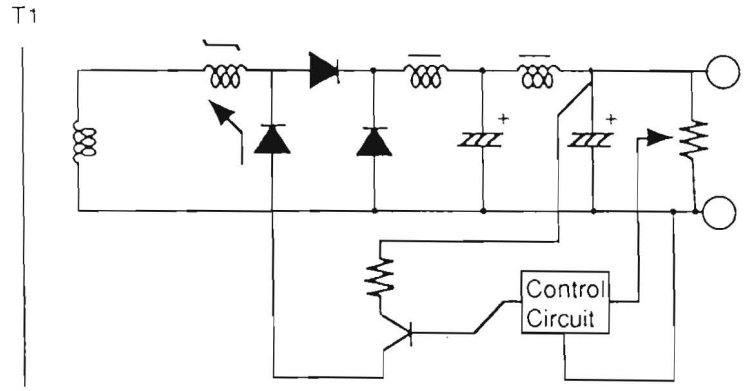
1. Output Power Circuit

The output power circuit has different output control circuits for each output and makes up for an output voltage drop in accordance with the current change of the output section to keep output constant.

The control system used for this circuit is called a magnetic amplifier.

As it is also called a magnetic PWM control system, this system makes use of the characteristics of the magnetic amplifier (magnetic core with rectangular magnetization characteristic) to obtain a constant voltage by adjusting the pulse width of the voltage coming from the input side, as required.

The voltage thus obtained is amoothed through the diode capacitor.



2. Sense Amplifier

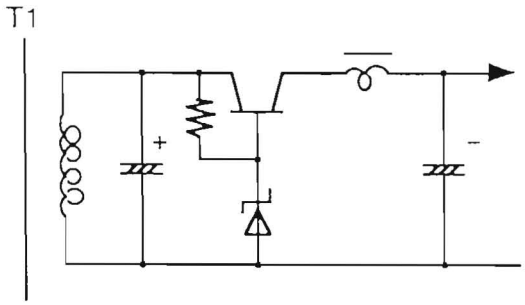
This circuit senses each voltage of the output section, and the output current of the power source for the CRT and logic.

For the CRT and logic circuits, the voltage and current are controlled by the BA728. For the other SG and analog power sources, only the voltage is controlled; TL431 is used for this control element.

3. Auxiliary Power Circuit

Since an OP amplifier is used to control the voltage and current in the CRT and logic power circuits, an auxiliary power circuit is required as a drive power source for this OP amplifier.

This auxiliary circuit consists of simple L and C smoothing circuits.



4. Overvoltage Protective Circuit and Low Battery Circuit

This overvoltage protective circuit is also provided to prevent an overvoltage of supply power from being applied to the CRT and logic sections.

When an overvoltage is generated in the output section and applied to the logic circuit (CRT, printer, etc.), this protective circuit immediately stops the power source to protect the circuit.

After this circuit operated, even if the circuit is restored to a normal condition, it is necessary to bring it up in several tens of seconds through several minutes.

The low battery circuit issues a low battery signal before a logic circuit voltage falls in order to protect it when power is turned off, and causes data to be fetched.

5. AC/DC Power Supply Specifications

Input condition	90-264 V AC (continuous operation) 110-370 V DC (continuous operation)
Output efficiency	70 % or more
Output channels	10 channels
Output	5V (Logic), 12V (CRT, printer, F.D.), ±12V (for SG), +5V, ±12V (for analog Ach), +5V, ±12V (for analog Bch)
Oscillation frequency	130kHz ± 10%
Power drive system	PWM system and magnetic amplifier system
Protective circuits	Rush current limiter, Output overvoltage protective circuit (=5V for logic, +12V for CRT), Output overcurrent protective circuit (for logic and CRT, at I = 20A)

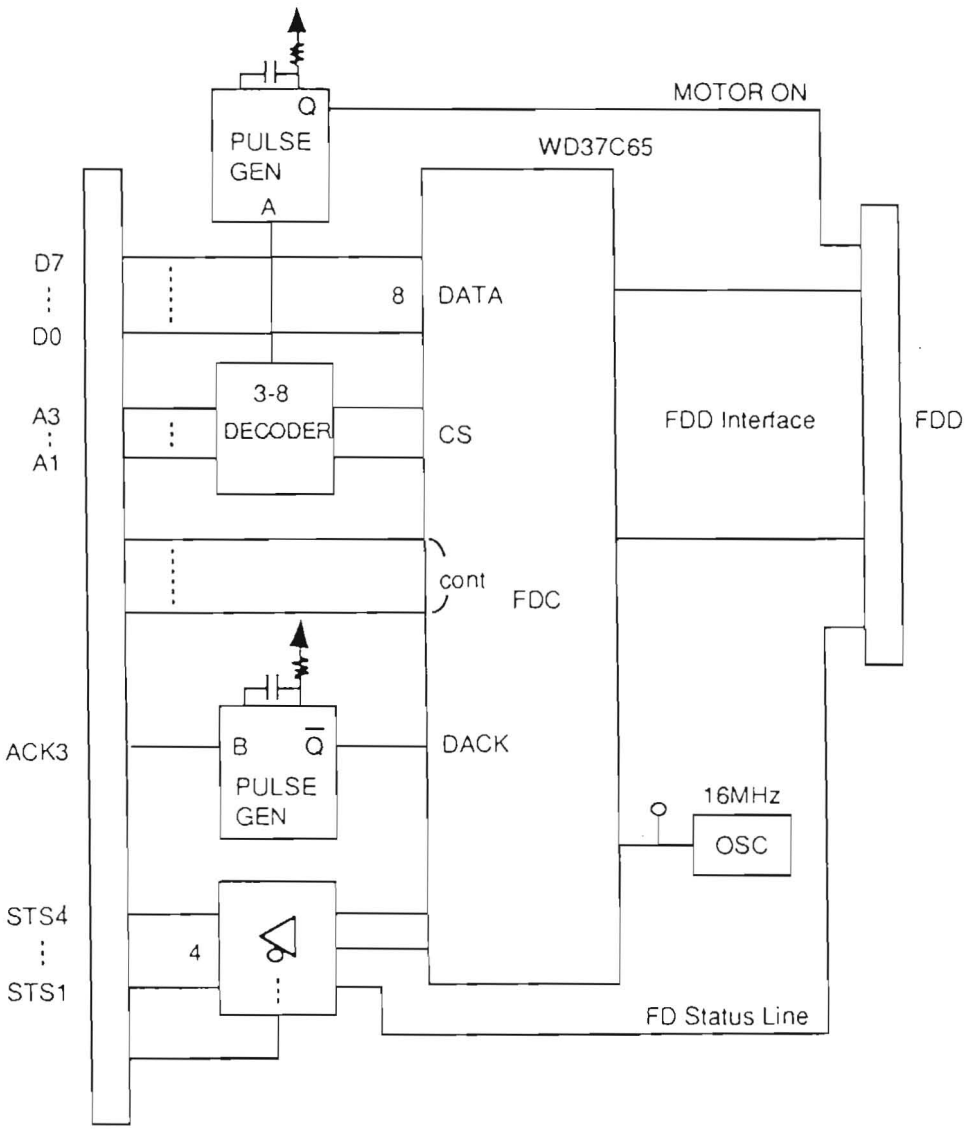
2-3-9 Floppy Disk (Option)

The FDC used is the WD37C65 made by Western Digital. The floppy disk drive is controlled by sending a command to this IC from the CPU.

Data transfer is DMA transfer.

Of the two pulse generators provided, one is connected to the MOTOR ON signal to run the motor for a specified period, and the other one generates the DACK signal at DMA transfer time.

Fig. 20 FDC Section



2-3-10 Video Printer (Option)

The printer unit used is the LTP452B made by Seiko Electronic Industry. This is a thermal printer and uses an in-line head (640 dots).

Since it uses the in-line head, there is only one step motor in the paper feed direction. Therefore, the printer control board has one IC (TD62803 made by Toshiba) to control the paper feed step motor.

Every time one rise edge is issued to this IC from OUT port, the step motor advances one step. Since the maximum speed of the step motor is 200 pps, intervals of 5 ms is generated by the step rate generator and monitored at the IN port.

PAPER EMPTY and HEAD UP/DOWN signals are coming from the printer unit and monitored at the IN port. These signals are also inputted to the decoder where HEAD STROBE is generated. When conditions are not met, power to the head is prohibited hardwarewise.

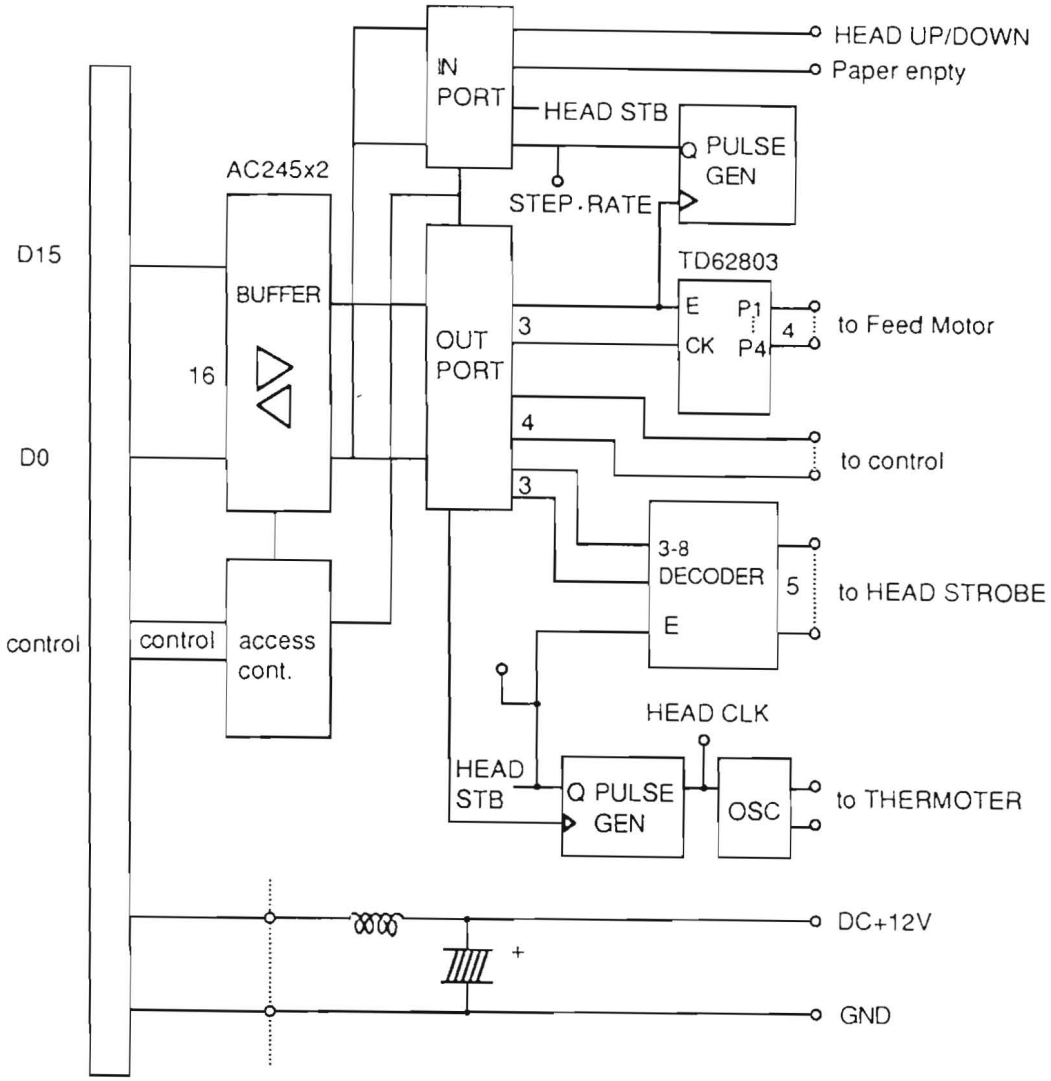
As the in-line head is connected to the output of the shift register inside the printer unit, printing data is serially transmitted 640 bits from the board and set in the shift register located inside the head.

Next, when you turn on the head to print, do so sequencing in 5 times because the head is of 128 dots.

A head power-on time is determined by the head strobe pulse generator.

Since the power-on time must be changed in accordance with a head temperature, the thermistor attached to the head is used to make a transmission circuit to perform automatic compensation so that the pulse width will correspond to the head temperature.

Fig. 19 Printer Section



2-3-11 1M-/2M-Word Memory Card (Option)

The 1M-/2M-word memory card is an extension memory with 1M-word/2M-word DRAM.

If this option is installed, the 2CH FFT main memory is extended and various functions are added.

The 1M-word memory card installs 16 1-Mbit (256K x 4) DRAMs, and 2M-word 32 of them.

The DRAMs are controlled by the MB1430 (made by Fujitsu) which employs CAS Before RAS Refresh. As a clock, D25 MHz axynchronous with the CPU is inputted to realize high speed.

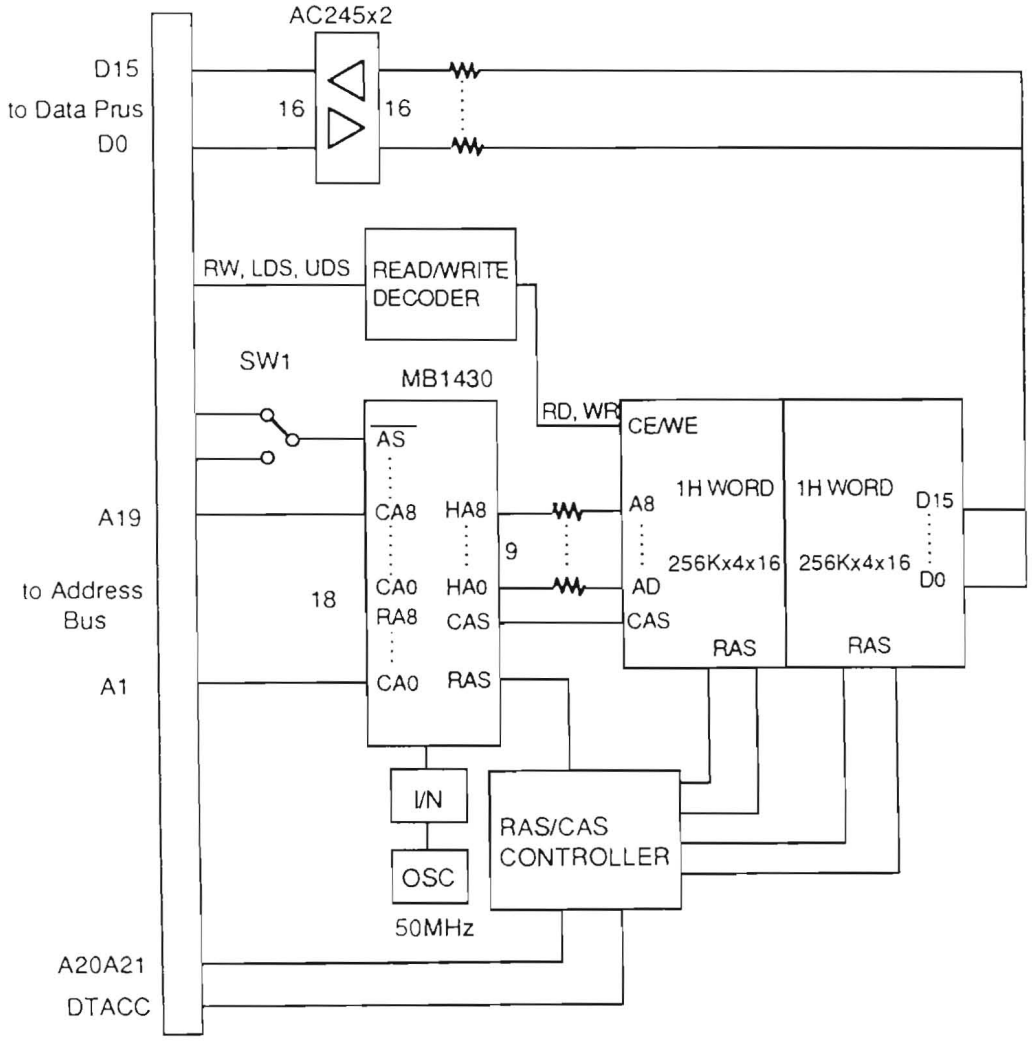
A standard option slot is J6, but when you install two cards, the 2nd one may be inserted into J3 or J5. The 1st one must be in J6.

There are slide switches on the board. When installing two cards, set them to 0 and 1, respectively.

The following shows memory addresses depending on a combination of the slide switch setting and memory capacitance.

	1st Card (Switch 0)	2nd Card (Switch)
1M and 1M	600000~7FFFFF	A00000~BFFFFF
1M and 2M	600000~9FFFFF	A00000~BFFFFF
	600000~7FFFFF	A00000~DFFFFF
2M and 2M	600000~9FFFFF	A00000~DFFFFF

Fig. 18 Extended DRAM Section



2-3-12 512 K-word CMOS Memory Card (Option)

The 512 k-word CMOS memory card is an extension memory with 512 k-word SRAM.

If this option is installed, the 2ch FFT main memory is extended and various functions are added.

The SRAM contains 32 256 Kbit (32 K x 8) memorys; in total, 512 k-word.

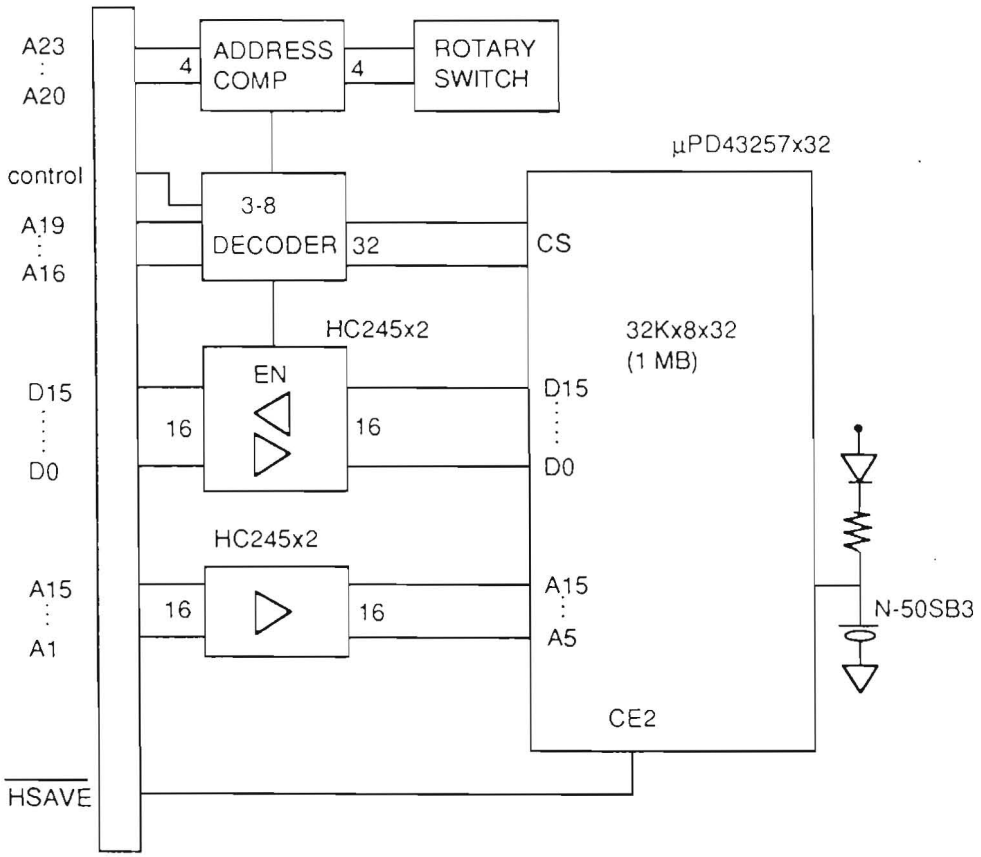
As it is backed up by nickel-cadmium batteries, data remains even if power is turned off.

It is inserted into the option slot J5 or J6. When installing it together with the extension DRAM, insert into J5.

SRAM memory addresses range from 600000 to Effiff by 1 MB. When installing together with the extension DRAM, the memory addresses must be set not to duplicate those for the DRAM.

For address setting, the number indicated by the rotary switch on the board shows the uppermost 4 bits of address. Normally, set to "E".

Fig. 20 Extension SRAM Section



1. ON/OFF Circuit

2-3-13 High-Speed Operation Card (Option)

The high-speed card is an option board to execute internal operations at a high speed. Installation of this board improves a processing speed.

The IC used for executing operations is the DSP PD77230 made by Nichiden and the 32 KB Static RAM is placed in the address space.

So that this Static RAM can be accessed from both CPU and DSP of the 2ch FFT, their respective buses are connected through a tri-state buffer.

Therefore, it is impossible to access from both at the same time.

The access arbitor adjusts an access from the main CPU and DSP to control the buffer so that the buses do not collide.

As the DSP data bus is 32 bits, the main data bus (16 bits) is doubly expanded and connected to the RAM.

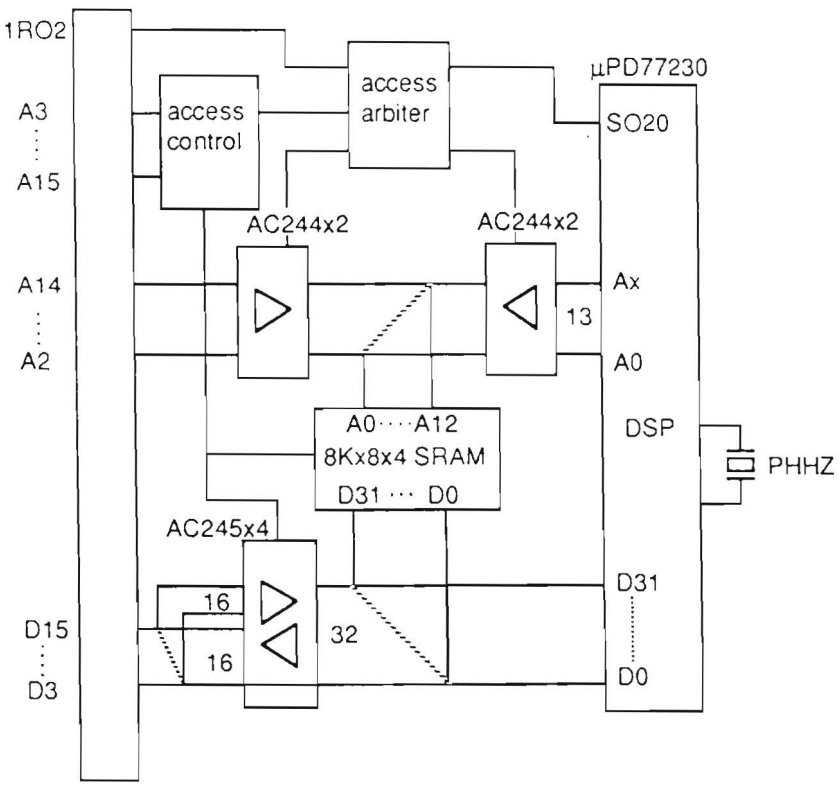
The main CPU first writes the program and computed data in the SRAM.

Next, it applies an interrupt to the DSP via the access arbitor to start the DSP and separate the bus from the main CPU itself.

The DSP computes data, and upon its completion, it applies an interrupt to the CPU to separate the bus.

The main CPU transfers data from the RAM.

Fig. 21 DSP Section



2-3-14 Signal Generator Card

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1. General Description

This card is a programmable signal generator.

It can outputs the waveform set by the soft key of the main body.

The following outlines the specifications of this card.

SG Card Specifications

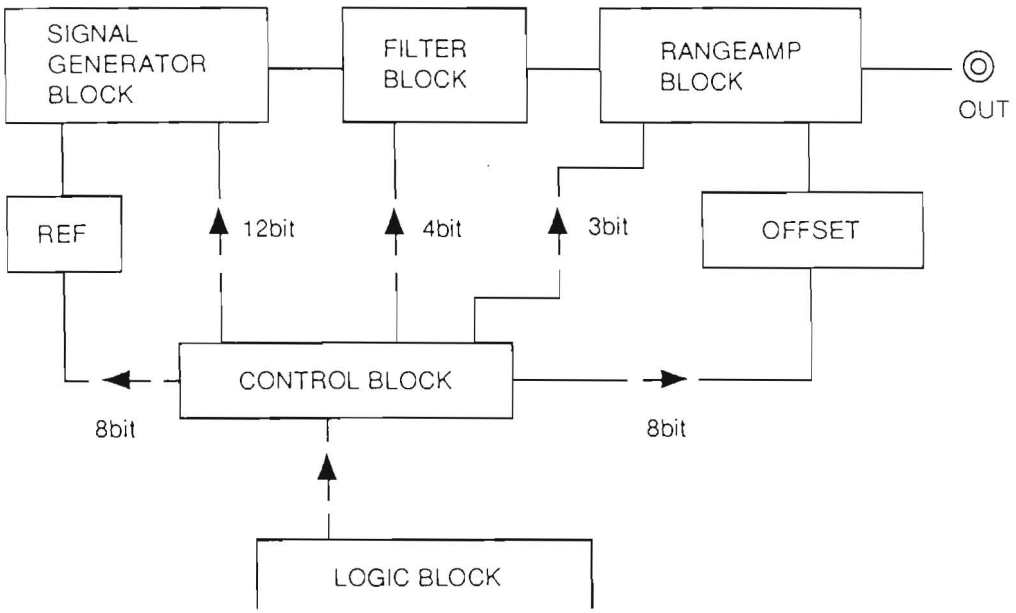
Waveform generator;	D/A resolution	12 bits
	Data format	2's complement
	Sampling rate	512kHz max. Sampling is performed twice the A/D sampling frequency.
Control section;	D/A resolution	8 bits
Filter		Tertiary LPF, In-band ripple : ±0.5 dB max., up to 100kHz through 20Hz, 12-point changeover interlocked with the frequency range of the main body
Output voltage		±5 V max., ±5 V offset voltage applicable to the output waveform
S/N ratio		60 dB typical
Output waveforms		Since,square, ramp Continuous waveforms such
as		since, square, ramp, impulse, multisine, swept since, etc. I-frame one-shot waveform by a single shot, Regeneration of analog waveforms of various memory data

2. Configuration

This card mainly consists of 1) waveform generator, 2) filter, 3) range amplifier, 4) control, and 5) logic blocks.

The following figure shows an overall block diagram.

Fig. 1 SGcard Block Diagram



3. Description of Functionings

1) Waveform Generator Block

The waveform generator block converts (D/A) 12-bit waveform data from the logic block and outputs as an analog waveform.

The D/A converter used is a unipolar, current output type. It is turned into bipolar output by giving an offset current from the external.

Thus, the D/A converter outputs +2mA current when the waveform data is at +full scale, 0mA when at 0, and -2mA when at -full scale.

The reference of this D/A converter is programmable, can be set with the full scale of 4 V and 8-bit resolution.

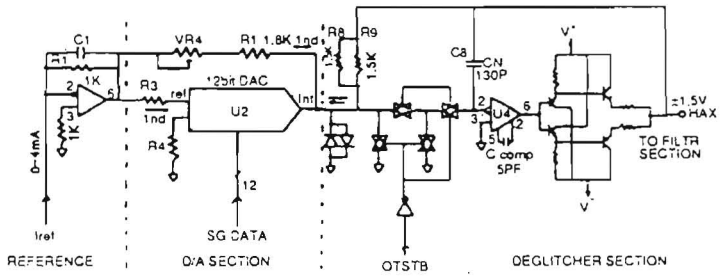
The D/A converter output "±2mA" is made when all the reference data are "1" (full scale).

Naturally, the full scale of the D/A converter decreases as this reference does.

The current output of the D/A converter is i-v converted through the deglitcher circuit, and a waveform voltage of ±1.5V max. is outputted.

The deglitcher circuit is a circuit is a circuit which, in order to eliminate glitches appearing in D/A output when D/A data changes, eliminates them, holding previous D/A output until this D/A output is stabilized.

It is a sampling state when the signal DTSTB from the logic block is "1", and a holding state when it is "0".



2) Filter Block

The filter used is a tertiary Chevishev type low-pass filter.

It compensates the in-band frequency characteristic of the waveform generating D/A converter and attenuates high-frequency components.

Although a filter gain is 0 dB, a peak of +0.55 dB is given in a cut-off frequency in order to compensate the D/A converter characteristic mentioned above.

The out-band suppression ratio of the filter itself is −46 dB.

With this combined with the out-band frequency characteristic of the D/A converter, the SG card has a typical out-band suppression ratio of −60 dB in total.

A transmission zero point is located at 4.5 times the cut-off frequency (frequency range). For a frequency range, it is changed over at 12 points by a 4-bit control signal (FLT1-4) from the control unit in 1-2-5 sequence, being interlocked with the frequency range of the main body, ranging from 100kHz to 20Hz.

A minimum range of 20 Hz is set in case of SG-off or DC output.

The frequency characteristic of the filter and list of frequency ranges follow.

Fig. 2 FILTER SECTION

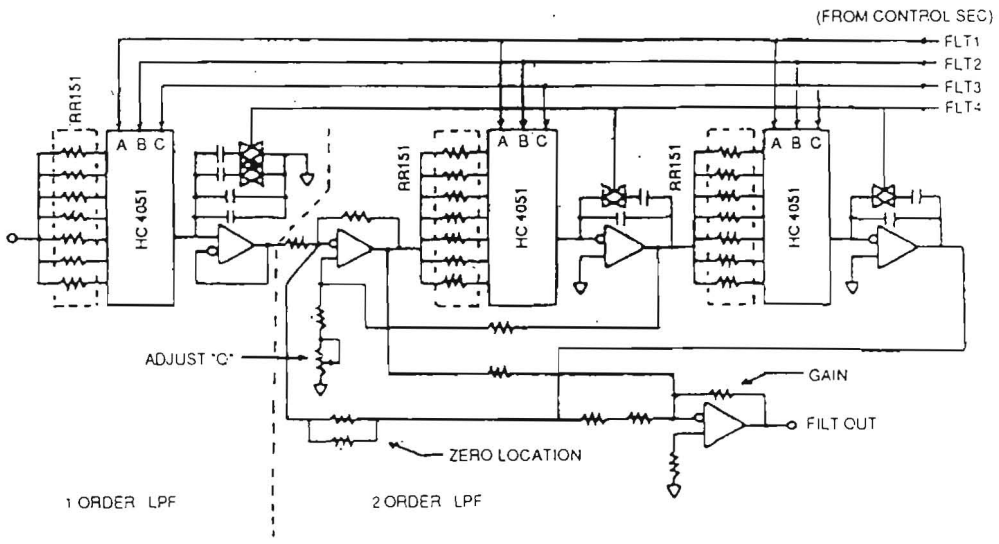


Table.1 Frequency Range and control data

FREQ RANGE	FLT 4	FLT 3	FLT 2	FLT 1
100 KHz	0	0	0	0
50 KHz	0	0	0	1
20 KHz	0	0	1	0
10 KHz	0	0	1	1
5 KHz	0	1	0	0
2 KHz	0	1	0	1
1 KHz	1	0	0	0
500 Hz	1	0	0	1
200 Hz	1	0	1	0
100 Hz	1	0	1	1
50 Hz	1	1	0	0
20 Hz	1	1	0	1

Frequency Characteristic of Filter

The figure below shows the frequency characteristic at cut-off frequency fc = 5kHz.

The FFT simplex does not allow observation of this filter characteristics (cut-off frequency, transmission zero point) because it is interlocked with the frequency range of the main body.

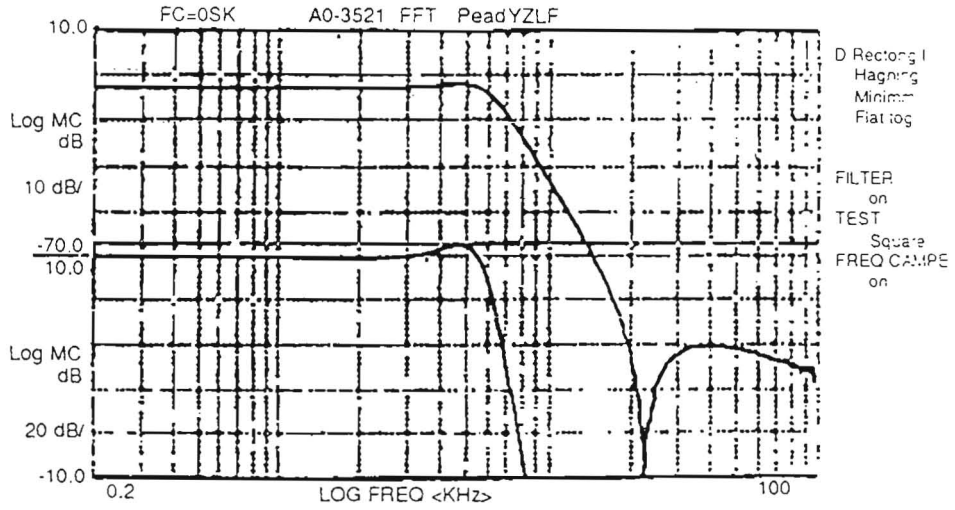
It is necessary to observe with another FFT analyzer.

The in-band enlarged view and out-band frequency characteristic are shown together.

A gain of 1 div has been adjusted in-band; 2 dB/div.

The transmission zero point is 4.5 fc, inband ripple = +0.55 dB max.

Fig. 4 FILTER CHARACTERISTIC



3) Range Amplifier Block

It amplifies or attenuates waveform output from filter. Here, amplitude is set by 10 dB step.

Finer setting is done by changing the reference of the D/A converter in the signal generator in 1).

Also, the output waveform of the range amplifier can be given an offset voltage of ±5V max. with 8-bit resolution.

This also allows only either of positive and negative polar output waveforms.

The following shows setting data for each range.

Table. 2 RangeAmp Gain and Control Data

GAIN	RNG 1	RNG 2	RNG 3
+10 dB	0	0	0
0 dB	0	0	1
-10 dB	0	1	0
-20 dB	0	1	1
-30 dB	1	0	1
-40 dB	1	1	0
-50 dB	1	1	1

4) Control Block

Serial data from the main board of the main body are converted into parallel data and used as data for the control unit (48 bits).

The breakdown of the analog data is 8-bit reference data (RDT0-7), 8-bit offset data (ODT0-7), 4-bit filter frequency range data (FLT1-4), and 3-bit range amplifier data (RNG1-3), and that for the digital data is 1-bit single action (MODE), 15-bit SG-CLK frequency division, 1-bit memory scan (RUN), 1-bit address clear (ACL), and 4-bit memory size data (MS0-3).

Fig. RANGE AMP SECTION

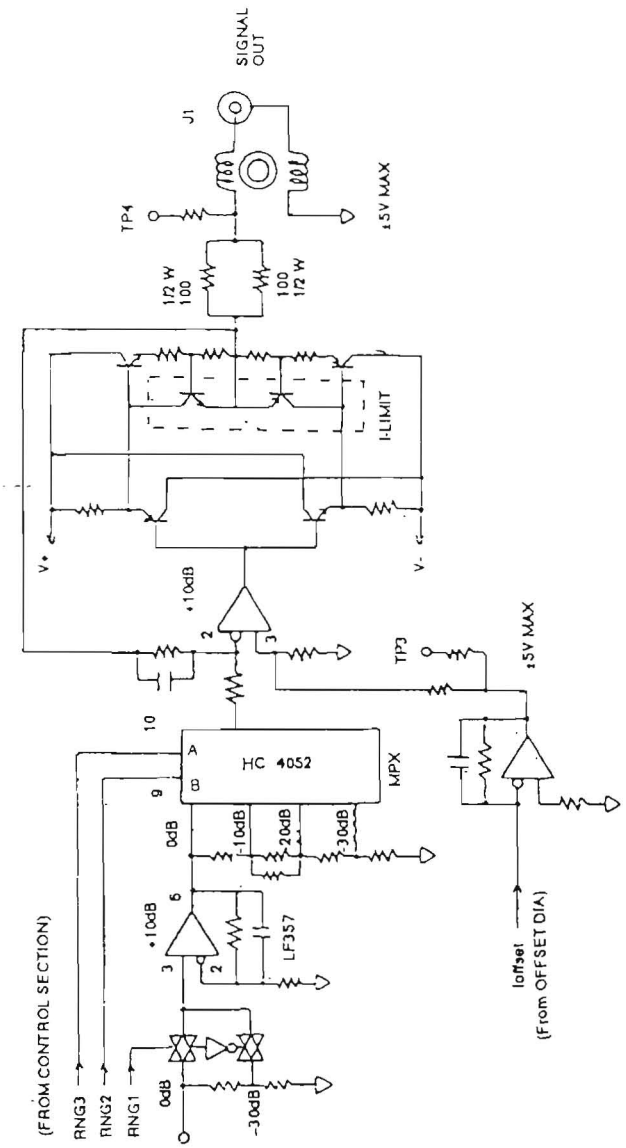
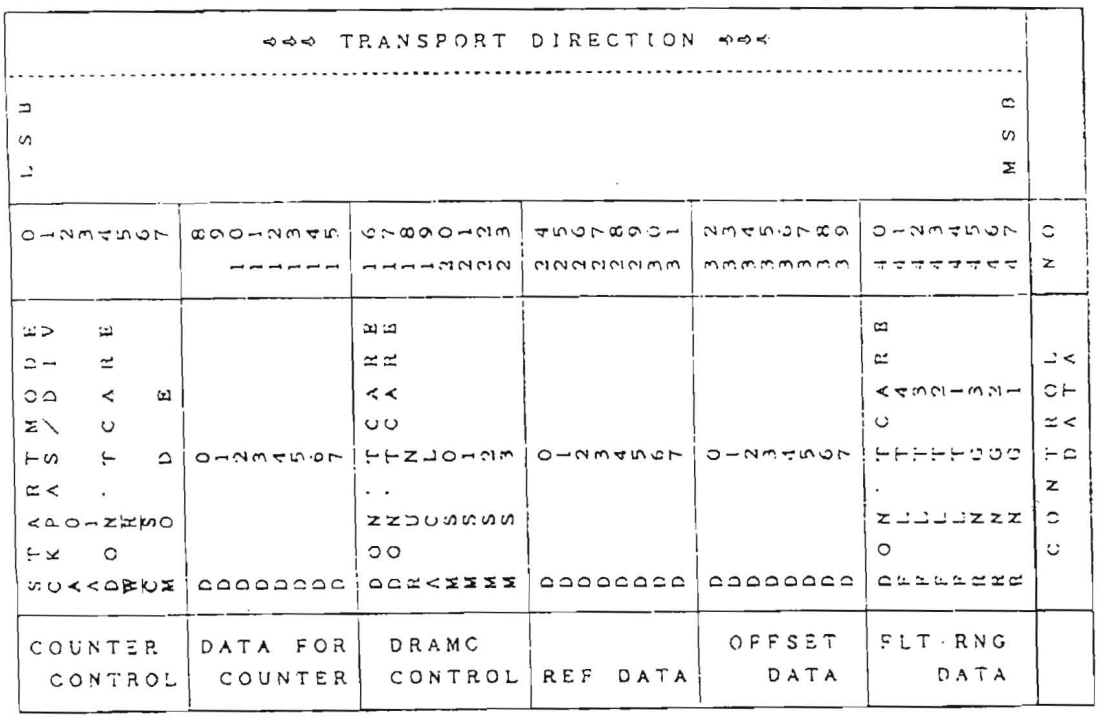


Table. 3 Memory Size and Control Data

MEMORY SIZE	MS 0	MS 1	MS 2	MS 3
256 wd	0	0	0	0
512 wd	1	0	0	0
1 kwd	0	1	0	0
2 kwd	1	1	0	0
4 kwd	0	0	1	0
8 kwd	1	0	1	0
16 kwd	0	1	1	0
32 kwd	1	1	1	0
64 kwd	0	0	1	1
128 kwd	1	0	1	1
256 kwd	0	1	1	1
512 kwd	1	1	1	1

Table. 4 SG Serial Data Format



5) Logic Block

The waveform data 16-bit from the main board is transferred to the SG internal memory by accessing the data input port of the SG (address: 00ffff0h).

In the SG card, when the waveform data is fetched into the internal memory, the address generator increments the address.

To transfer, therefore, you only need to access the identical address.

The internal memory has two memory blocks, each of which has a capacity of 12 x 256 Kbits; totaling 12 x 512 Kbits.

The memory is controlled by the DMA controller. The size of the memory used can be specified by sending 4-bit size data (MS0-3) to the address generator (256-512 Kword).

The data to control the timing control logic and address generator are transferred from the main board as serial data, converted into parallel data inside the SG card, and sent to each block of the analog circuit's controller.

While the waveform data is being written into the internal memory, the mode is switched from RUN to CPU and the data register is cleared to all 0. When the mode is switched from RUN to SCAN, the address continues to be incremented synchronously with SG-CLK, the waveform data is outputted from the memory into the data register.

The address generator forms a ring counter which increments the address from 0 again when a specified memory size is exceeded.

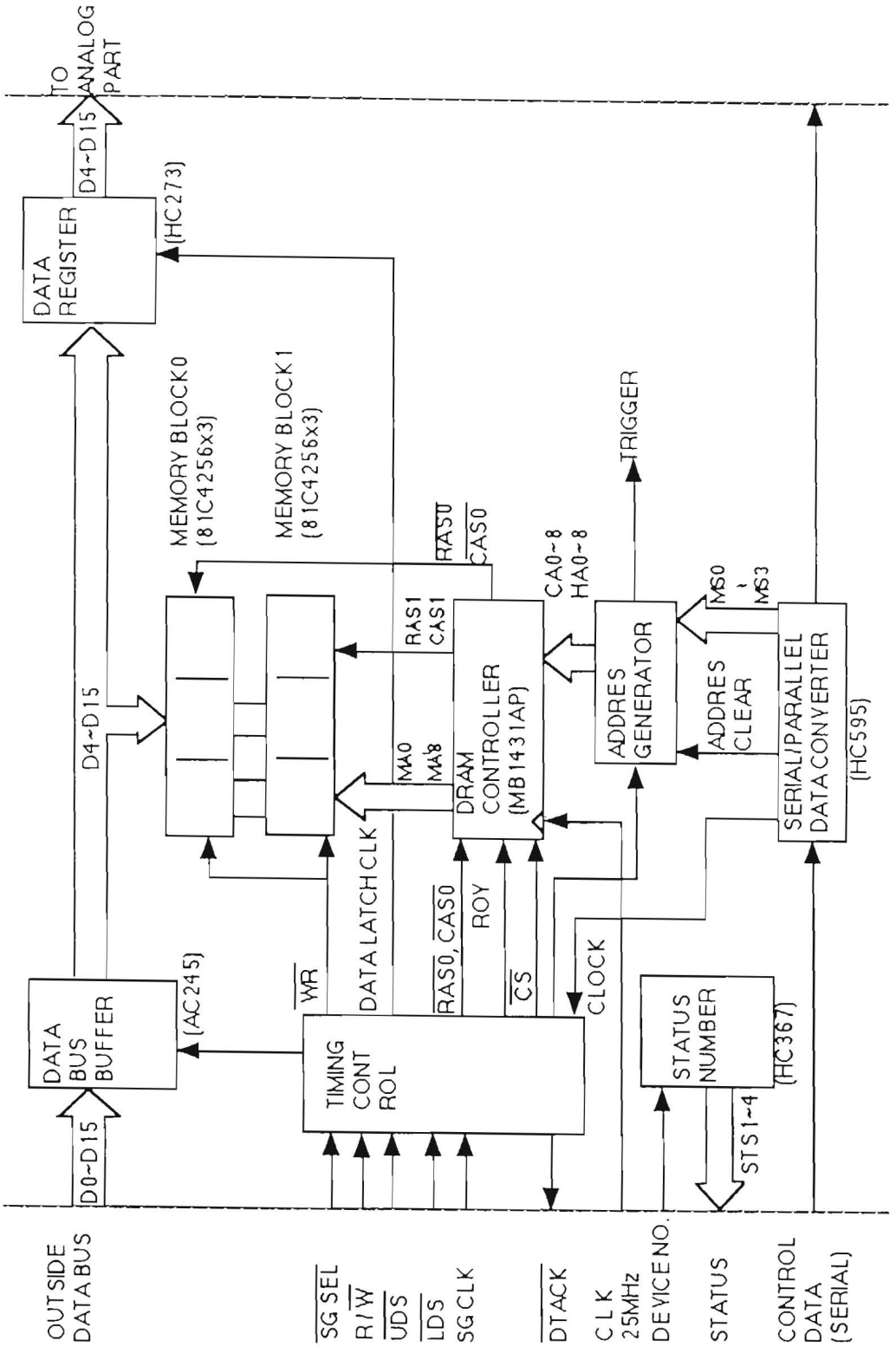
Since SGCLK is two times A/D sampling CLK, for example, in order to output the data from the SG board 1,024 points worth of time data from the SG board, 2,048 points worth of data must be written in the memory in advance.

Since the 100kHz version uses the digital filter in a range of 100Hz or less, and the 20kHz version uses it in a range of 20Hz or less, SG-CLK does not change. So, it is necessary to frequency-divide SG-CLK on the part of the SG card. To frequency-divide SG-CLK, the CH0 of the μPD71054G (programmable timer/counter) is used.

Also, there are two output modes; the "continuous output mode" which scans the memory and continuously outputs signals, and the "single mode" which outputs one frame worth of signals only when the soft key of the main body is pressed.

In the single mode, pressing the "Single" key clears the address and continuously accesses the memory address 0. The access to the address 0 continues in a standby state until the "Single" key is pressed again. To return to the continuous output mode, press the "Normal" key.

Fig. LOGIC SECTION BLOCK DIAGRAM



2-3-15 Capacitor MIC Card (option)

General Description

The capacitor MIC card is an option for the 2ch FFT. This allows you to measure a sound by connecting a Lyon or B&K capacitor microphone.

OP-11 : Exclusive for the Lyon capacitor microphone

OP-11A : Exclusive for B&K capacitor microphone

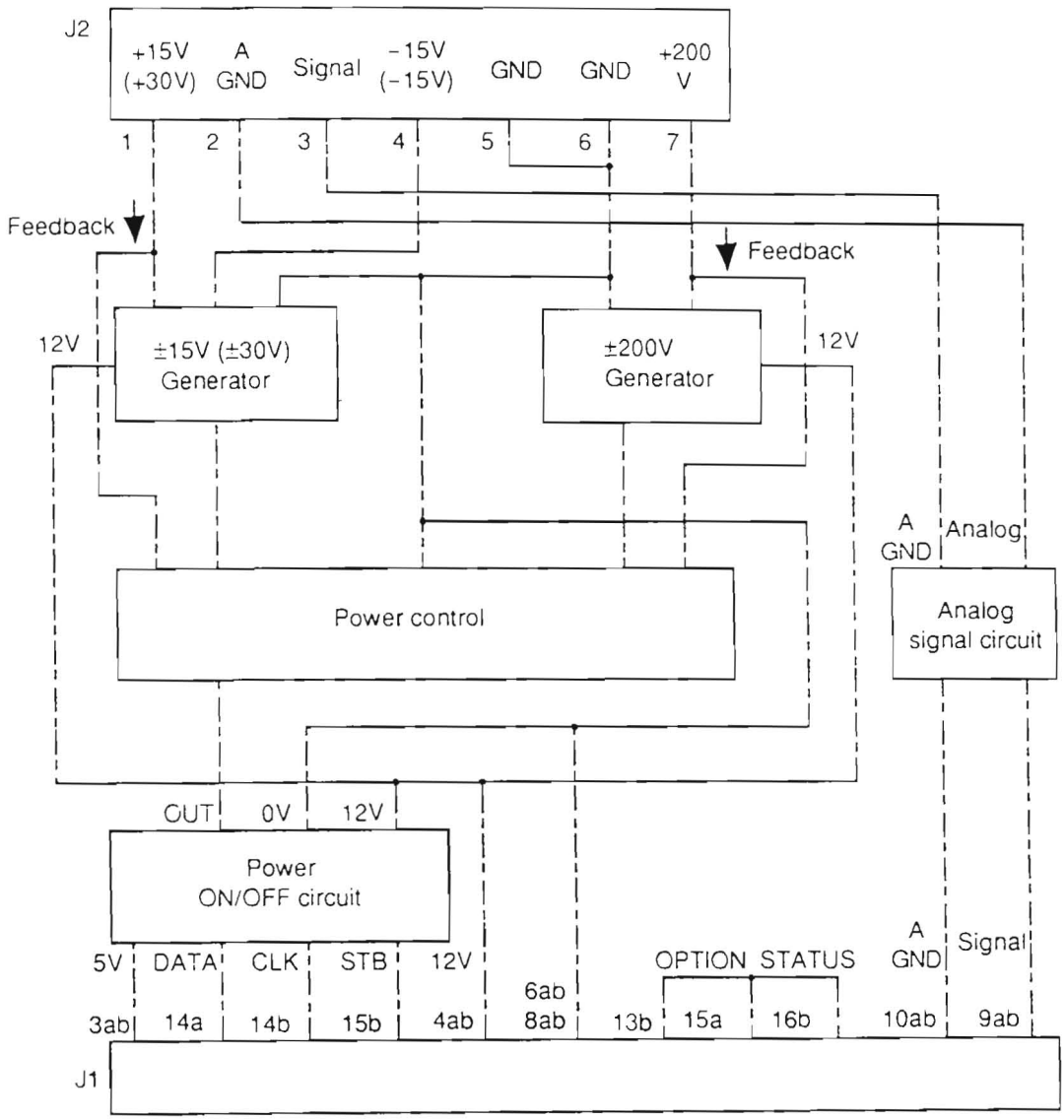
PZ : 2244 Capacitor Microphone Board

This board is a DC/DC converter to generate a voltage required for driving the capacitor microphone. It boosts a 12V DC voltage supplied from the A/D board to +200V and ±15V (+28V: B&K).

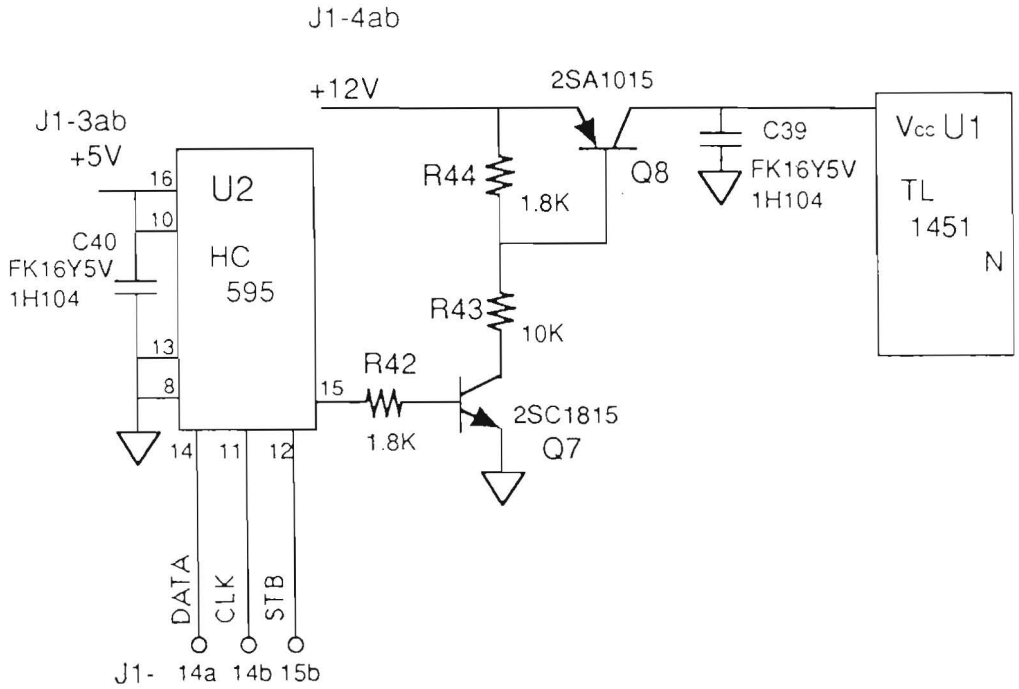
This board consists of the following circuits:

1. ON/OFF circuit
2. Power control
3. 200V generator
4. ±15V generator (±30V output allowed)
5. Analog signal circuit

Capacitor MIC Card Block Diagram



1. ON/OFF Circuit

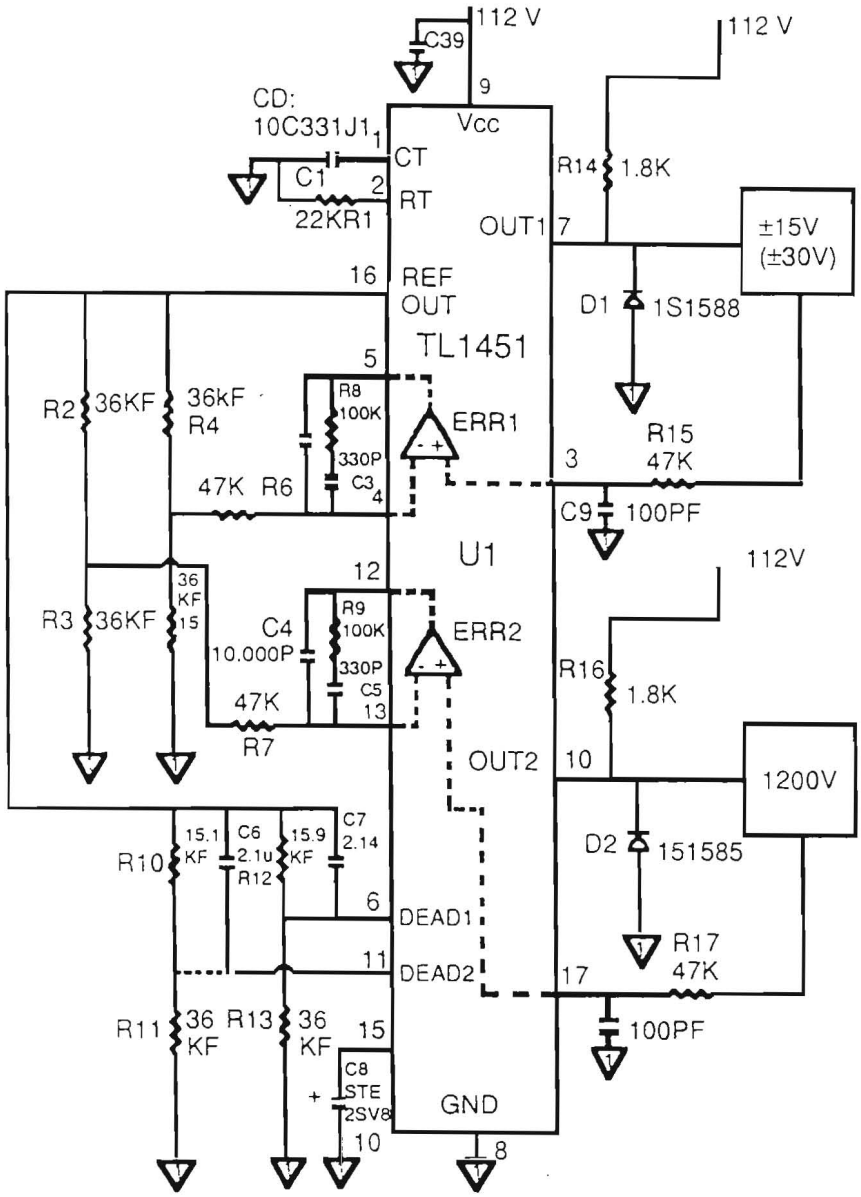


As shown above, this circuit turns on/off Vcc of U1 (TL1451N: switching current controller) by means of software by using U2 and turns on/off +200V and ±15V (±30V) outputs.

When MIC INPUT is turned on by operating the key of the 2ch FTT proper, the pin 15 of U2 is set to +5V (High), +12V is supplied to Vcc (pin 9) of U1, and power for the microphone (+200V, ±15V) is outputted.

When MIC INPUT is off, the pin 15 of U2 is set to 0V (low) and power for the microphone is turned off.

2. Power Control



As shown in the left figure, U1 (TL1451N) controls the 2 channels of the switching power source (±15V, +200V).

An oscillation frequency is about 120kHz, determined by R1 and C1.

(Should be 100kHz or more.)

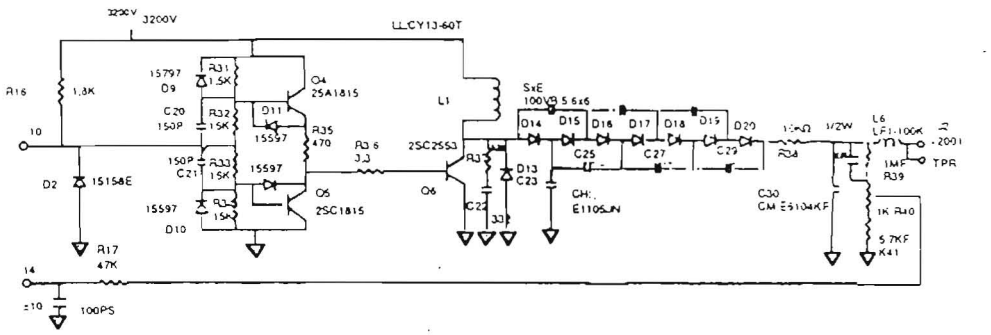
When output is short-circuited, oscillation stops for both 2 channels.

To restart oscillation, you must turn off Vcc of U1 once.

Turn off "MIC INPUT" once by operating the key of the FFT proper and turn it on again. Oscillation restarts.

Note: When intermittent oscillation is performed (output seems to have more ripples), check whether an output resistance load is given properly. Also, pay attention to a feedback loop (whether C9 and C10 values are normal).

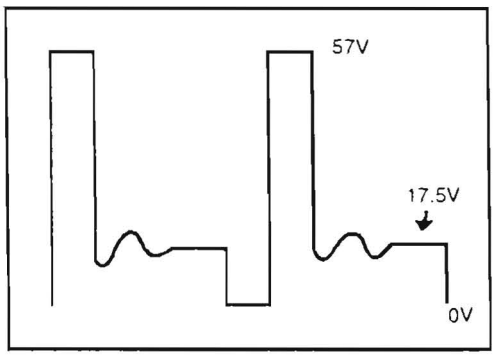
3. 200 V Generator



The above circuits boosts 12V DC to 200V DC.

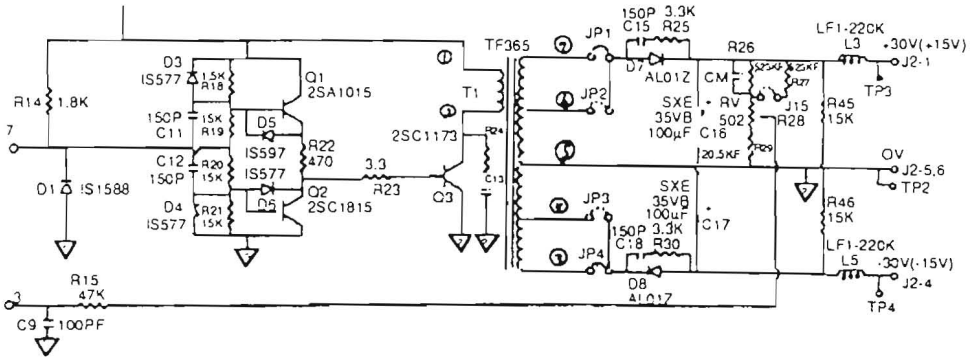
Energy is generated to L1 by turning on/off the transistor 2SC2553 of Q6.

As a result, a waveform with a peak of about 57V takes place at the collector Q6. Next, the voltage is boosted 3.5 times by D13-D20 and C23-C29, and +200V is outputted. The output voltage is determined by a ratio of the resistors R39-41 and adjusted by the control knob R40. (The output voltage is stabilized by the feedback loop.)

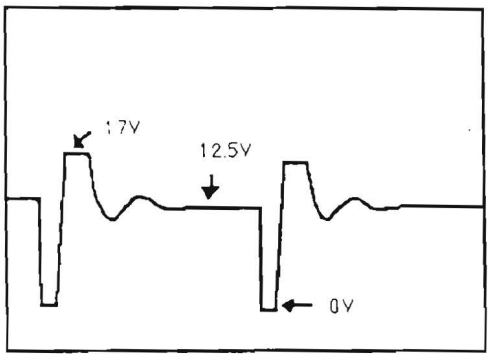


Voltage Waveform of Collector Q6

4. ±15V Generator (±30V Output Allowed)



The above circuit boosts 12V DC to ±15V (±30V) DC. Energy is generated to the transformer TF365 of T1 by turning on/off the transistor 2SC1173 of Q3 by the control of TL1451.



Voltage Waveform of Collector Q3

When you want to output ±15V, connect JP2, JP3, and JP5 with jumper wires, and open JP1 and JP4.

When you want to output ±30V, connect JP1 and JP4 with a jumper wire, and open JP2, JP3, and JP5.

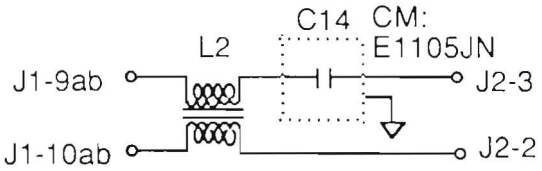
To adjust the output voltage, use the control knob RV502 of R28.

Adjust to the following values, respectively:

For the Lyon microphone : ±15.0V(±0.5V)
For B&K microphone : ±28.0V(±0.5V)

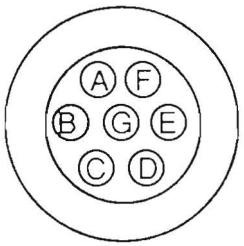
5. Analog Signal Circuit

The analog signal circuit supplies an analog signal from the microphone to the analog board (PZ:2066) by AC coupling.



• Connector Pin Layout for Microphone

Lyon capacitor microphone connector



A : +15
B : GND
C : Analog signal input
D : -15V
E : GND
F : N. C
G : +200V

☆ Applicable connector (opponent of the microphone input connector)

Type	:	TC1108-12A10-7M
Maker	:	Tajimi Musen Denki K.K.

• Inspection Jigs

Jigs for OP-11

A	:	+15 V
B	:	GND(OV)
D	:	-15 V
C	:	Analog
E	:	GND(OV)
F	:	N.C
G	:	+200 V

2-3-16 Envelope Card

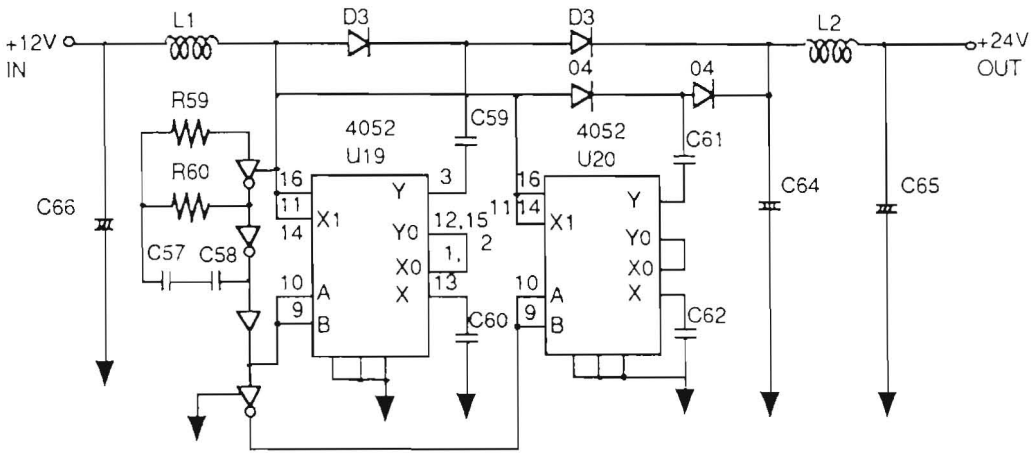
1. General Description

For a signal which changes amplitude as if it is modulated, its features can be seen even in an amplitude change time, in addition to a frequency which is its basis. Therefore, the features of the signal waveform can be represented by obtaining the envelope of that signal.

It also has a function to supply a current to an acceleration sensor with amplifier built in; 2 mA and 0.5 mA.

2. Description of Circuits

24V Generator Block



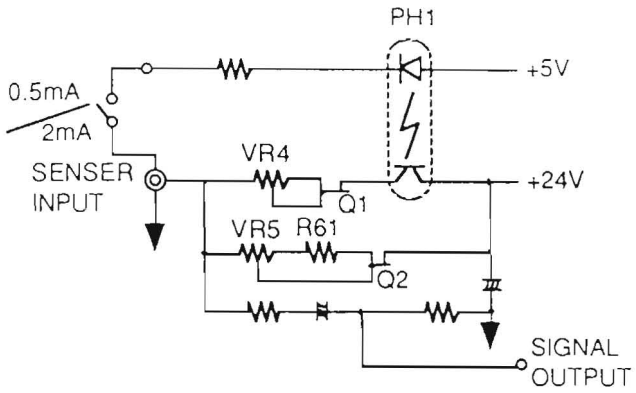
Its operational principle is the same as the charge pump.

Two capacitors are charged in parallel, and then, they are discharged in series. this action provides an output twice larger than an input.

The circuit shown in the left figure has two of the above-mentioned circuit, that is, 4052 arranged in parallel. Since one of them is being discharged when the other is being charged, the same action results as full-wave rectification of the rectification circuit.

At this time, changeover is done by the transmission circuit using the left 4001 on the circuit shown in the figure above.

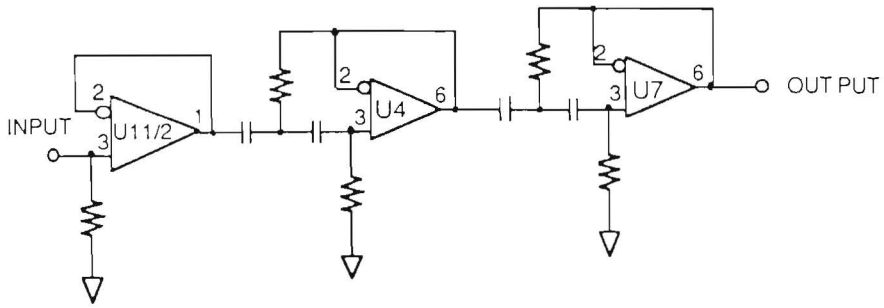
Power Supply Block



This circuit produces 0.5mA and 2mA currents to be supplied to the acceleration sensor. The circuit portion, which does not contain a photocoupler in place of a switch before the FET, produces the 0.5 mA constant current, and the other portion produces the 1.5mA constant current.

When obtaining the constant current, it is produced by turning on the photocoupler and adding 0.5mA and 1.5mA.

HPF Block



This circuit provides pre-processing before enveloping. Enveloping aims at obtaining the envelope of the signal whose amplitude such as a modulated wave.

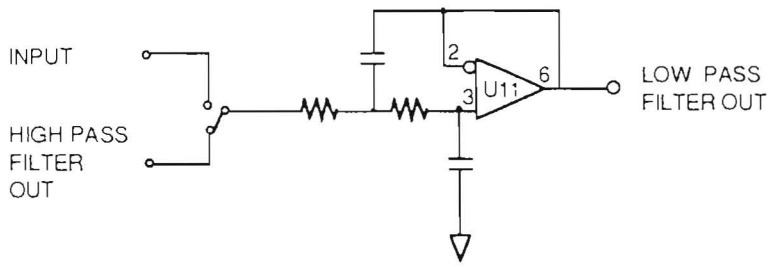
If a low-frequency signal is on the modulated wave from the beginning the components of the low-frequency wave are contained even at the time of enveloping, and they may not be distinguished from those of the envelope.

To avoid this problem, extra low-frequency wave components are cut off by HPF in advance. The circuit shown in the left figure is a general positive feedback type active filter.

There are 9 kinds of cut-off frequencies; 20kHz, 10kHz, 5kHz, 2kHz, 1kHz, 500Hz , 200Hz, 100Hz, and 50Hz. A constant configuration is on a 3 x 3 bases; 3 kinds for capacitors, and 3 kinds for resistors.

With this configuration, changing one of the constants (for capacitors or resistors) automatically affects 3 ranges. This option has two of this circuit one over another to obtain a biquadratic attenuation amount of 24 dB.

LPF Block



This circuit also provides pre-processing before enveloping.

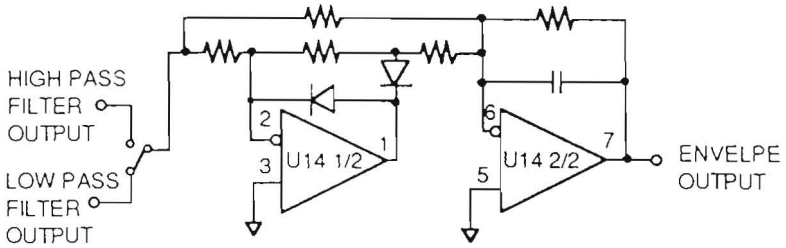
It cuts off extra high-frequency components before enveloping.

The circuit shown in the left figure is a general positive feedback type active filter.

There are 3 kinds of cut-off frequencies; 50kHz, 20kHz, and 10kHz.

This circuit is provided only one and obtains a binary attenuation amount of 12dB.This LPF can be used as BPF by combining it with the above HPF and the anti-aliasing filter of the FFT proper.

Envelope Block



This part can be referred to the main body of this option, Its operational principle is the same as that of the detection circuit of the AM radio.

This circuit consists of two parts;' one is a full-wave rectification circuit called an absolute value circuit, and the other is an integration circuit. It is normally deflected plus/minus.

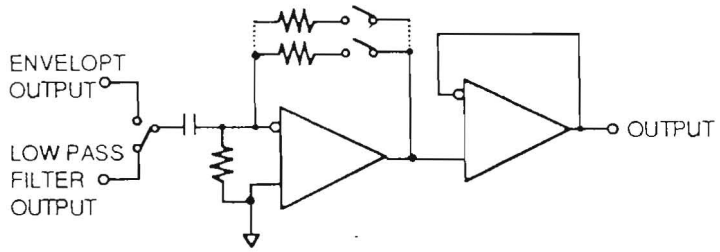
If a modulated wave is put through the integration circuit as it is it is offset in mutual directions and nothing is outputted.

Therefore, it is necessary to perform full-wave rectification.

Next, the envelope can be obtained by putting the signal obtained there through the integration circuit and cutting off high-frequency components.

The time constant of the integration circuit is interlocked with the HPF's switching circuit.

Amplifier Block



The signal put through the enveloping circuit is relatively small.

When its size is not so different from the computational noise level of the FFT, it is very difficult to distinguish it.

There, a gain of 20 dB must be obtained as required.

2-3-17 Comparator Output Card

1. General Description

This card is designed to output to an external device the results of comparison done at the 2ch FFT.

2. Specifications

Comparator output

No. of relay contacts : 32

1 = Make (Go)

0 = Break (NG), (OFF)

Electrical specifications

Device used	:	Photo MOS relay AQV203 made by Matsushita
Absolute maximum load voltage	:	100V
Continuous load current	:	150mA
Peak load current	:	600 mA (100ms)
Output loss	:	180mW
Withstand voltage	:	200V AC
Total power dissipation	:	210mW
ON resistance	:	8 maximum
Leak current at break time	:	1A (1 = 250V)

Output connectors

Connector used	:	JI: 365P064-AG (with JI360A2)
Opponent connector	:	FCN-361J064-AG (Fujitsu) + FNC-360C064-B (Fujitsu)

Pin connection

Pin	1	2	3	4	5	6	7	8	9	10	11
A	+D0	+D1	+D2	+D3	+D4	+D5	+D6	+D7	+D8	+D9	+D10
B	-D0	-D1	-D2	-D3	-D4	-D5	-D6	-D7	-D8	-D9	-D10

Pin	12	13	14	15	16	17	18	19	20	21	22
A	+D11	+D12	+D13	+D14	+D15	+B0	+D16	+D17	+D18	+D19	+D20
B	-D11	-D12	-D13	-D14	-D15	-B0	-D16	-D17	-D18	-D19	-D20

Pin	23	24	25	26	27	28	29	30	31	32
A	+D21	+D22	+D23	+D24	+D25	+D26	+D27	+D28	+D29	+B1
B	-D21	-D22	-D23	-D24	-D25	-D26	-D27	-D28	-D29	-B1

Functioning

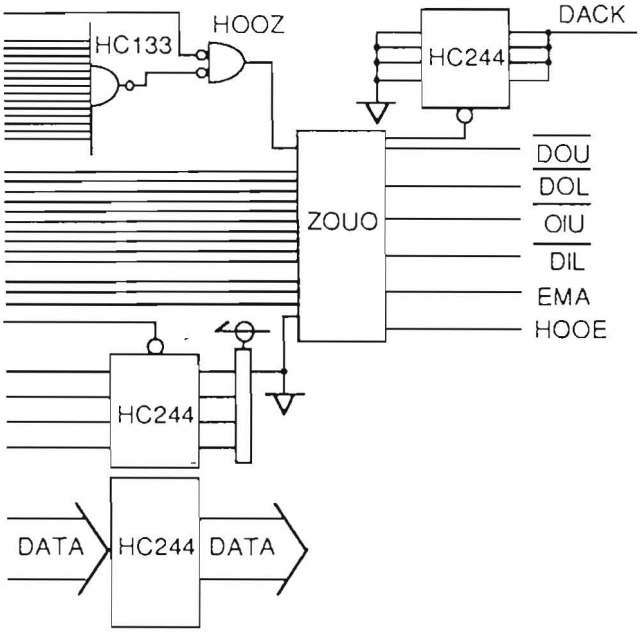
Mode

0 : Outputs comparison results directly to the relays.
Holds the output until next change of the register.

1 : Produces relay output by taking the product of comparison results and an output enable signal.

3. Description of Circuits (Parent Board)

Decoder Block

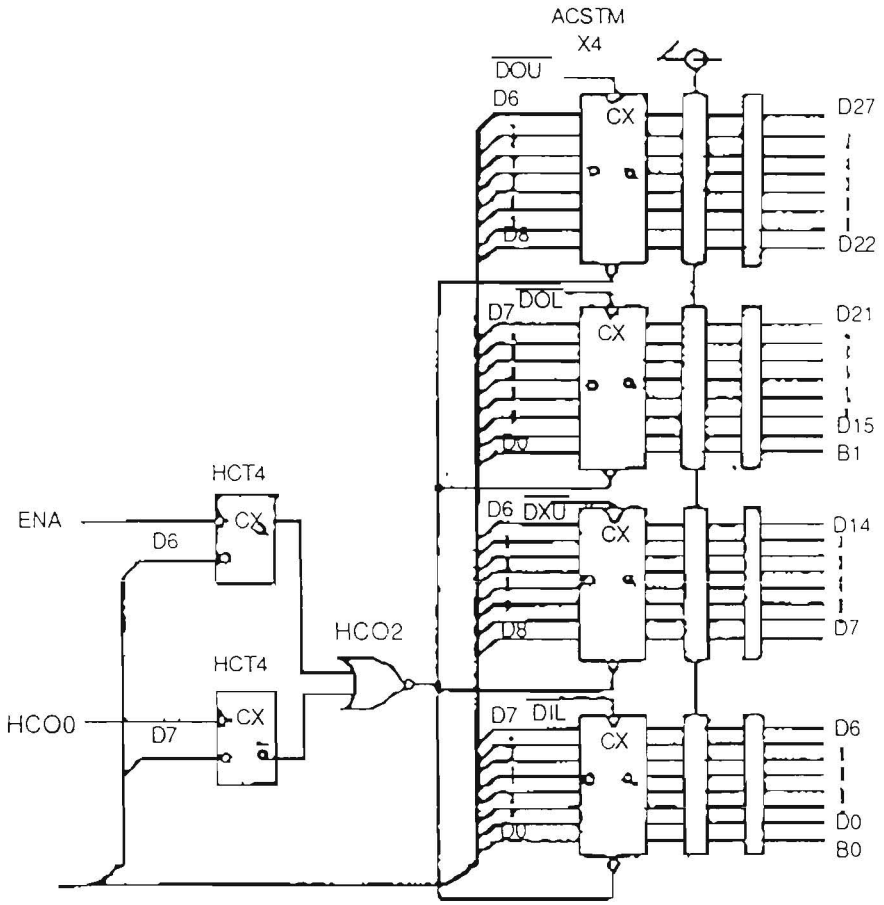


This is an address decoder block which selects the comparator output board on the side of the main body.

PAL is used here, by which signals for writing output result data or set data required for the comparator output board are generated.

The lower left circuit shown in the left figure produces the status of the comparator output board, and immediately below it is the bus buffer.

Relay Drive Block



This circuit mainly aims at driving the relays and latching the data.

The device used for latching is the 74AC574.

Since FACT allows you to obtain a sync source current of 24mA per output, this is directly used as a relay driving circuit.

The flip-flop (to be referred to as FF hereafter) and NOR on the left forms a circuit to set the mode of the comparator board.

The lower FF latches the mode, and upper FF provides an enable signal for the comparate output board.

When the FF, which latches the mode, receives a "0" signal, every time the data of a comparison signal from the main body changes,a relay output signal leading to the external also changes along with it. As there are 16 signal buses coming from the main body, the relay output also change every 16 lines by turn without all of 32 lines being changed at the same time. Next, when the FF, which latches the mode, receives "1", a product with the enable signal appears in the relay output, and the relay output signal can be changed by the signal in all of 32 lines at the same time.

The right circuit latches the comparison signal sent from the main body.

4. Description of Circuits (Child Board)

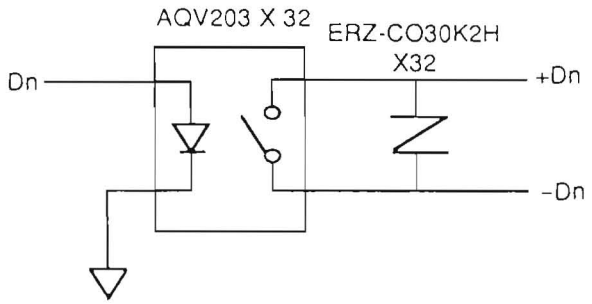
Relay Block

This is a relay output block. It breaks and makes 32 relays by the comparison signal sent from the main body. The relays used in this block are not generally used mechanical ones with coils, but photo MOS relays made of semiconductors. Use of those photo MOS relays allows low current consumption and high-density mounting.

Also, this block uses a "surge absorber" as an element to absorb a noise. This element is a voltage dependent resistor. When a high voltage is applied to it, a resistance value is lowered to prevent a high voltage from being directly applied to the relays.

When a load connected to the relays is likely to contain a high voltage, it is necessary to attach a fuse for load protection.

Since relay output is mutually insulated, a different ground line can also provide control.



2-3-18 Mike Filter

1. General Description

Connector conversion is made and 20 Hz HPF is inserted so that OP-11 (microphone power board), which is one of options for the 2 ch FFT, can be used with the B & K microphone.

2. Specifications

Filter specifications

- Filter characteristic Bessel
- Filter model State variable
- Filter type HPF
- Filter order 2-stage, biquadratic
- Cut-off frequency 20Hz ± 1%
- Attenuation factor 24 dB or more
- Phase 0.1° (adjust when using between 2 channels)
- Dynamic range 90 dB or more
- Noise level 120 dB or more

Input/Output

- Cable with input connector (connected AD3524/25-11)
- Output connectors; JJ-0723 (made by B&K)
  TC1108-23A10-7F
  (made by Tajimi Musen Denki), when the Lyon microphone is used

3. Description of Circuits

Power Source Block

Since only the plus power is aupplied, the block makes a middle points to produce the puls/minus power for the OP amplifier.

HPF Block

A circuit configuration, etc. are the same as the above specifications.

Since the power used for this filter has the voltage mentioned above, it is of AC coupling. Its capacitors are CI and C6.

For control knobs, etc., refer to Chapter 4 ADJUSTMENT & INSPECTION.

4. Adjustment

What You Reguire

- FFT
- AD8621
- Power source

Adjustment of Filter

This instrument has biquadratic 2-stage filters. First, adjust the 1st-stage filter.

First, connect the power source; +15V to +28V to J2 No.3, and GND to J1 No.4.

Remove JPI, connect AD8621 to TP1, and FFT to TP2.

When this is done, set AD8621 to Multisine and connect CLOCK TO CLOCK OUT of FFT for synchronous operation. At this time, FFT causes the spectrum to be displayed and the window to be set to RECT.

Turn VR1 so that the cut-off point of the frequency characteristic picture on the display will be 13.9Hz.

Next, adjust the 2nd-stage filter. Connect AD8621 to TP3, and FFT to TP4. Setting should be the same as the above.

Adjust VR2 and VR3 almost to their center position. Then, turn VR4 so that the cut-off point of the frequency characteristic picture on the display will be 12.5 Hz.

Connect JPI again, and AD8621 to TP1, and FET to TP4.

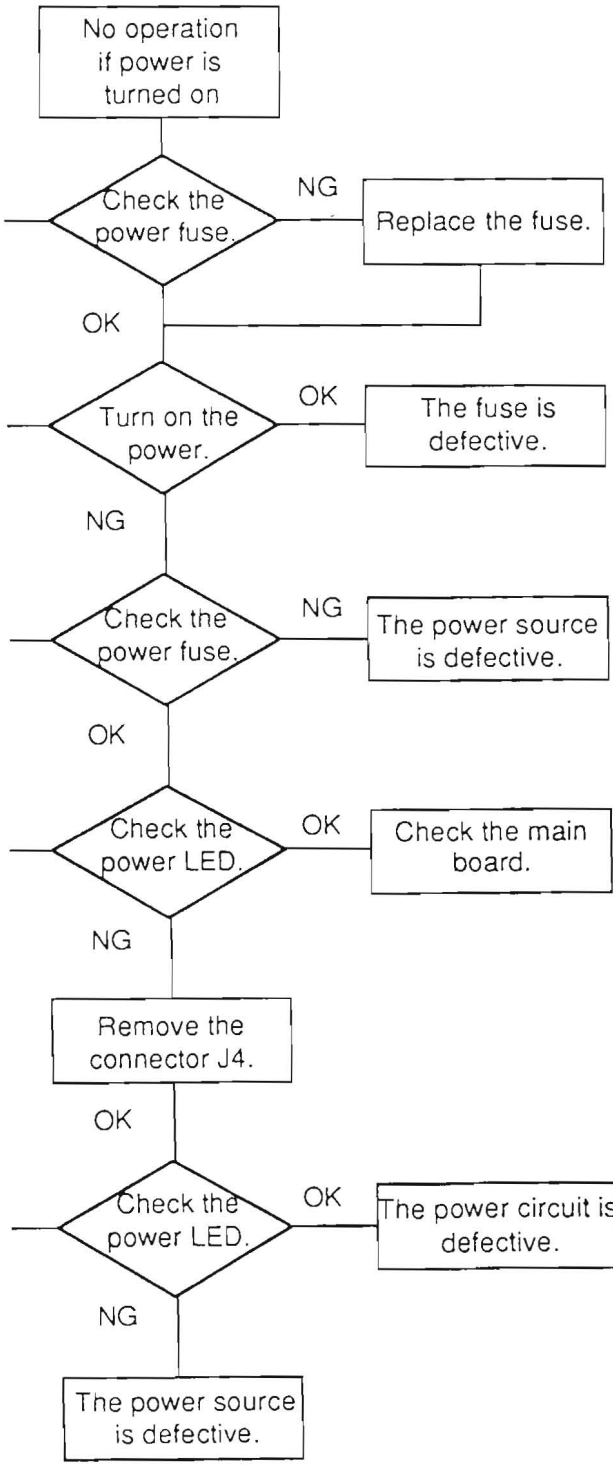
Set each of them as before. Using VR2 and VR3, make adjustment so that the cut-off point of the frequency characteristic picture on the display will be 10 Hz, and that attenuation characteristic will be 24 dB or more. VR2 is associated with a filter gain, and VR3 with a partial raise of the frequency characteristic, that is, attenuation characteristic.

CHAPTER 3 MAINTENANCE

3-1 Troubleshooting

3-1-1 How to Identify the Defective Board by Trouble

1. When the instrument does not work even if the power is turned on, make the following check.

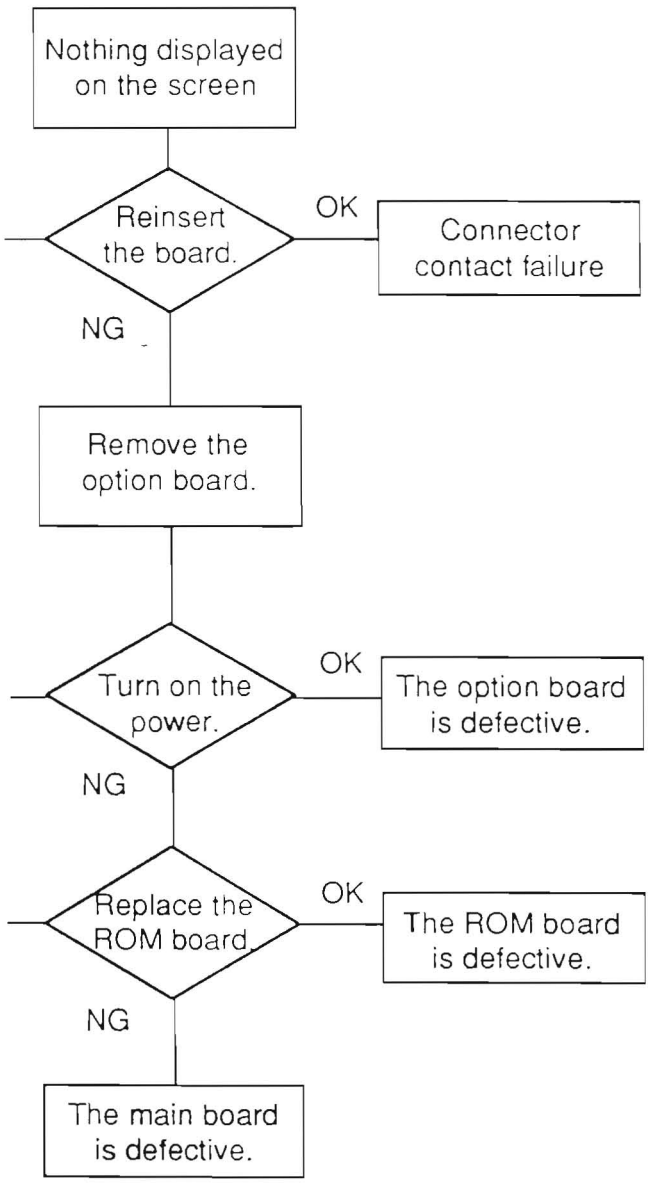


Note: When the power source is defective, replace the power unit or repair the power source.

3. The power source is defectless, but the instrument does not work.

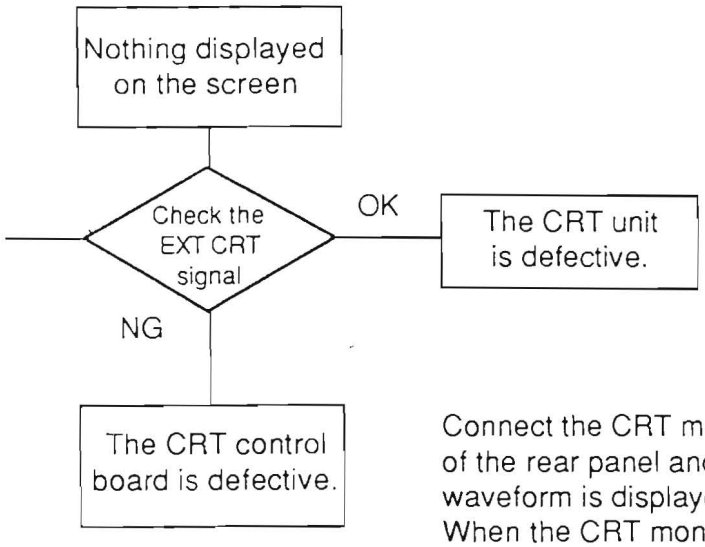
   - Either the power cable inside the instrument is disconnected or the connector is defective.

4. Although a buzzer sounds and the LED on the front panel is turned on, nothing appears on the CRT screen. Also, there is no relay switching sound heard.



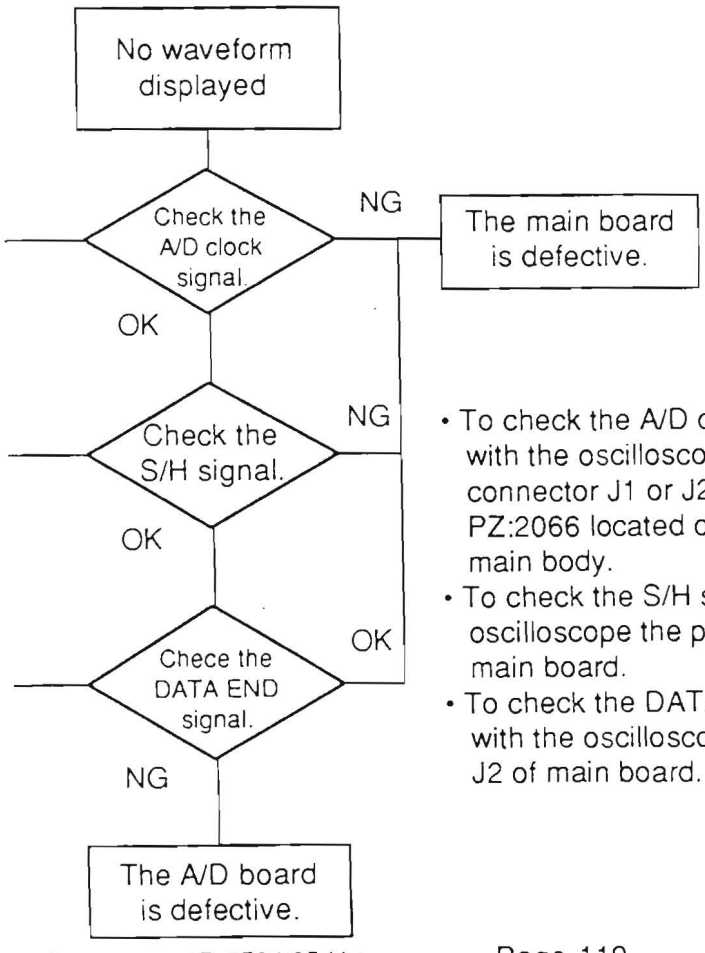
when there are several option board, insert one by one to check whether they are defective or defectless.

5. **Although the LED on the front panel is turned on and a key accepting sound is heard, nothing appears on the CRT screen.**



Connect the CRT monitor to VIDEO OUT of the rear panel and check whether a waveform is displayed on the screen. When the CRT monitor is not available, check with the oscilloscope whether the video signal is outputted.

6. **Although characters are displayed, no waveform is displayed.**



- To check the A/D clock signal, observe with the oscilloscope the pin 22B of the connector J1 or J2 of the main board PZ:2066 located on the back of the main body.
- To check the S/H signal, observe with the oscilloscope the pin 26B of J1 or J2 of the main board.
- To check the DATA END signal, observe with the oscilloscope the pin 29B of J1 or J2 of main board.

Power Board PZ : 2068

LEDs, and Output Voltages and Names Table

Name	Voltage	LED	Circuit Used
+ VC12	12 V	D206	CRT and printer
+ VL 5	5 V	D106	Main board and option
+ VS12	12 V	D401	Main board, external trigger, test signal, generation circuit, SG option
- VS12	12 V	D402	
+ VA 5	5 V	D403	Ach A/D board
+ VA12	12 V	D404	
- VA12	12 V	D405	
+ VB 5	5 V	D406	Bch A/D board
+ VB12	12 V	D407	
- VB12	12 V	D408	
+ VS 2	15 V	D211	Power source for VC12 control circuit
+ VS 1	15 V	D111	Power source for VL15 control circuit

3-1-2 Troubleshooting of Each Board

1. Troubleshooting of Power Source

There are various cases of troubles concerning the power source, among which major ones are;

A. Start-up error
B. Output is made, but functionings are faulty and unstable.

"Start-up error" means that when the power switch is turned on, the power source stops functioning, resulting in an operation halt state.

The following causes are likely:

① Due to breakage

- Breakage due to an excessive force applied to the FET, drive circuit, etc.
  (The power source does not start up completely)
- Breakage due to deterioration of diode pins of the PZ : 2068
  (Output comes to stop or disappears sometimes)
- Due to characteristic deterioration of SCR
  (Although the power source starts up, it stops immediately or is very unstable)

② Due to O.V.S.

When the overvoltage sense circuit stops because CRT +12V or logic +5V is an overvoltage.

③ Due to "divergence of circuit constant"

Divergence of the timing of the start-up circuit
Voltage stop of the starting circuit takes place prior to the functioning of the main circuit.

As for the item B above, there is nothing wrong with start-up, but the output section is affected.

④ A ripple noise (particularly CRT) appears.

Unstableness of the primary/secondary circuit

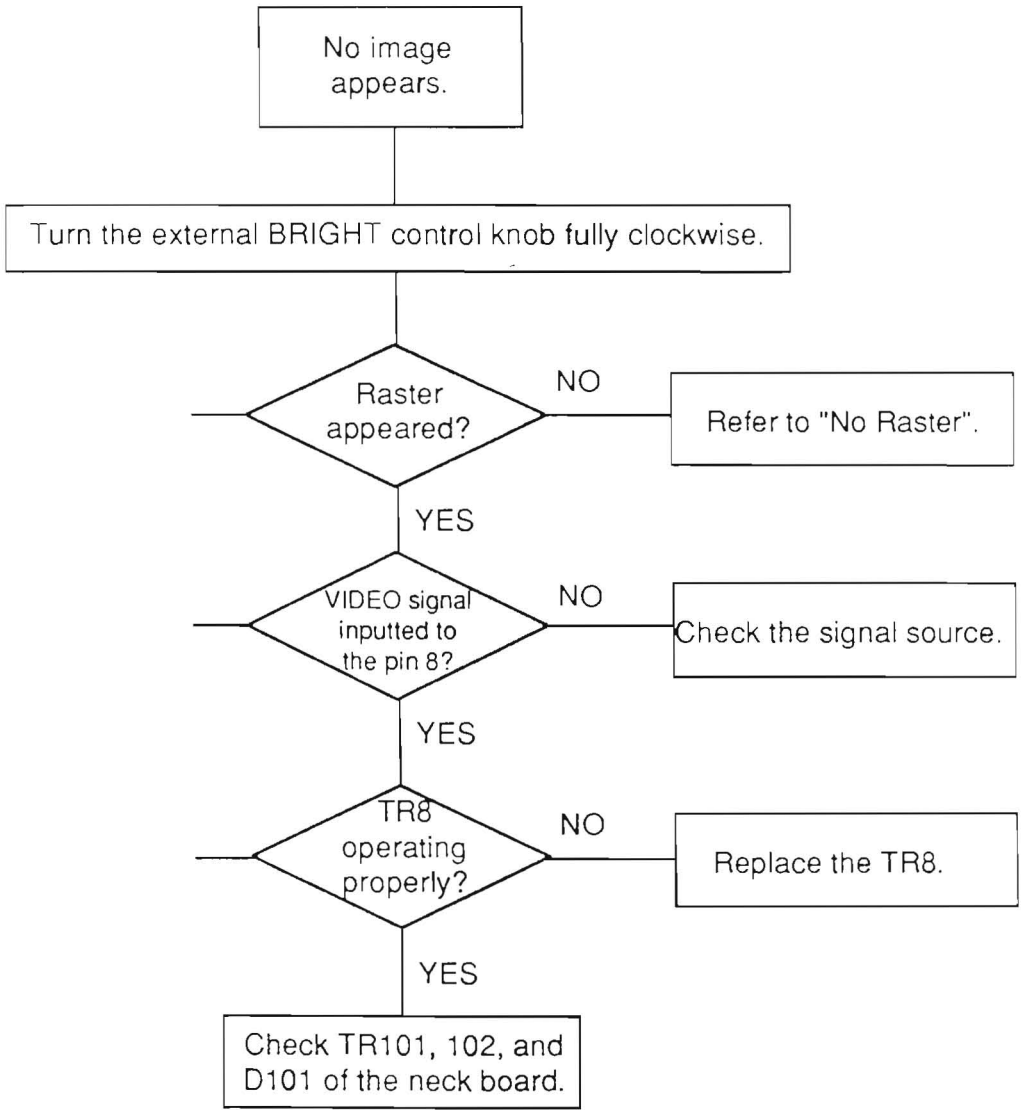
⑤ Due to defective parts in each section

Particularly, pin breakage or wrong connection of capacitor diodes, etc.

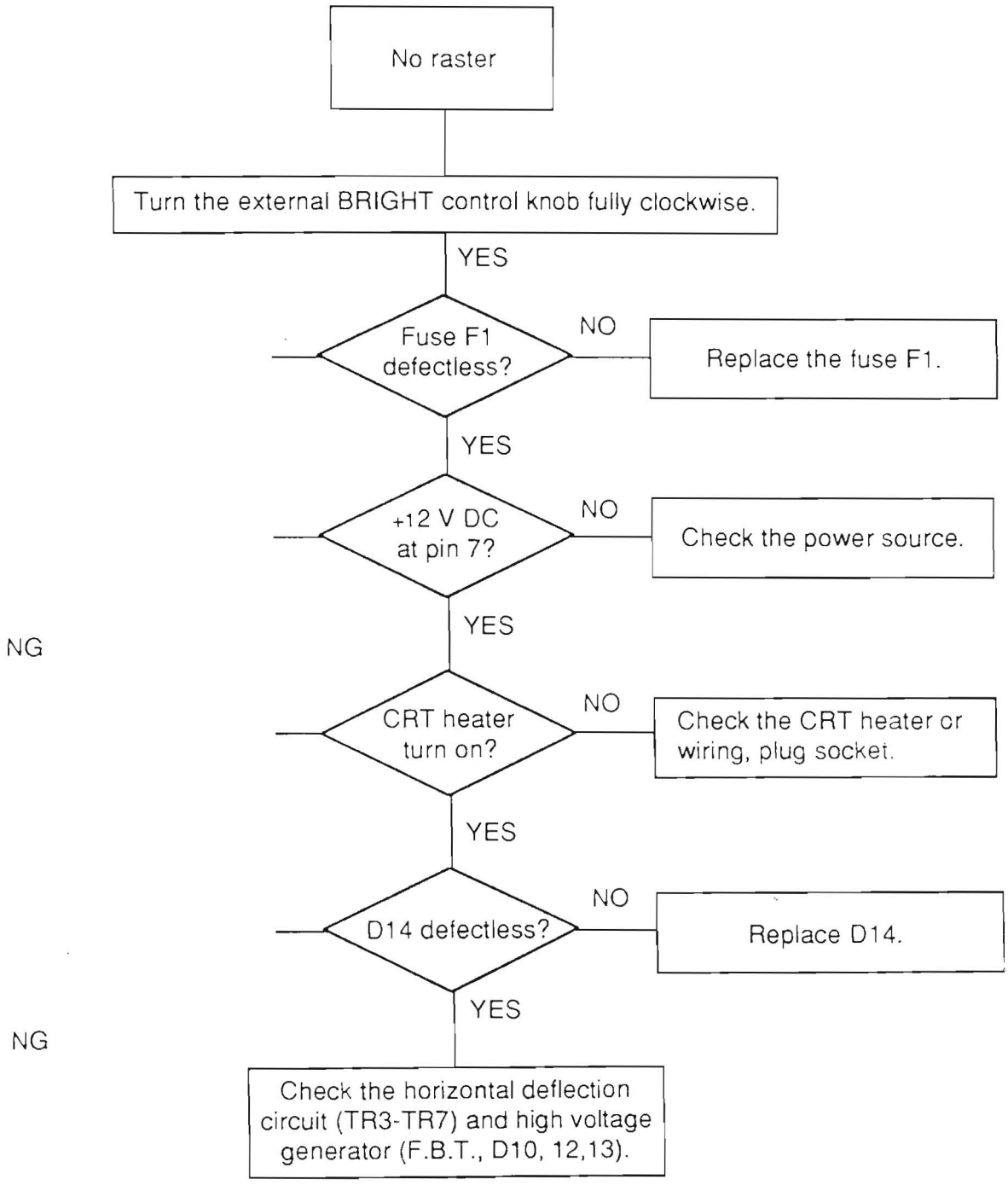
2. Troubleshooting of CRT Unit

1. Troubleshooting

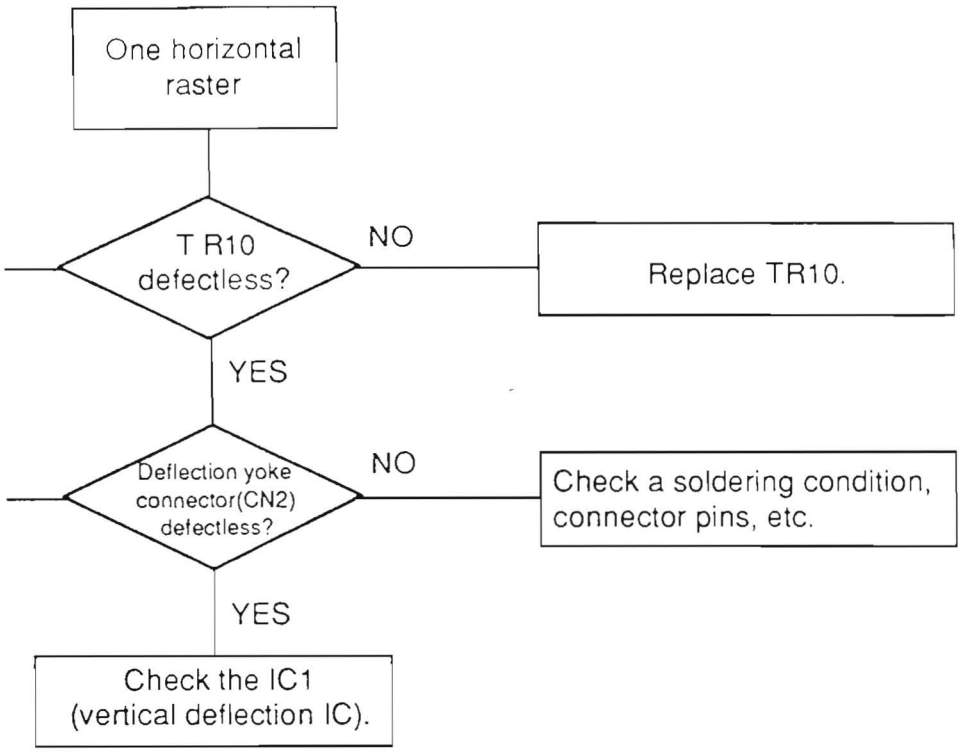
① No image appears.



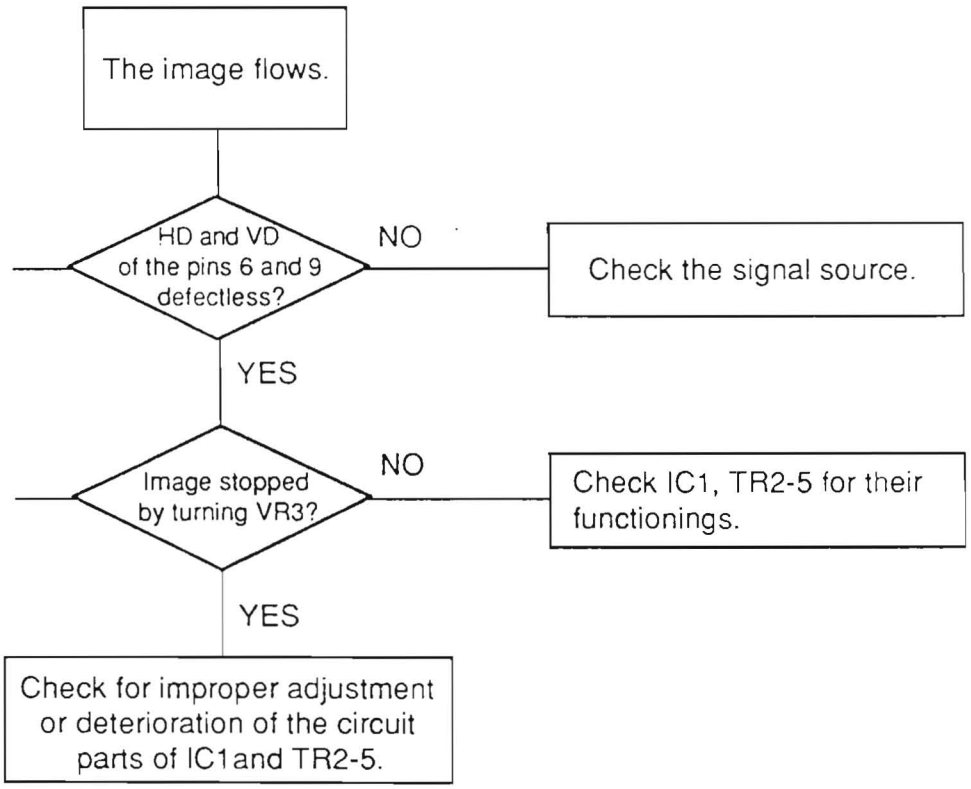
② No raster


No raster
Turn the external BRIGHT control knob fully clockwise.
YES
Fuse F1 defectless?
NO
Replace the fuse F1.
YES
+12 V DC at pin 7?
NO
Check the power source.
YES
NG
CRT heater turn on?
NO
Check the CRT heater or wiring, plug socket.
YES
D14 defectless?
NO
Replace D14.
YES
NG
Check the horizontal deflection circuit (TR3-TR7) and high voltage generator (F.B.T., D10, 12,13).

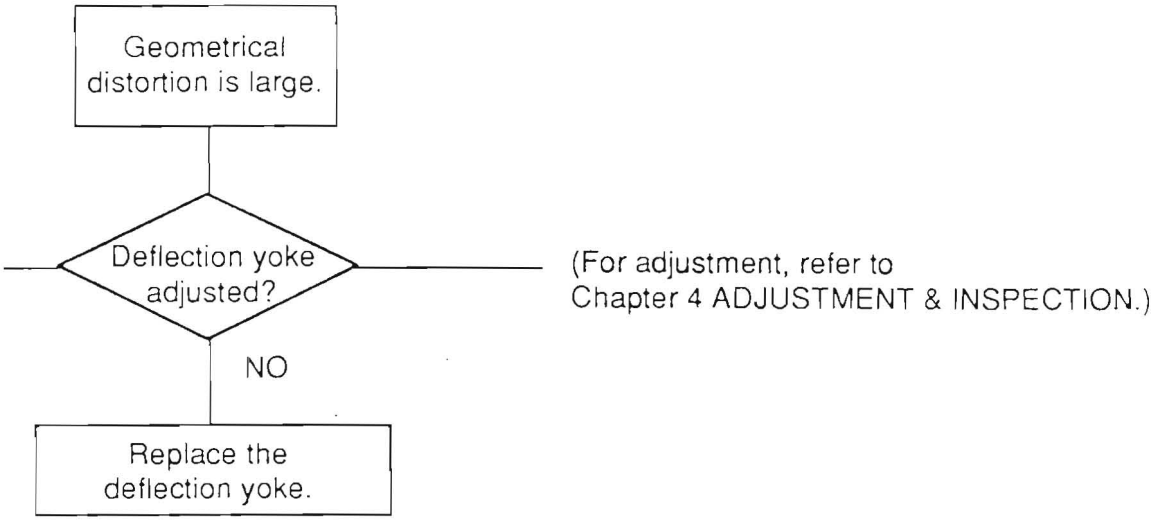
③ One horizontal raster



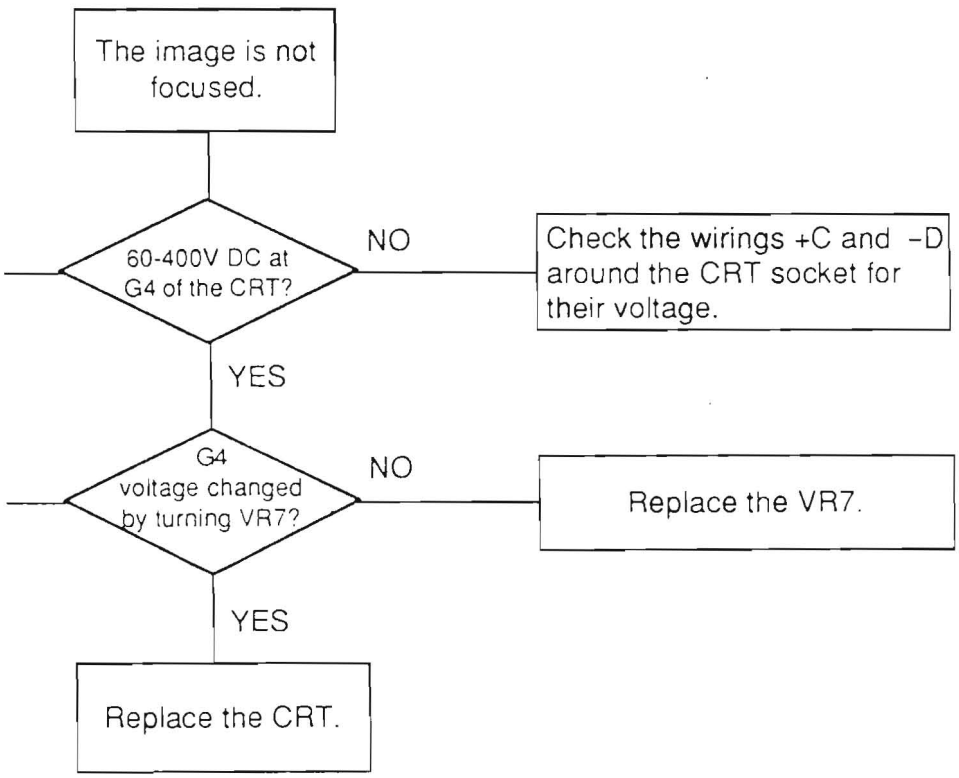
④ The image flows without stopping.



⑤ Geometrical distortion is large.

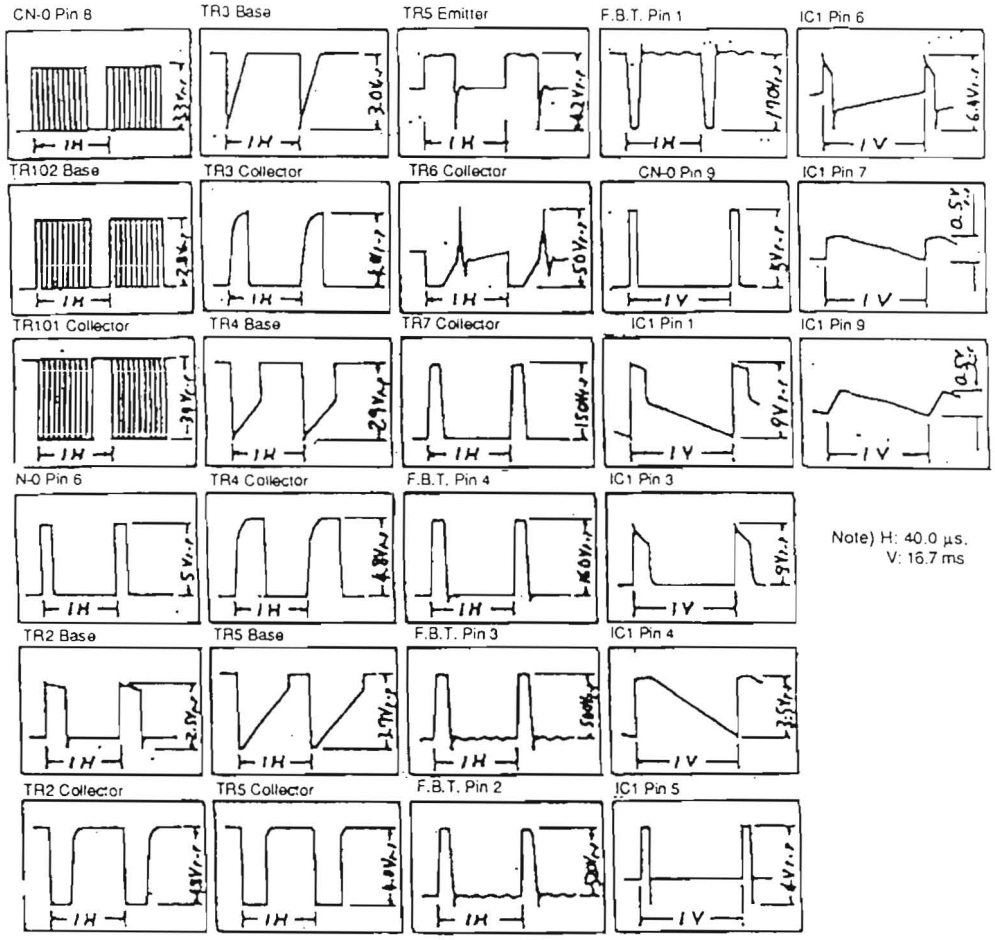


⑥ The image is not focused.



2. Voltage Waveform of Each Section and High Voltage Generator

Voltage Waveform and DC Voltages of Each Section



Note) H: 40.0 µs,
V: 16.7 ms

DC Voltages of Each Section

DC Voltages of Each Section

Unit: V

	Base	Collector	Emitter
TR1	8.36	0.0	8.37
TR2	0.67	2.84	0.55
TR3	0.24	1.28	0.0
TR4	0.71	2.72	0.58
TR5	0.41	2.78	0.31
TR6	0.31	7.69	0.0
TR7	—	—	0.0
TR8	2.12	11.85	1.61
TR9	11.95	0.15	0.0
TR101	6.34	19.5	6.01
TR102	1.60	6.01	1.27

Unit: V

IC1 1	5.4
IC1 2	11.8
IC1 3	11.0
IC1 4	8.9
IC1 5	0.6
IC1 6	2.9
IC1 7	5.1
IC1 8	0.0
IC1 9	5.9
IC1 10	11.9

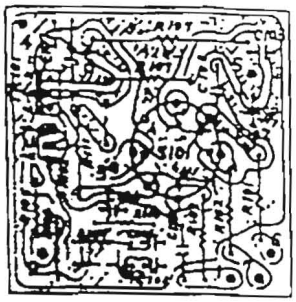
Unit: V

CN-0 7	12.0
S101 1	-15.4
S101 2	19.4
S101 3	11.8
S101 4	0.0
S101 5	—
S101 6	470.0
S101 7	60.0
+B	64.6
+C	480.0
-D	-136.0
F.B.T 6	—

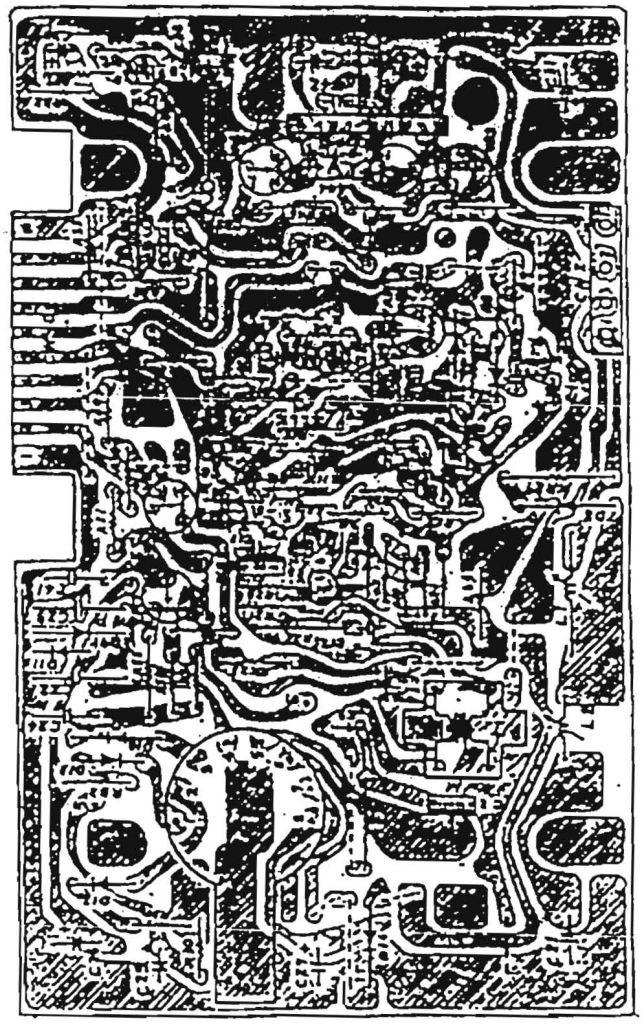
Note: To measure a voltage, use the DC range of a digital voltmeter.

Parts Mounting Drawing of Printed Circuit Board

[Neck PCB]



[Main PCB]



3. Precautions for Disassembly

Note the following points when removing the parts from this instrument either in production or maintenance.

3-1 When modifying (removing) the parts or wirings of this instrument due to a certain reason, be sure to turn off the power and disconnect the power supply connector to the monitor.

3-2 When dismounting/remounting the anode cap (high-voltage cap) to the CRT

1 Prepare the screwdrivers 1 and 2 shown in Fig. 17-1.

2. The grip of the screwdrivers 1 and 2 must be an insulator.

3. Fixing the tip of the screwdriver 1 at the carbon black section of the CRT, ①

4. Fix the base of the screwdriver 2 to that of the screwdriver 1.②

5. Holding this state, insert the tip of the screwdriver 2 into inside the anode cap.③
   When this is done, a high voltage is discharged with a snap.

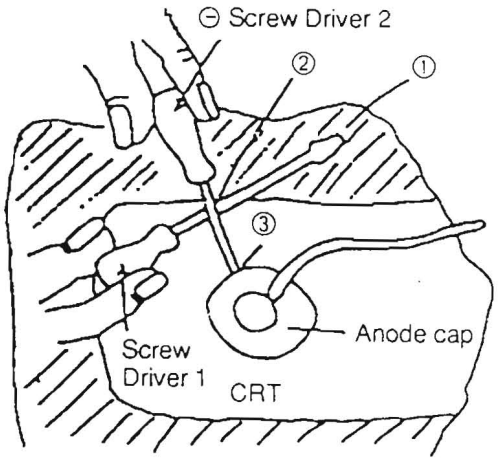


Fig. 17-1

6. Hold this state for about another 5 seconds. After this, the anode cap can be removed by unlocking an internal hook fitting with the screwdriver 2.

Note: Do not directly touch the high-voltage section (anode cap) because a voltage of about 10 kV is impressed there. Also, a high voltage flows here again from somewhere else in instantaneous discharge and you may get an electric shock.

3-3 When removing the main PCB

With the power turned off, a voltage of -150V or less is held at C26. This is so done to prevent the CRT from flashing at a beam spot. To remove the main PCB, follow the procedure below.

1. Remove the CRT neck PCB.
   The CRT neck is relatively fragile. When removing it, pull it out backward, twisting it lightly.
2. If the CRT neck PCB is removed, there appears no beam spot. After this, short-circuit both ends of D11 and discharge the -150V system. After this, the main PCB can be removed by loosening its setscrews.

Note: Be careful not to touch the compensation magnet (for deflection) of the diflection yoke.

3-4 When removing the CRT

1. Discharge a high voltage from the anode cap.
2. Remove the CRT neck PCB.
3. Remove from the main PCB the connector at the end of the line coming from the deflection yoke(DY).
4. After this, remove the screws at the lugs of the CRT.

CHAPTER 4 ADJUSTMENT AND INSPECTION

Table of Contents

4-1-1 A/D Board Adjustment Procedures PZ:2066

Table of Contents

1. Preparation

Prepare the following tools and jigs.

- Voltmeter (4 and 1/2 digits or more)
- Oscilloscope
- Signal source ---------AD8621 or National VP-7201A
- 2ch FFT main body
- Getter board for the analog board (1 : 1)

Note: That this is different from one foe logic.
There is a danger of destroying P.S.

2. Outline of Adjustment Procedures

Adjustment of the PC2066A/B follows the procedures below.

① Coarse adjustment
Visual, check, operation check, etc., and casing after coarse adjustment

② High-temperature heat run
Heat run in a high-temperature room (40°C)

③ Fine adjustment
Fine adjustment if defectless after high-temperature heat run

3. Coarse adjustment

3-1 Visual Check

① Check whether the polarities of chemical and tantalum capacitors match the silk.

② Check whether the filter module(U14) is in a correct direction. Also, check for the filter type.

20kHz version---------AAD12009 (20k)

100kHz version -------AD11009 (100K)

③ Check whether the A/D module (U13) is in a correct direction.

④ Check whether the offset module (U1) is in a correct direction. (100kHz version only)

⑤ Check whether the input and output ends of the common choke are not replaced by each other. They may be replaced sometimes.

⑥ Check whether the shielding tape does not touch RND, part pine, etc.

3-2 Relay Operation Check

Insert the analog board into the main body through the getter board, and check that the relays work.

① Turn on/off the soft keys AC/DC and GND, and check that the relays are working.

② press OFFSET, and then, ON/OFF, and check that the relays are working.

③ Press TEST, and then, ON/OFF, and check that the relays are working. As a test waveform (square wave) appears on the CRT screen, you can check with it as well.

④ Increase a gain from +30dB to -6dB by continuously pressing the Gain key of Bcn (or Ach) INPUT. This causes the attenuator's relays to be changed over at a point changing from -20dB to -30dB. Change the gain at one stretch, and if a relay sound is heard, then, it is O.K.

3-3 Power Source Check

Measure the anlog connector J2 on the anlog board with a voltmeter and make sure that there is a voltage.

Connector No.

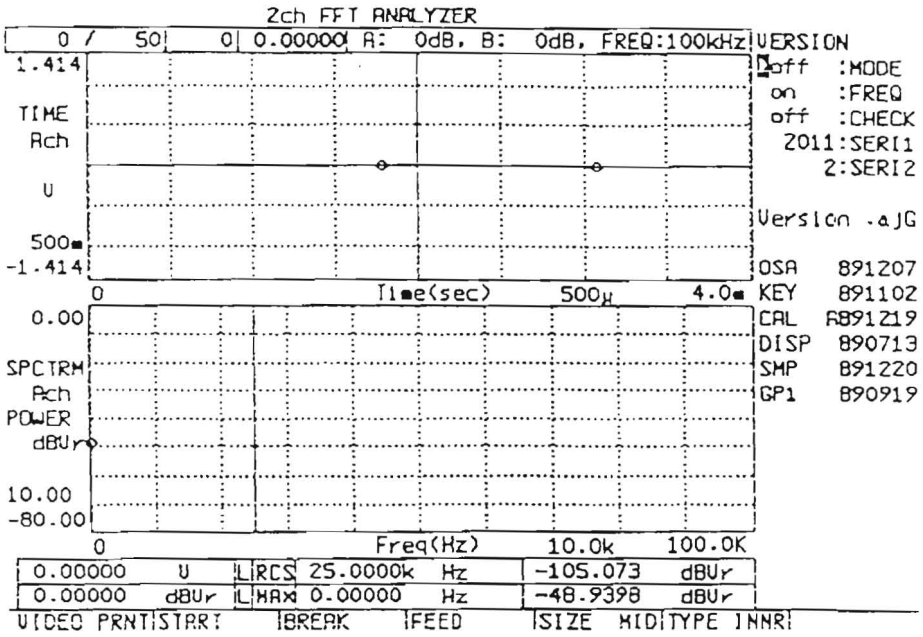
	(Hi)	(Lo)	
-12V	5, 6 ABC	1, 2, 3, 4, ABC	Make sure of -12V (±1.2V)
+5V	7, 8 ABC	↑	Make sure of +5V(±0.5V)
+12V	9, 10 ABC	↑	Make sure of +12V (±1.2V)
D5V	17 ABC	16 ABC	Make sure of +5V (±0.5V)
+8V	Q22 emitter	1, 2, 3, 4 ABC	Make sure of +8V (±0.8V)
-8V	Q24 emitter	↑	Make sure of -8V (±0.8V)
-5V	Pin 3 of U21	↑	Make sure of -5V (±0.5V)

3-4 Version Setting

The analog boards PC2066A and PC2066B for the FFT are the same except the filter module(U13). When making adjustment, software must be set in accordance with each machine type. A setting procedure is as follows. After pressing the HELP key, "MEM CLR" appears on the soft key. Press it. Subsequently, press rightmost f6 where nothing is displayed. This displays the version on the right part of the screen.

Modes are as follows.

- MODE ------ Must be OFF.
- FREQ ------- OFF for the 20kHz version, and ON for the 100kHz version.
- CHECK ---- For various checks. Must be OFF upon shipment.



Note: Pressing: ENTER Sets to each version

3-5 Offset Adjustment

Setting : +10dB, DC coupling, internal GND
+10dB, DC coupling, internal GND

(1) Head Amplifier Offset Adjustment

① Fully turn VR1 (3-turn trimmer) fully to the left (or right), and then, return it one and half turns (to the center).

② Observing between TP3 (High) and TPø (Low) with a voltmeter, connect 5KVR to R63 (or R69) in parallel. Turn the VR to adjust to within 0 ± 1mV. Leave VR1 intact at the center.

③ Remove the VR and measure its resistance value. Attach a metal-film resistor with the closest value to that value to the position where the VR was.

④ Measure the voltage between the TP3 (High) and TPø (Low), and turn VR1 to adjust to within 0 ± 1mV.

(2) Range Amplifier Offset Adjustment

Measure between TP4(High) and TPø (Low) with the voltmeter and turn VR6 to adjust to within 0 ±1mV.

(3) Gain Amplifier offset Adjustment

Measure between TP6 (High) and TPø (Low) with the voltmeter, and turn VR5 to adjust to within 0 ± mV.

(4) Filter Offset Adjustment

Measuring between TP6 (Hi) and TPø (Low) with the voltmeter, repeat turning on/off the filter. With VR4, adjust to within the difference of 2~3mV so that the voltage at TP6 will not change by turning the filter on/off.

3-6 Frequency Characteristic Compensation

The AD8621 is connected to the signal source, which compensates a change of the frequency characteristic of the input attenuator and flattens the frequency characteristic. Connection and compensation methods follow.

(1) Connecting the FFT to the AD8621

① With a coaxial cable, connect CLKOUT of the FFT to CLKIN of the AD8621.

② Press the MODE key of the AD3621 to determine whether to synchronize with INT CLK or EXT CLK. When the LED is illuminated, it indicates synchronization with INT CLK, and when unilluminated, EXT CLK. When blinking, turn the rotary encoder to change the CLK mode. Before changing the mode, match the frequency range of the FFT analyzer and AD3621 which are to be synchronized. Otherwise, they could not be synchronized. If then are synchronized, the LED goes off and FFT mode setting is as follows.

- 2.56 x Range, 1,024 points
- The frequency range is 20K for the 20kHz version, and 100K for the 100kHz version.

(2) Compensation 1 Frequency Characteristic Compensation with ATT at -30dB

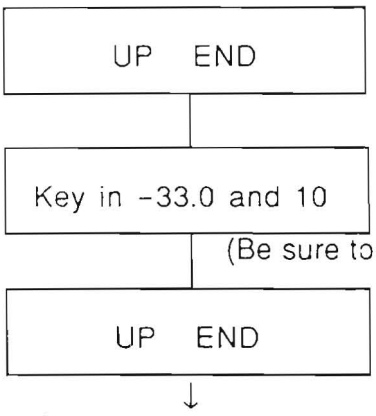
Setting : ødB; AC coupling; FLTON
AD8621 MULTI SIN(ødB) input

(a) Input MULTI SIN from the AD8621 to synchronize with the FFT clock. The time waveform appears on the upper screen, and the spectrum waveform on the lower screen.

(b) Set the FFT window RECT(rectangular). Pressing the EXTEND key displays the menu on the soft keys. f1 reads "WINDOW". Pressing it displays the window types on the right part of the screen. Set to "RECT" with the ENTRY key.

(c) Pressing the Y-SCALE key displays the menu on the soft keys. Press the NEXT key to display the next menu. The UP ENT key is displayed. The upper limit of the spectrum can be set by pressing that key. For example, when setting the upper limit to

ex.



The upper limit of the spectrum is set to -33.0dB.

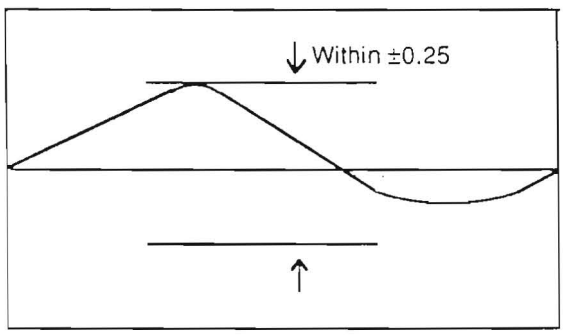
Note: When a set value is entered, that value appears at f6. When clearing the numerical value currently set, press the "UP ENT", and then, press "EXTEND".

(d) Press LOW ENT and set the lower limit in the similar manner as in (c).

(e) Viewing the enlarged screen (to such an extent that the entire waveform can be viewed), adjust the waveform straight, using VC1.

(f) Enlarge the screen so that the full scale will be 1dBp-p, and make fine adjustment further so that it will be within ±0.25dB.

SPECTRUM



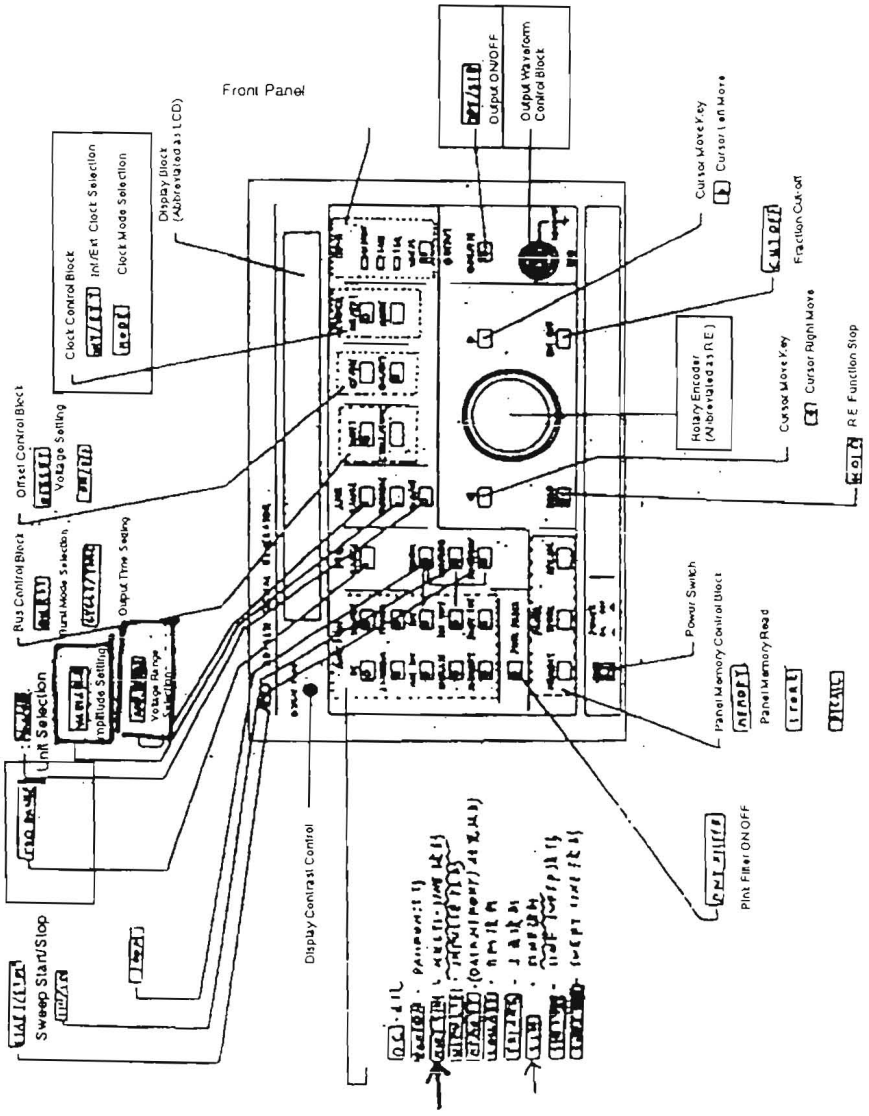
The states of (a) through (f) above are illustrated in the figures (a) through (f) on the following pages. The visible ripples represent the characteristic of the anti-aliasing filter(U13) itself, because this filter has the octonary simultaneous Chevishev characteristic. The filter Characteristic can be clearly seen by turning the filter on/off.

Fig. (g) is when the filter is turned on.

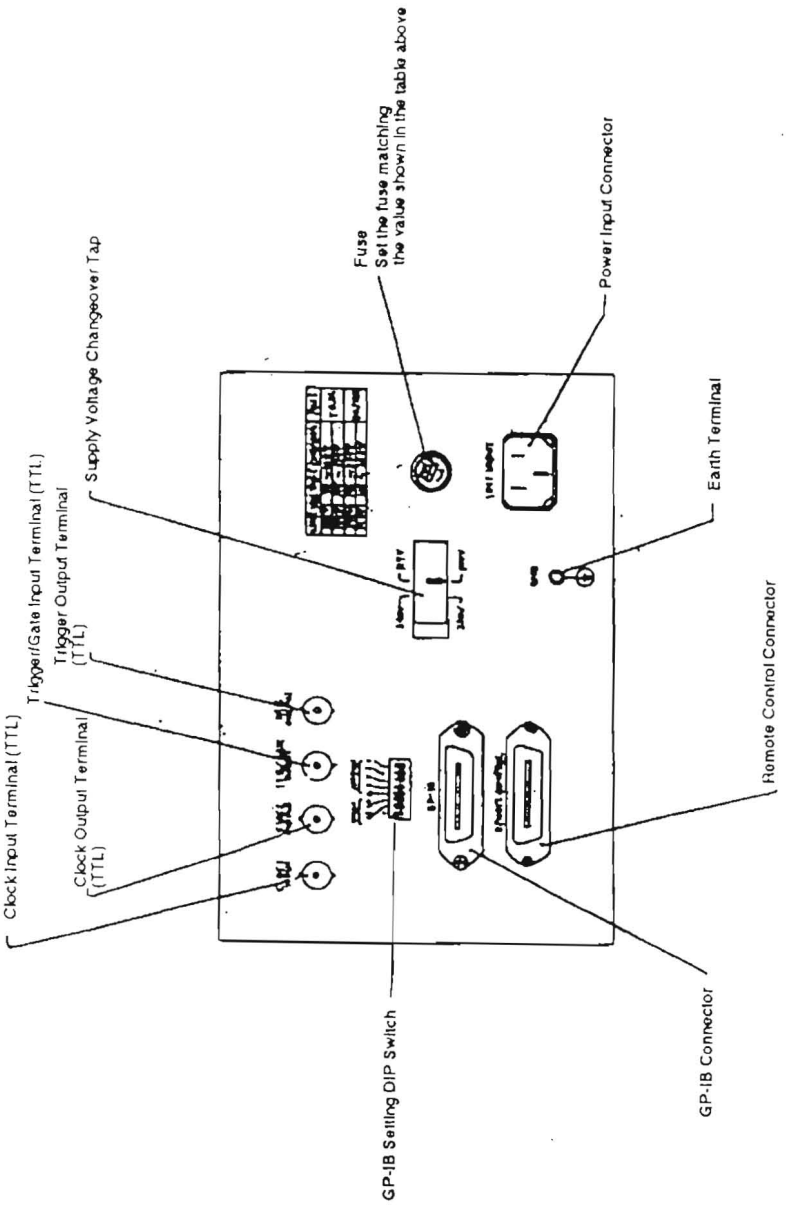
Fig. (h) is when the filter is turned off.

Note: The front and rear views of the AD8621 are shown on the following pages.

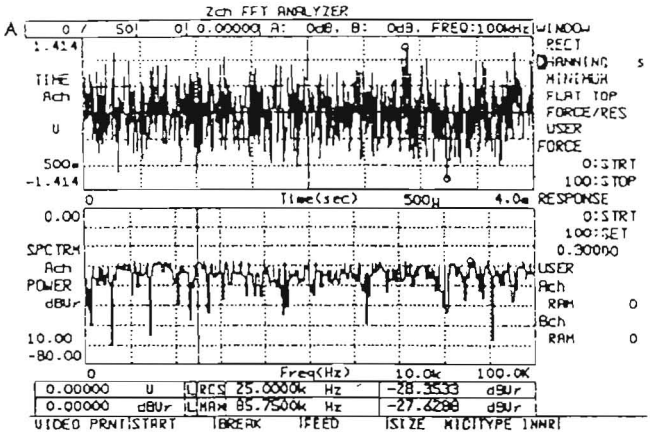
Description Panels

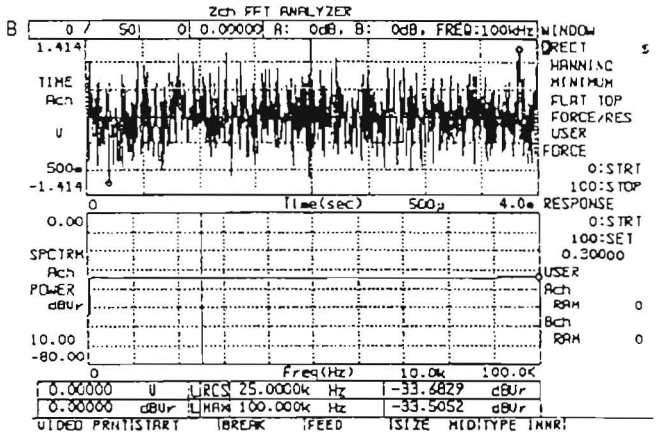


Rear Panel

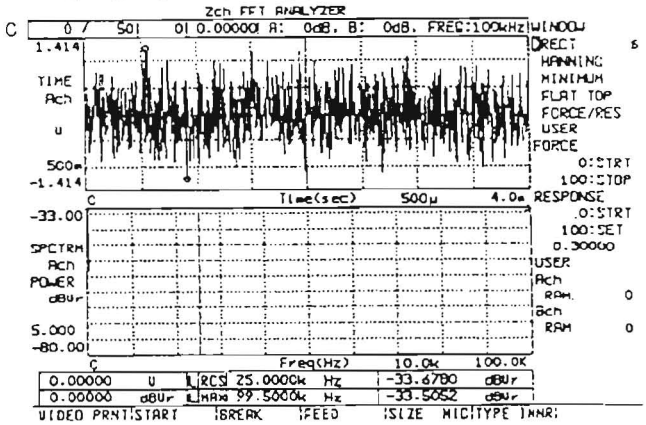

Fuse
Set the fuse matching
the value shown in the table above
Power Input Connector
Supply Voltage Changeover Tap
Earth Terminal
Trigger/Gate Input Terminal (TTL)
Trigger Output Terminal
(TTL)
Clock Output Terminal
(TTL)
Clock Input Terminal (TTL)
Remote Control Connector
GP-IB Setting DIP Switch
GP-IB Connector

AD8621 MULTISIN (ødB. 100K)
Input

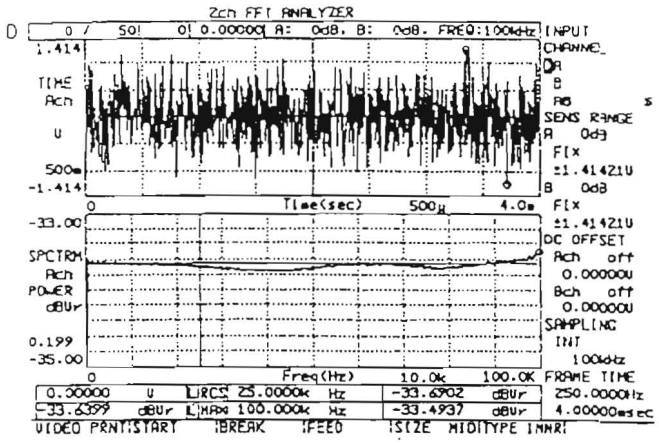




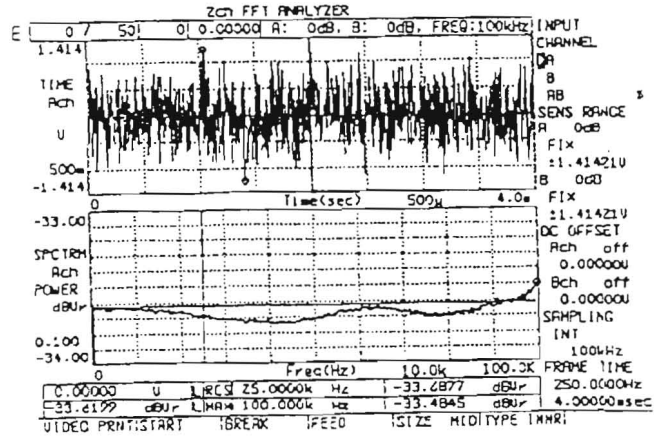
When the upper limit of the full scale is set to -33.0 dB
with "UP-ENT" of "Y-SCALE"



When the lower limit of the full scale is set to -35dB with "LOW-ENT"of "Y-SCALE"

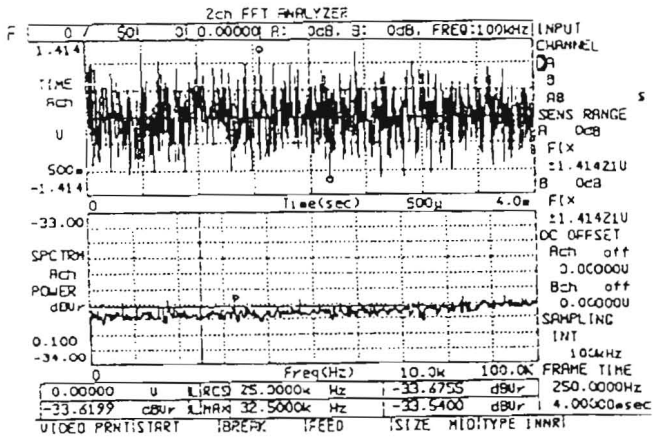


When the full scale in (d) is enlarged further

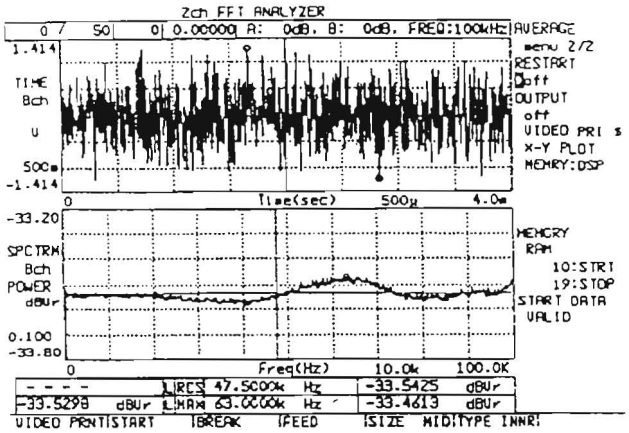


When the frequency characterstiic is adjusted with VC1

FILTER OFF

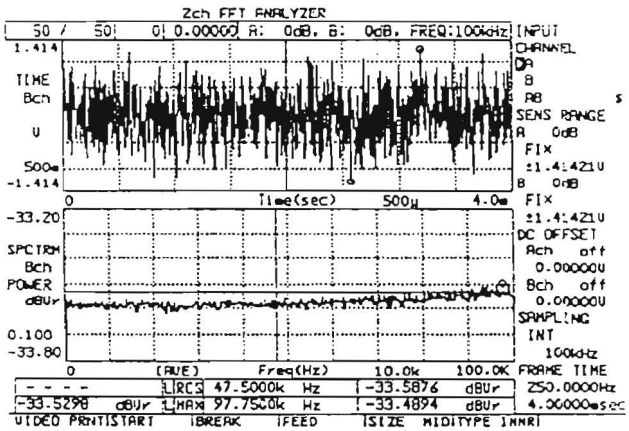


G



H

When the filter is turned off



(3) Compensation 2(Frequency Characteristic Adjustment with ATT at -60dB)

Setting : +10dB, AC coupling, FLT ON
AD8621 MULTI-SIN(+10dB) input

Like (a) through (f) in 6-2, adjust with VC2 to within ±0.25dB.

(4) Full Scale Adjustment

Adjust the full scale after frequency characteristic adjustment.

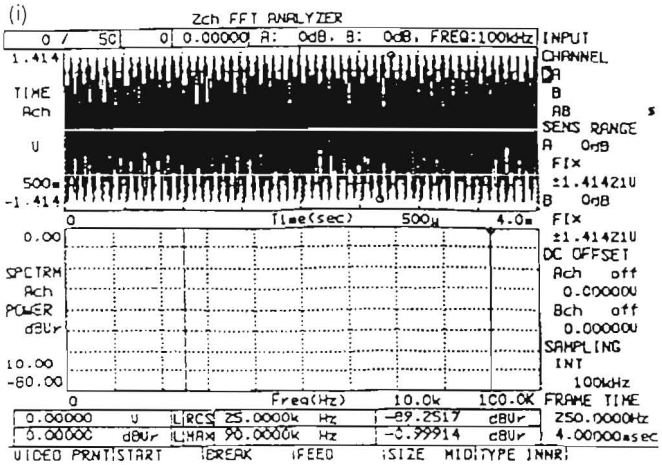
Setting : ødB, AC coupling, FLT ON
AD8621 SIN(-1.0dB) input

Viewing the frequency characteristic observed in 6-1, enter the sine wave(-1.0dB) around the center frequency, and then, make adjustment with VR2, viewing a maximum value(to -1.00dB, ±0.05dB).

ex.

When the full scale is adjusted

(i)

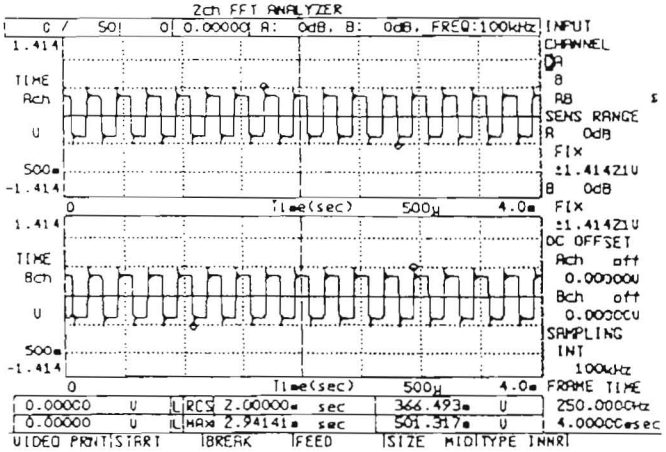


In the left example (1), a sine wave of 90kHz, -1.0dB was entered because the center frequency was 90kHz in the figure (f).

3-7 Test Waveform Observation

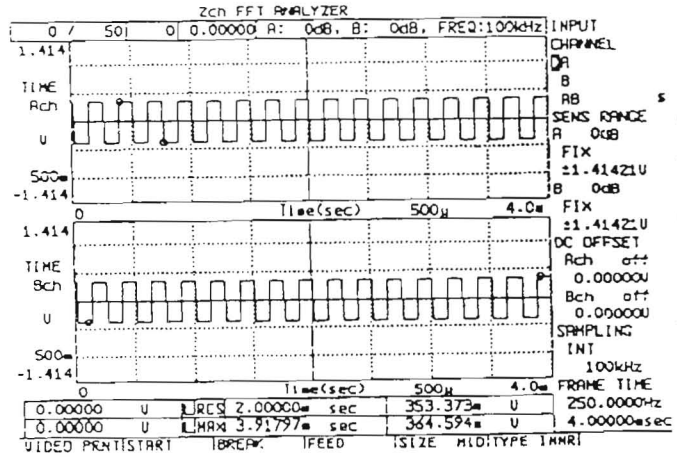
Make a test waveform outputted and observe its time waveform and spectrum waveform.

Note: Even if the input is switched to Internal GND at this time, only the LED is illuminated and the test waveform is not cleared.



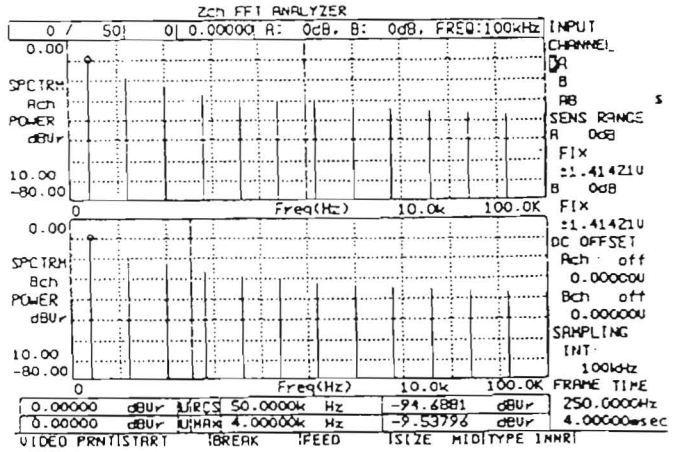
When the filter is turned on

Due to the filter characteristic, overshoot and ringing are observed in a transient area.



When the filter is turned off

When this is done, no noise sould be superimposed on the time waveform. Overshoot disappears.



Viewing with the spectrum, there should be no peculiar components other than those of the basic wave and harmonic wave.

Note: Since the test waveform is made by frequency-dividing the sampling clock, the number of square waves and that of spectral lines are not changed even if the frequency range is changed.

3-8 OVER Detection Check

Setting: ødB, DC coupling
AD8621 DC input

Input a direct current from the AD8621. Since an analog OVER detection values is 125 % of the full scale, increase the DC input and make sure that the OVER buzzer sounds at +1.76V(±5 %) = 1.67V~1.84V. Likewise, input for the minus(-) side and make sure that the buzzer sounds at -1.76V (±5 %).

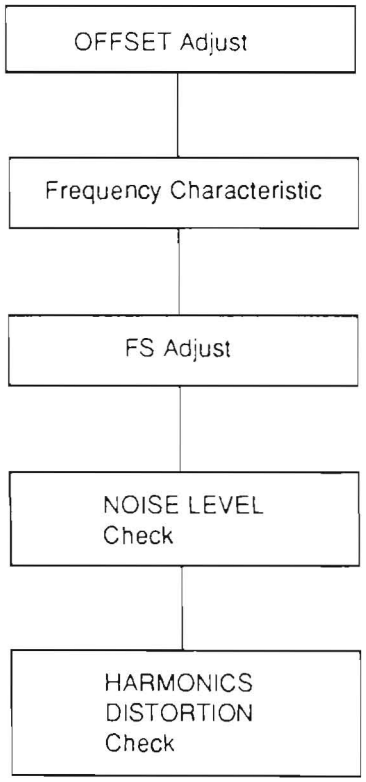
Note: The OVER LED is illuminated by digital OVER at 90-plus % of the full scale. The digital OVER threshold values for Ach and Bch differ depending on the gate arrays. The Ach has a higher set value than the Bch. Therefore, when the same input is given to the Ach and Bch, the OVER LED is illuminated for the Ach, but not for the Bch.

For the Ach, the OVER LED is illuminated at ±0.56dB or more.
For the Bch, the OVER LED is illuminated at ±1.15dB or more.

4. Fine Adjustment

Mount a shielding case and incorporate in the main body. After 15 to 20 minutes, perform a neat run and proceed to fine adjustment. Make fine adjustment in the similar manner as coarse adjustment. However, no analog getter board is used. Insert directly into the slot of the main body.

Adjustment procedures are as follows.

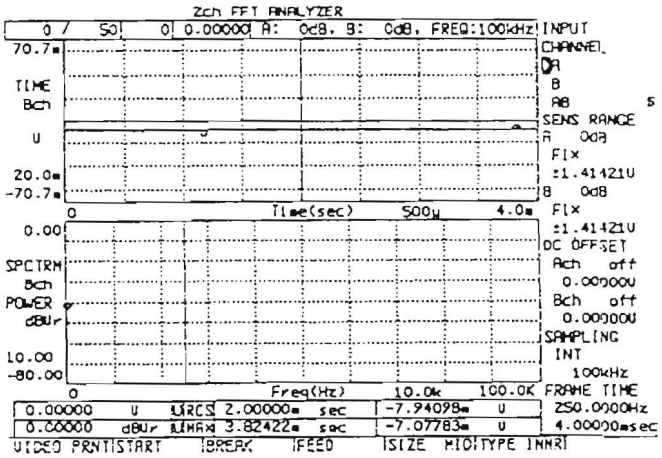


100k version 100K~100Hz 10 Range
20k version 20K~20Hz

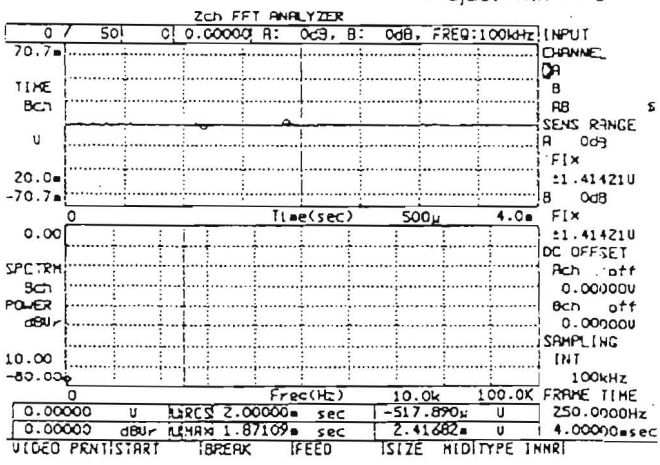
Offset Adjust (a)~(f)

(a) FILTER OFF

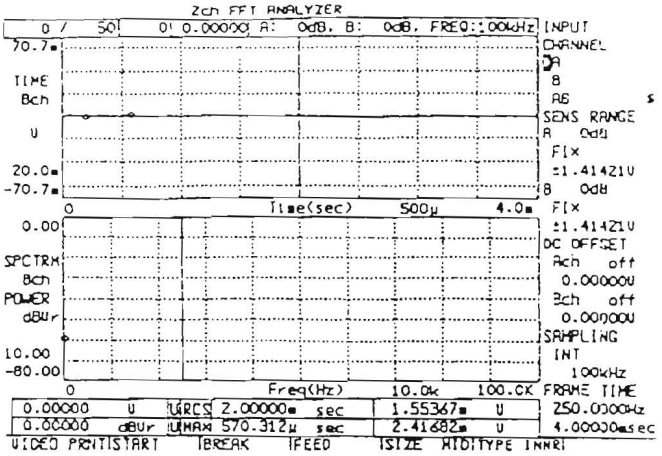
AC COUPLE



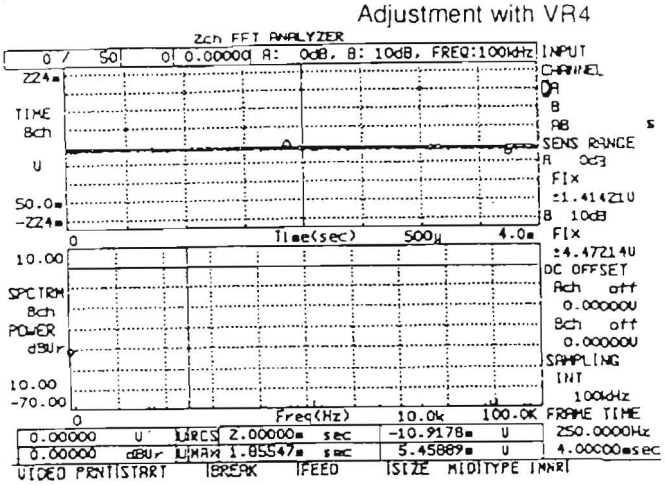
(b) FILTER OFF AC
Adjust with VR3



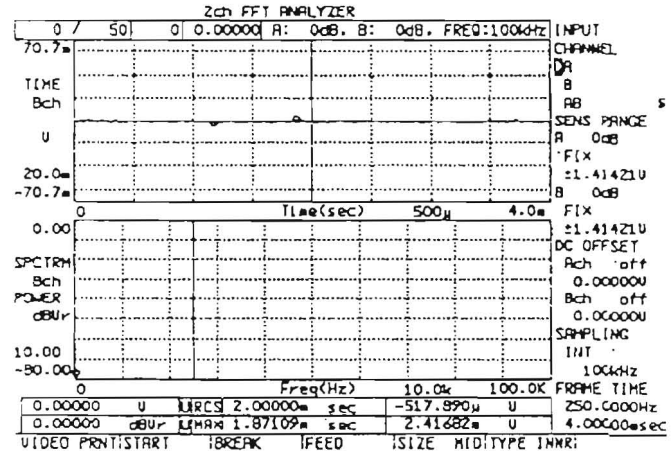
(c) FILTER ON
AC COUPLING


2ch FFT ANALYZER
INPUT
CHANNEL
A
B
AB
SENS RANGE
A 0dB
FIX
±1.41421V
B 0dB
FIX
±1.41421V
DC OFFSET
Ach off
0.000000V
Bch off
0.000000V
SAMPLING
INT
100kHz
FRAME TIME
250.00000Hz
4.000000msec
TIME
Bch
V
SPCTRM
Bch
POWER
dBVr
Time(sec)
Freq(Hz)
VIDEO PRNT
START
BREAK
FEED
SIZE
HDTYPE
INNR

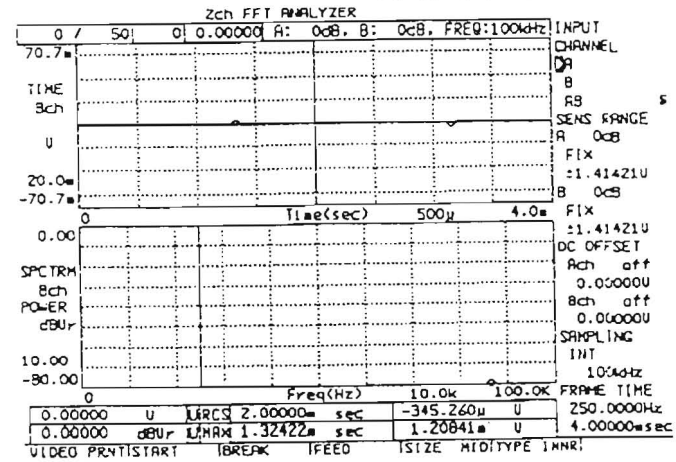
(d) FLTER ON AC COUPLING
Adjustment with VR4



(e) ±10dB range
FLTER ON DC COUPLING



(f) ±10dB
FLTER ON DC COUPLING
Adjustment with VR1



4-1 Offset Adjustment

(1) A/D Module Offset Adjustment

Setting: Sense: 0dB, AC coupling, FLT OFF
Input internal GND(make sure that the offset module is OFF)

Observing the time waveform and spectrum waveform(enlarge the time waveform to such an extent that it is not forced out of the screen), adjust VR3 so that DC components are minimized.

Example) Refer to Fig. (a) and Fig. (b)

(2) Filter Module Offset Adjustment

Next, turn on FLT. When FLT is turned on, the offset is shifted because the offset of the filter is superimposed. Adjust that offset with VR4, viewing the spectrum as well, so that DC components are minimized.

Example Refer to Fig. (c) and Fig. (d)

(3) Heat Amplifier Offset Adjustment

Next, set DC coupling. Adjust the shifted offset with VR1 so that DC components are minimized.

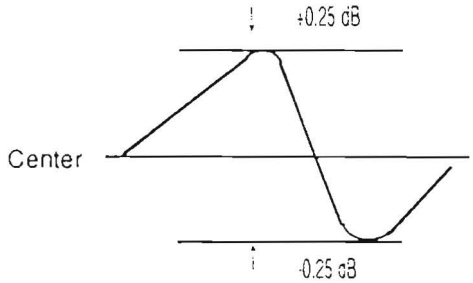
Example Refer to Fig. (e) and Fig. (f)

(4) Make sure that DC components do not change, by repeatedly turning on/off AC/DC and FLT. If there is a change, repeat the above steps 1-3 to make readjustment.

4-2 Frequency Characteristic Compensation

(1) Perform Frequency characteristic compensation in the similar manner as coarse adjustment.(in the maximum frequency range)

0dB (ATT-30 dB)	To ±0.25 dB or less with VC1
+10 dB (ATT-60 dB)	To ± 0.25 dB with VC2

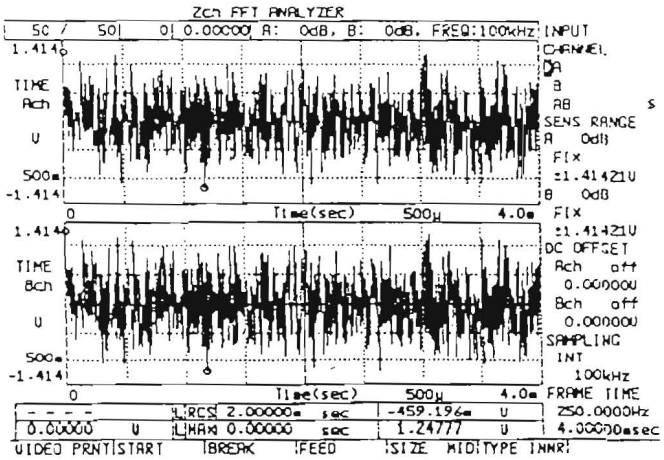


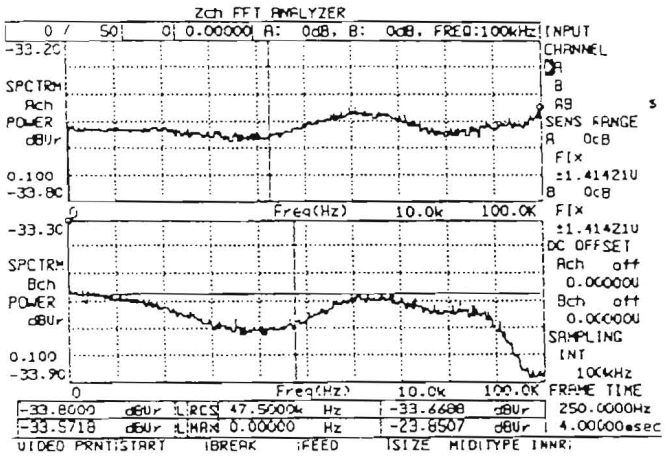
Note: Be sure to adjust at ødB (with VCL), and then, at +10dB (with VC2). Turning VC1 greatly changes adjustment of VC2, and turning VC2 changes adjustment of VC1 only a little. However, it is necessary to observe repeatedly.

(2) After completing the adjustment in 1 above, the specifications must be met in each frequency range as well (10 ranges in total).

100 K Version	20 K Version
100 K 50 K	
20 K 10 K 5 K 2 K 1 K 500 Hz 200 Hz 100 Hz	20 K 10 K 5 K 2 K 1 K 500 Hz 200 Hz 100 Hz
	50 Hz
	20 Hz

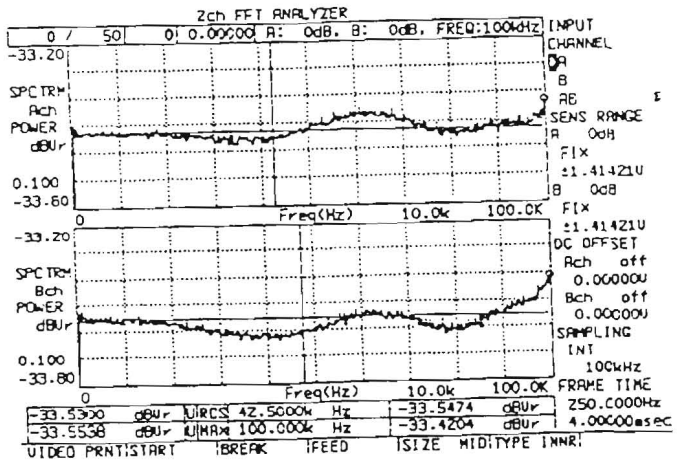
Note: Average when observing a noise, because it makes the screen more visible by reducing the noise.(20 to 30 times)

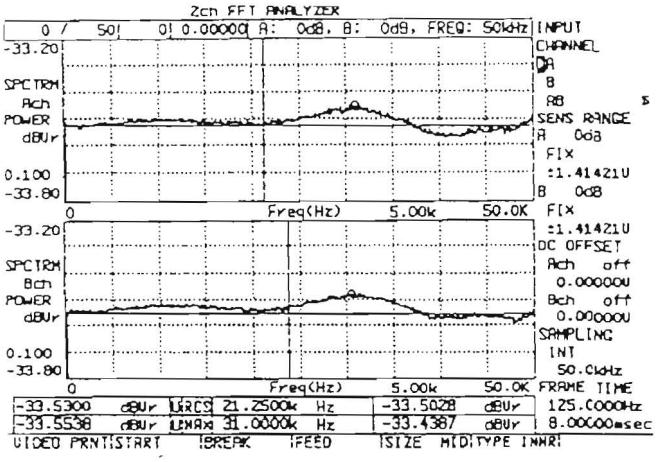


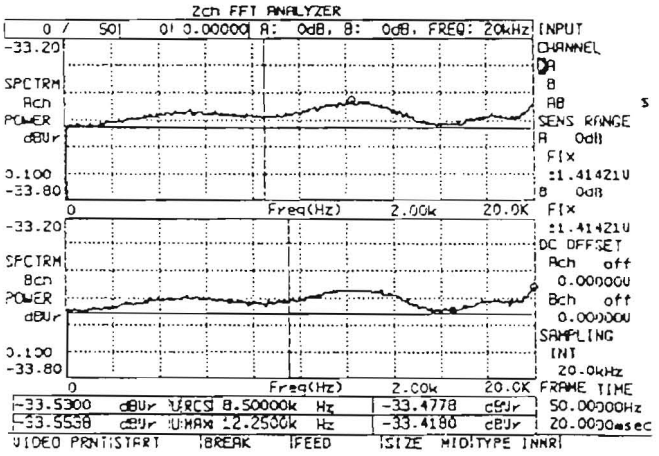


A CH OK

B CH NG




2ch FFT ANALYZER
0 / 50 0 0.00000 A: 0dB, B: 0dB, FREQ: 50kHz
INPUT
CHANNEL
A
B
AB
SENS RANGE
A 0dB
FIX
±1.414ZIV
B 0dB
FIX
±1.414ZIV
DC OFFSET
Ach off
0.000000V
Bch off
0.000000V
SAMPLING
INT
50.0kHz
FRAME TIME
125.0000Hz
8.00000msec
SPCTRM
Ach
POWER
dBVr
-33.20
0.100
-33.80
0
Freq(Hz)
5.00k
50.0K
SPCTRM
Bch
-33.5300 dBVr
-33.5538 dBVr
-33.5028 dBVr
-33.4387 dBVr
VIDEO PRNT START BREAK FEED SIZE MIDI TYPE INNR


2ch FFT ANALYZER
0 / 50 0 0.00000 A: 0dB, B: 0dB, FREQ: 20kHz
INPUT
CHANNEL
A
B
AB
SENS RANGE
A 0dB
FIX
±1.414ZIV
B 0dB
FIX
±1.414ZIV
DC OFFSET
Ach off
0.000000V
Bch off
0.000000V
SAMPLING
INT
20.0kHz
FRAME TIME
50.0000Hz
20.0000msec
SPCTRM
Ach
POWER
dBVr
-33.20
0.100
-33.80
0
Freq(Hz)
2.00k
20.0K
SPCTRM
Bch
-33.5300 dBVr
-33.5538 dBVr
-33.4778 dBVr
-33.4180 dBVr
VIDEO PRNT START BREAK FEED SIZE MIDI TYPE INNR

4-3 Full Scale Adjustment

Like coarse adjustment, input the sine wave of the center frequency of the frequency characteristic in the maximum frequency range and adjust with VR2.

4-4 Noise Level Observation

Specifications }Adjusted

Freq RENG	SENSE RENG	Spec. Adjusted
20 Hz~100 KHz	+30 dB~-10 dB	-85 dB/full or less
20 Hz~20 KHz	-20 dB~-50 dB	-85 dB/full or less
50 KHz~100 KHz	-20 dB~-50 dB	-75 dB/full or less
20 Hz~100 KHz	-60 dB	-70 dB/full or less

Note: When observing the noise level, use FFT computational 32 bits or high-speed operation card.

4-5 High Harmonic Distortion

Use a pure sine generator and observe as a signal source and observe A/D conversion results in the form of spectrum.

Setting of the main body : SENSE RANGE ødB, frequency range max.

Signal source : National VP-7201A
Frequency=1/10 of the frequency range
Output amplitude=±1.4V
Input 10KSIN for the kHz version,
and 2KSIN for the 20kHz version.

Observe high harmonic distortion and make sure that a secondary (tertiary) distrotion factor does not exceed -80dB. If it is exceeding, readjust the A/D module to reduce distortion. (For details, refer to the Adjustment Manual for the A/D module)

4-1-2 Offset Module Adjustment

The offset module is provided as a standard attachment for the 100kHz version, and as an optional one for the 20kHz version.

1. Visual Check

- Check whether the polarities of tantalum match with the silk.
- Check whether the IC is in a correct direction, and whether its pins are not bridged.
- Check whether it is short-circuited with a jumper wire between the pins 15 and 16.

2. Adjustment

Mount the offset module to the anlog board. Mount the analog board to the main body through getter board.

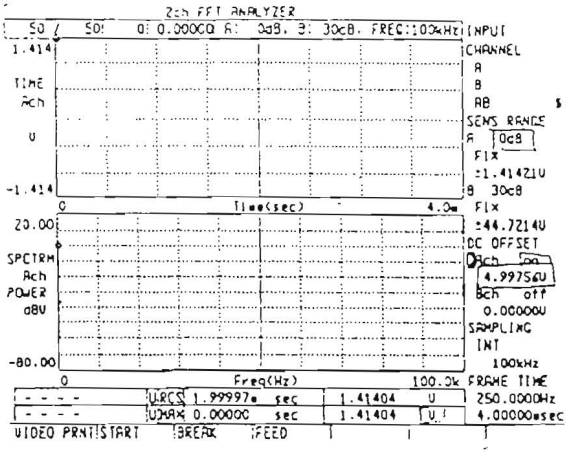
Setting of the main body : Sense: ødB, DC coupling
Internal GND

① Turn on OFFSET, measure between the pin 21 (High) of the offset module and TPø (Low) of the analog board with a voltmeter, and turn VR1 (surface mounting VR) to adjust to 5V (±1mV)

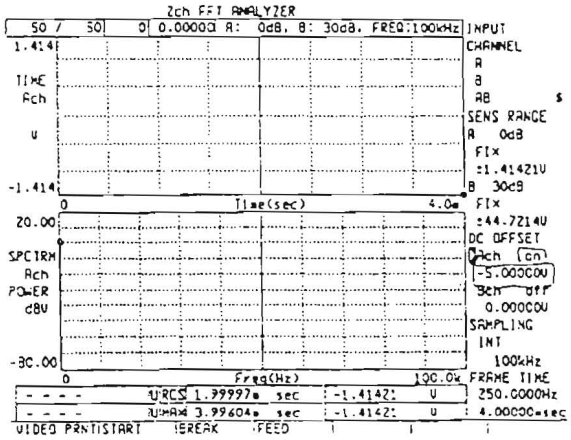
② Measure between TP3 (High) and TPø (Low) of the analog board with the voltmeter, and turn VR2 (surface mounting VR) to adjust to 0 (±1mV).

③ Press ▲ key to adjust to 4,997V. Measure between TP3 (High) and TPø (Low) the voltmeter, and turn VR1 to adjust to 5V.

When the offset module is turned off



When +MAX (+4,997V) is set, the analog board goes over.



When -MAX (-5.000V) is set, the analog board goes over.

4-1-3 Logic Block Adjustment Procedures

Table of Contents

1. Main Board Adjustment Procedures

(1) Prepare the following for adjustment the main board.

External CRT, comparator checking jig, voltage generator, 3.5- inch diskette, and oscilloscope

(2) Set the brilliance control knob on the rear panel to the center.

(3) Install the ROM board in the slot.

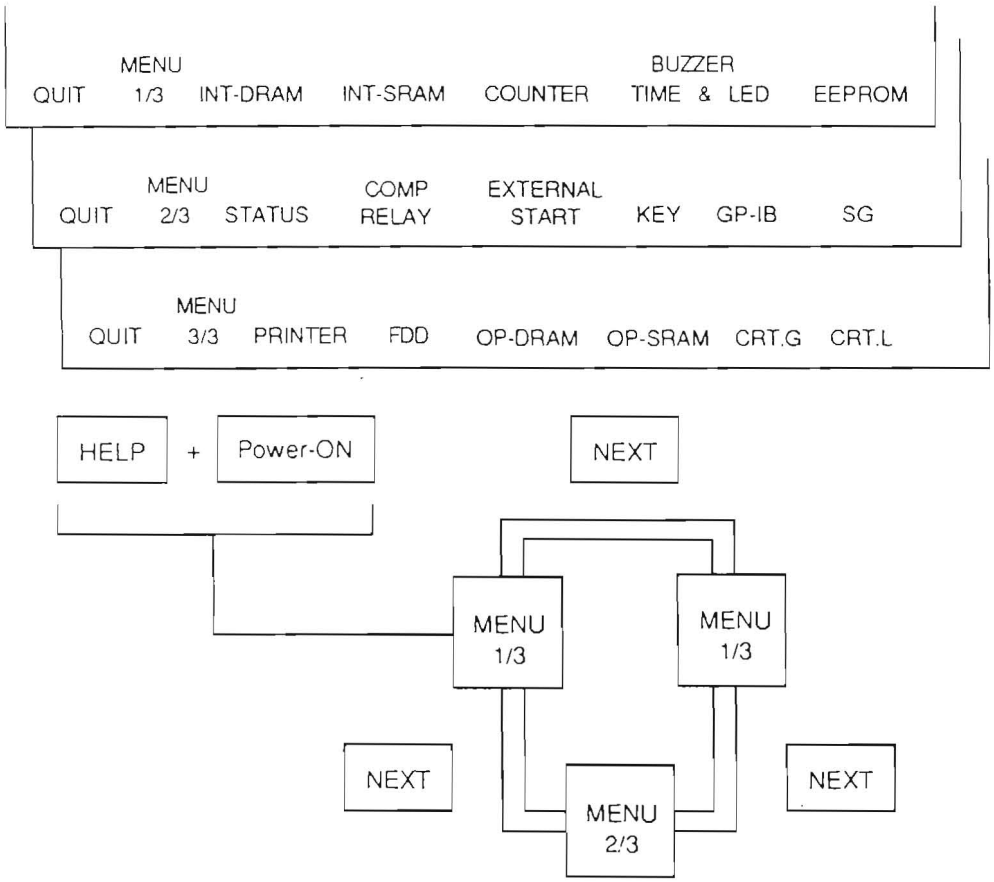
Slot	#1	A/D Ach
	#2	A/D Bch
	#3	
	#4	ROM
	#5	Extension SRAM (rotary switch "E")
	#6	Extension DRAM (slide switch "0"), 4 MB type
	#7	
	#8	
	#9	Printer

Note: Install the floppy diskette on the main board.

(4) Upon start-up, turn on the power switch\tch with the HELP key pressed.
Then, the following screen appears.Changeover of Menu Display

```
        ***  SELF DIAGNOSTIC PROGRAM  ***




          MENU                              BUZZER
    QUIT  1/3  INT-SRAM  COUNTER  TIME & LED  EEPROM
```

- The 3-page menu can be changed over by selecting the function key MENU (NEXT).



(5) Check the following items in accordance with the menu displayed on the screen.

1) INT-DRAM : Internal DRAM CHECKT

Select the function key INT-DRAM and press START. This starts the check. Countdown starts in several tens of seconds, and it is O.K. if "COMPLETE" is displayed. (as shown in the figure below)

```
Warning:This `CHECK-PROGRAM` Destroies the contents
        of the menories.
        If you don`t want to destray them, push `QUIT` Key

CHECK-PROGRAM in progress!
            COUNT DOWN.....1   COMPLETE!



 QUIT START
```

To terminate, press the function key QUIT.

2) INT-SRAM : Internal SRAM check

Selecting the function key INT-SRAM starts the check.

It counts up from 0 and ends with 15. It is O.K. if no error message is displayed.

```
          *** SELF DIAGNOSTIC PROGRAM ***


SRAM CHECK SRAM ADDRESS 15


     MENU                                    BUZZER
QUIT 1/3 INT-DRAM INT-SRAM COUNTER TIME & LED EEPROM
```

3) COUNTER : Counter check

Selecting the function key COUNTER starts the check.

Of 6 sets of numbers, it is O.K. if the 3rd, 4th and 5th are counted.

```
        ***  SELF DIAGNOSTIC PROGRAM  ***

COUNTER CHECK

    ffffd ffff db37 95de 8dc2 fffc


      MENU                                          BUZZER
QUIT 1/3 INT-DRAM INT-SRAM COUNTER TIME & LED EEPROM
```

To terminate, press the function key QUIT.

4) TIME :Time check

Selecting the function key TIME starts the check.

Make sure that the time displayed on the screen is updated every second.

Next, with the ten keys (numerical keys) on the panel, enter a date and a time, finally, press the COMPLEX key. Then, it is O.K. if the set value is displayed as the time.

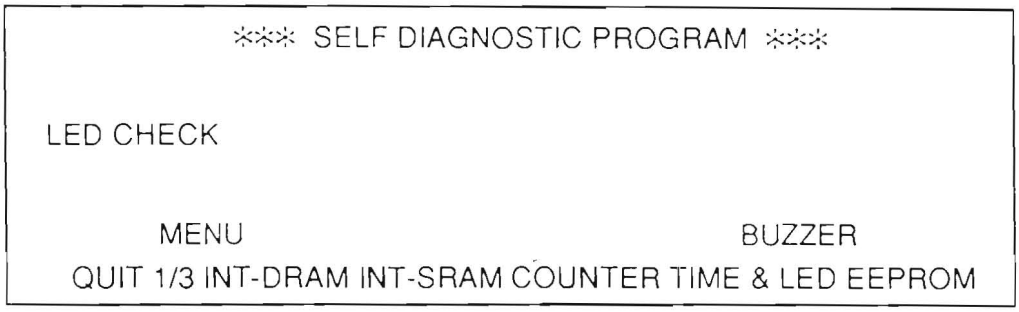
```
        ***  SELF DIAGNOSTIC PROGRAM  ***

TIME SET CHECK

8712311259590 1988 03 17 15 00 00


      MENU                                          BUZZER
QUIT 1/3 INT-DRAM INT-SRAM COUNTER TIME & LED EEPROM
```

To terminate, press the function key QUIT.

5) BUZZER & LED : LED check

Selecting the function key BAZZER & LED starts the check.

Make sure that all the LEDs are illuminated, alternately emitting short and long buzzer sounds. It is O.K. if there is no abnormality.

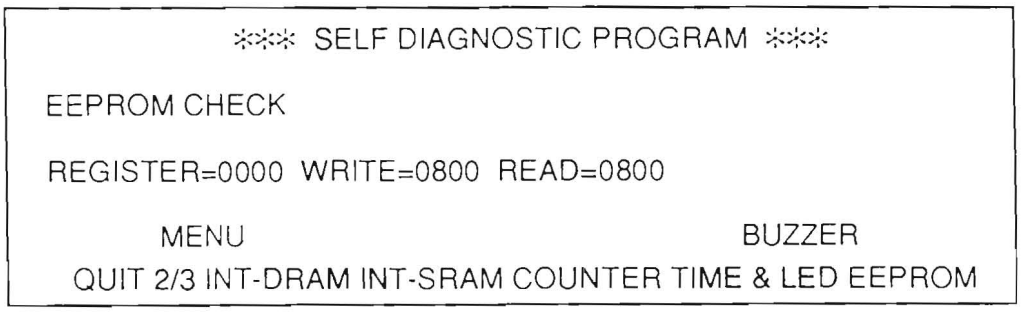


To terminate, press the function key QUIT.

6) EEPROM :EEPROM check

Selecting the function key EEPROM starts the check.

there appear 3 sets of numbers on the screen, all of which start counting up. It is O.K. if REGISTER reaches 003F and the message " EEPROM O.K.!" appears.



7) STATUS : Status check

It is O.K. if the data as shown below are displayed by selecting the function key STATUS.

```
          *** SELF DIAGNOSTIC PROGRAM ***

OPTION STATUS CHECK

  #0   #1   #2   #3   #4   #5   #6   #7   #8
  0f   0f   0f   04   02   0f   0f   0c   07

        MENU          COMP  EXTERNAL
 QUIT  2/3  STATUS  RELAY   STATUS  KEY  GP-IB  SG
```

To terminate, press the function key QUIT.

8) COMP RELAY : Relay check

Connect the checking jig to COMP OUT of the rear panel and select the function key COMP RELAY. It is L.K. if the LEDs of the checking jig are illuminated sequentially.

```
          *** SELF DIAGNOSTIC PROGRAM ***

RELAY CHECK

BUSY MAKE

        MENU          COMP  EXTERNAL
 QUIT  2/3  STATUS  RELAY   START  KEY  GP-IB  SG
```

To terminate, press the function key QUIT.

9) EXTERNAL START : External start check

Selecting the function key EXTERNAL START starts the check.

It is O.K. if "EXTERNAL START IS INPUT" is displayed by shifting the lower toggle switch.

Also, it is O.K. if "MEMORY STORE IS INPUT" is displayed by shifting the lower toggle switch.

```
          *** SELF DIAGNOSTIC PROGRAM ***

EXTERNAL START CHECK


        MENU          COMP  EXTERNAL
  QUIT  2/3  STATUS  RELAY  START  KEY  GP-IB  SG
```

To terminate, press the function key QUIT.

10) KEY :Key check

Selecting the function key KEY starts the check.

Press the keys on the panel one after another. It is O.K. if the name the key pressed coincides with the one displayed.

However, the QUIT and PRINT keys function differently.

The QUIT key gets out of a key check routine, and the PRINT key makes output to the printer. Therefore, they are O.K. if those actions occur, respectively.

```
          *** SELF DIAGNOSTIC PROGRAM ***

 KEY CHECK

UP/LW  0  code=00

        MENU          COMP  EXTERNAL
  QUIT  2/3  STATUS  RELAY  START  KEY  GP-IB  SG
```

To terminate, press the function key QUIT.

11) PRINTER : Printer check

Selecting the function key PRINTER enters the check mode.

Pressing the function key F1 (PRINTER) performs test printing of the printer.

It is O.K. if printing is performed properly.

```
            ***  SELF DIAGNOSTIC PROGRAM  ***

  PRINTER CHECK

F1:TEST PATTERN PRINT
F2:FEED


          MENU
   QUIT  3/3  PRINTER  FDD  CP-DRAM  OP-SRAM  CRT.G  CRT.L
```

12) OP-SRAM : Option SRAM check

Selecting the function key OP-SRAM enters the check mode.

Start the check by selecting the function key START.

It is O.K. if the following is displayed.

```
 Warning : This 'CHECK-PROGRAM' destroies the contents
           of the memories.
           If you son't want to destroy them, push 'QUIT' Key.

             ***  512k-Words SRAM  ***

 CHECK-PROGRAM in progress !

                COUNT DOWN..... 0      COMPLETE !
 QUIT START
```

To terminate, press the function key QUIT.

13) OP-DRAM : Option DRAM check

As in 12, select the function key OP-DRAM to check the option DRAM.

14) Display check (CRT-L)

Pressing the CRT-L key displays the grid. In that state, adjust the CRT, referring to the CRT adjustment procedures.

15) Mother board check

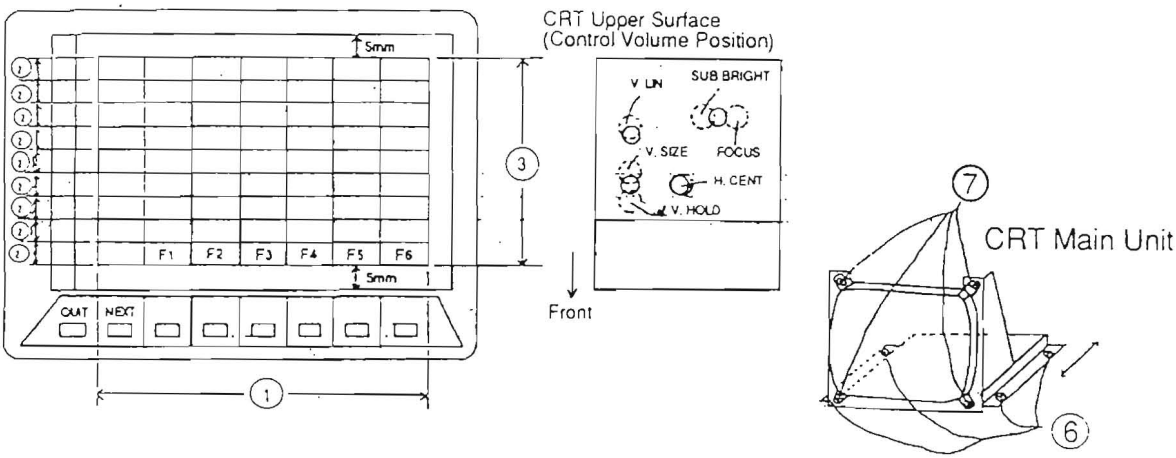
Using an extension card, insert the extension SRAM board into the slot between the A/D and ROM, and make a check of the option SRAM again.

16) FD check (FDD)

Insert a checking disk (formatted one) into the drive and press the FDD key. It is O.K. if the message "PASS" appears.

2. CRT Adjustment Procedures

As with the main board adjustment, start up with the HELP key pressed when the power is turned on.



(1) Press the CRT button of the check menu. The grid pattern is plotted as shown in the figure above.

① Turn H. CENT so that each function key position on the panel will match the position of F1-F6 plotted. (moves to the left/right)

② Turn V. LIN so that each measure will be spaced equally.

③ Turn V. SIZE so that there will be a gap of about 5 mm between the grid pattern and the panel. (moves up and down)

④ Turn the INT control knob located on the rear panel of the main body fully in the direction of increasing brightness. When this is done, turn SUB. BRIGHT to such an extent that the background of the grid pattern does not become bright.

⑤ Turn FOCUS so that the lines of the grid pattern will become clearest.

⑥ See to it that the front of the CRT barely touches the front panel. (Loosen screws and move back and forth)

⑦ Adjust the horizontal lines of the grid pattern at a level. (Loosen screws and twist)

(2) Now, turn off the power once. With the QUIT key pressed, turn on the power again. This effects the FFT mode.

① Connect the external CRT and make sure that it provides a display.

② Turn off the power once. In about 10 seconds, turn it on again and make sure of normal operation.

③ Adjust to the center the two external trigger control knobs on the main board.

④ Connect to the PC-9801 with the GP-IB. Load the file "TST24" onto the PC-9801 and make it run. It is acceptable if "O.K." appears on the screen of the PC-9801. Make sure that the FFT display is a single screen display.

⑤ Set the frequency range to 20kHz (for the 20k version FFT) or 100kHz (for the 100k version FFT). After displaying a test signal, make sure of the following:

a) A trigger should be applied.

b) A trigger strobe should be changed over.

c) If trigger point setting is changed, a trigger position should be dislocated, following it.

d) If trigger level setting is changed, a trigger point level should be dislocated, following it.

e) Display the spectrum and it should be free from distortion.

f) The buzzer should sound as you increase sensitivity of the sense range. The OVER buzzer function should be left turned on.

⑥ When a printer option is attached, adjust a printer head power-on pulse width. After Adjustment, do not change a combination of the main body, printer unit, and printer board.

Note: The procedures are separately descried.

(3) Check for single channel data sampling.

① With the NEXT key, turn on the power.

② Press the HELP key and MEMCLR key to display the menu on the right part of the screen, and turn on CHECK on the third line from the top.

③ After turning on the test signal and setting INPUT and CHANNEL A, press the FRAME key to display the frame menu.

④ After making sure of SEGMENT NUMIO and SEGMENT SIZE 12, change over SINGLE to MULTI displayed at the top of the menu.

⑤ Press the HOLD key to start sampling. When this is done, there must be 8 wavelengths of the time waveform in one screen.

3. Floppy Disk Adjustment Procedures

① Mount the floppy disk drive to the 2ch FFT chassis and install the interface board on the main board.

② Pressing the HELP key, turn on the power to start a hardware check program.

③ Set a formatted disk in the floppy disk drive.

④ Select a floppy check (FDD) from the menu.

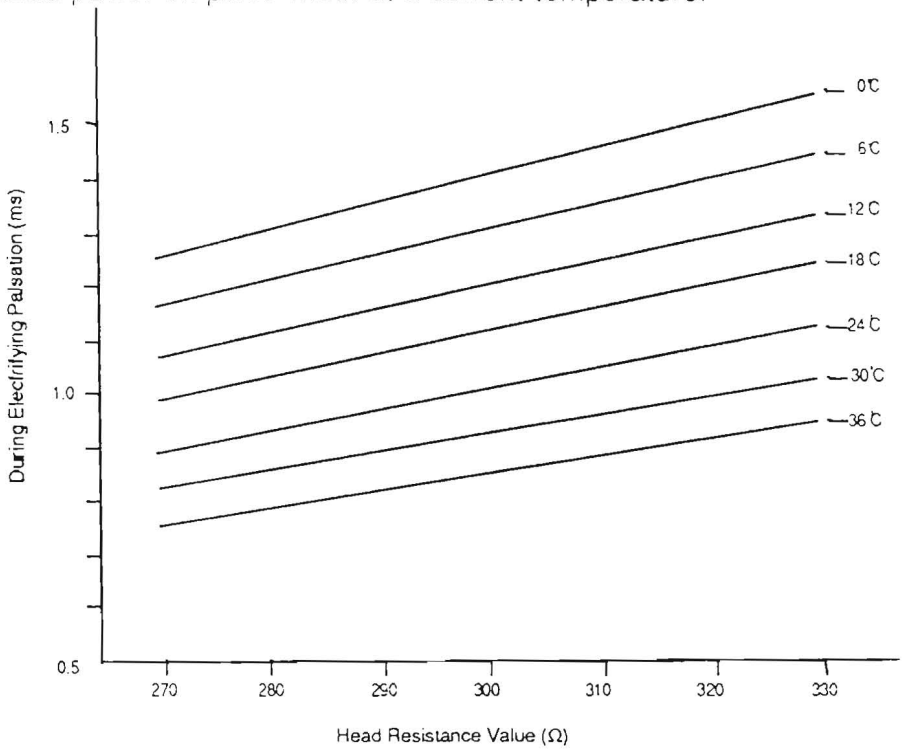
⑤ After pressing the FDD key, the drive is accessed and the message "PASS!" must appear.

4. Video Printer Adjustment Procedures

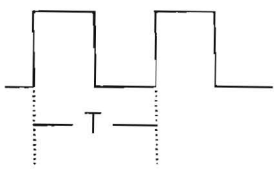
① Read the head resistance value inscribed on the back of the flexible board of the printer.

② Connect the + pole of the digital voltmeter to the pins 18 and 19 of the connector attached to the flexible board, and the - pole to the pins 16 and 17, and turn the power control knob R214 to adjust to 12.0V.

③ Measure a room temperature, and from the table below, obtain the head power-on pulse width at a current temperature.



④ Connect a synchroscope to TP2 of the printer driver board and calculate a pulse interval time width. Turn the trimmer capacitor so that the time width will be the value of;



T (calculated head power-on pulse width) ÷45

When the time width cannot be obtained only by means of the trimmer capacitor, attach a ceramic capacitor (10s pF 100 pF) to the pattern next to the trimmer capacitor.

Note: Make this adjustment when the printer head is equal to a room temperature. When the printer head has been warmed such as immediately after printing, wait until it is cooled off.

⑤ Make a hard copy of the screen to check to see quality of printing.

5. 1 M-/2 M-Word Memory Card Adjustment Procedures

① With the switch on the 1 M-/2 M-word memory card shifted to 0, install it in the option slot #6 of the 2ch FFT (from the CRT).

② Pressing the HELP key, turn on the power to start up a check program.

③ Press the OP-DRAM key.

④ Make sure that the message "1 Mega words" appears when the 1 M-word memory card is installed, and that "2 Mega words" when OP-04 is installed.

⑤ Press the START key to start a check.

⑥ It is O.K. If the message "COMPLETE!" is displayed.

6. 512k-Word CMOS Memory Card Adjustment Procedures

① With the rotary switch on the extension SRAM shifted to "E", install it in the option slot #5 of the 2ch FFT.

② Pressing the HELP key, turn on the power to start a check grogram.

③ Press the OP-SRAM key.

④ Press the START key to start a check.

⑤ It is O.K. if the message "COMPLETE!" is displayed.

4-1-4 CRT Unit Adjustment Procedures

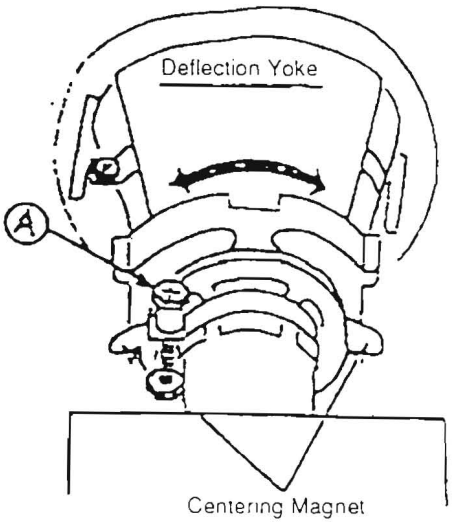
Table of Contents

1. Adjustment Procedures

1-1 Screen Tilt Adjustment (Deflection Yoke)

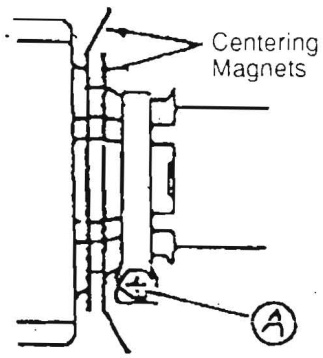
Loosen the screw A use for fixing the deflection yoke. Viewing the raster or display screen, adjust the screen tilt by turning the deflection yoke to the left and right.

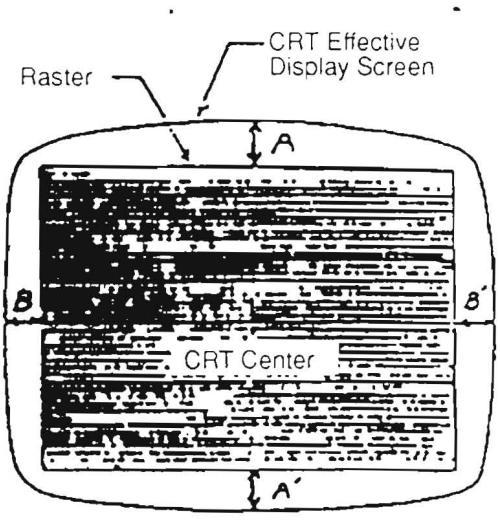
After completing the adjustment, insert the deflection yoke into the CRT neck fully and fix it with the screw A. Tighten the screw A with a tightening torque of 5 to 6kg/cm. Be careful not to break the CRT neck.



1-2 Screen Centering Adjustment (Deflection Yoke Centering Magnet)

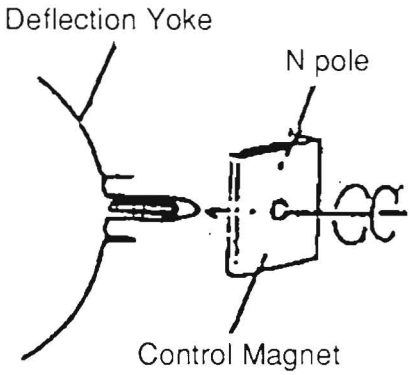
Turn the two centering magnets to the left and right so that the raster will be located at the center of the CRT. (A = A', B = B')





1-3 Geometrical Distortion Adjustment (Deflection Yoke Distortion Control Magnets)

As shown in the figure in 1-4, the geometrical distortion of the image (rester) can be adjusted by turning the control magnets attached at 8 places, respectively.

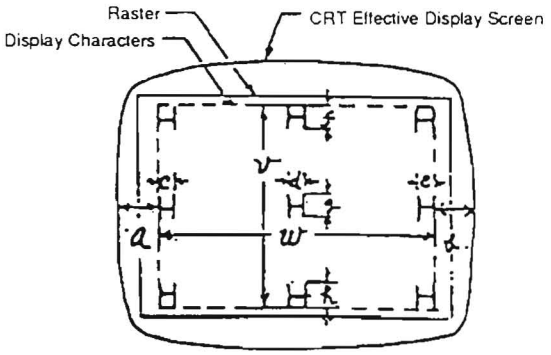


1-4 H. CENT (Horizontal Position Control) VR1

Make adjustment so that the horizontal position of the display characters will be located at the center of the CRT. (a = b)

They are moved to the right by turning the control knob to the right, and to the left by turning it to the left.

(Adjust from the parts mounting surface)



1-5 H. SIZE (Horizontal Size Control) L2

Adjust the horizontal size of the display characters.(W in the figure above)

The size is widened by turning the core of L2 to the right, and narrowed by turning it to the left. For this core, use a plastic adjustment rod. (Adjust from the parts mounting surface)

1-6 H. LIN (Horizontal Linearity Control) L1

Adjust the horizontal linearity of the display characters. (c = d = e in the figure above)

1-7 V. HOLD (Vertical Sync. Control) VR3

Adjust almost to the center of the range which is vertically synchronized, by turning the control knob to the left and right.

1-8 V. SIZE (Vertical Size Control) VR2

Adjust the vertical size of the display characters. (V in the figure above)

The size is widened by turning the control knob to the right, and narrowed by turning it to the left.

(Adjust fro the parts mounting surface)

1-9 V. LIN (Vertical Linearity Control) VR4

Adjust the vertical linearity of the display characters. (f = g = h on the front)

(Adjust from the parts mounting surface)

1-10 FOCUS (Focus Control) VR7

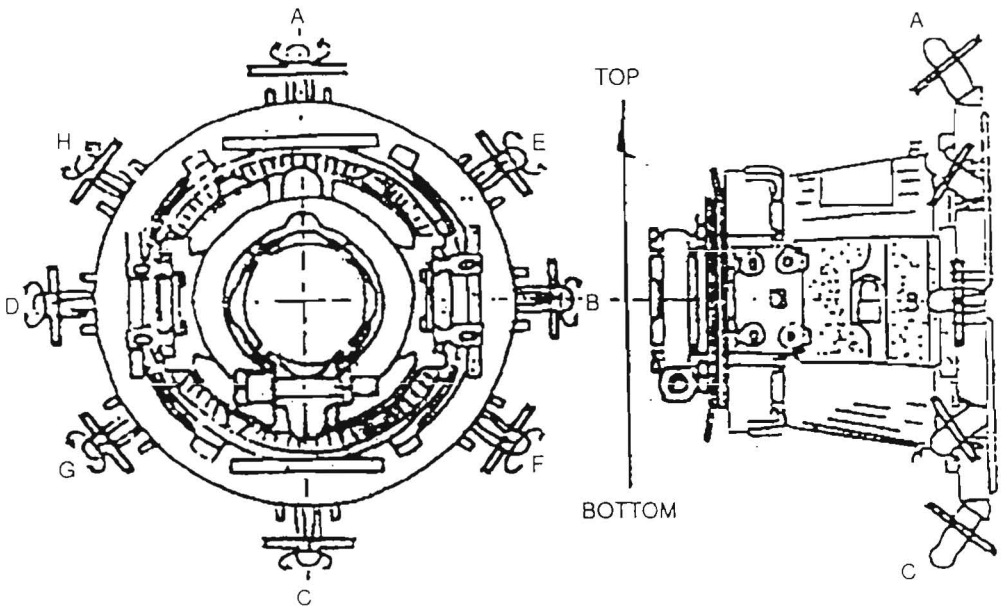
Adjust so that the display characters will become clear.

1-11 SUB. BRIGHT (Sub-brightness Control) VR6

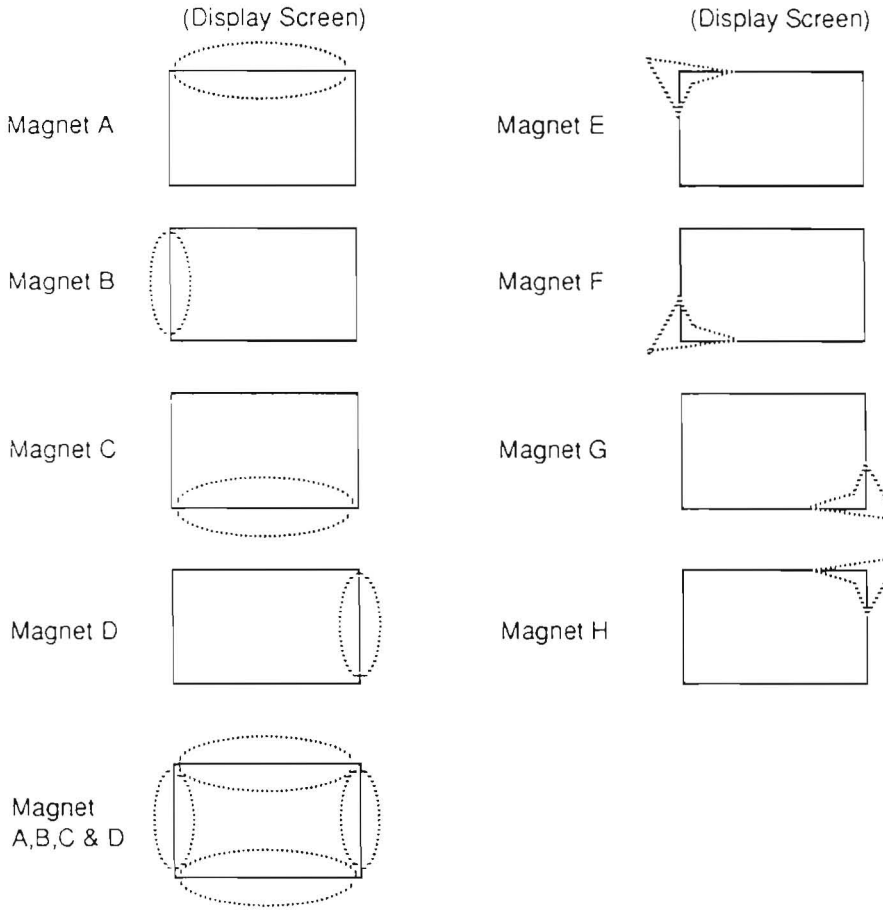
Turn the internally connected BRIGHTNESS control knob fully to the right, and adjust the SUB. BRIGHT control knob so that other portion than the display characters (back raster) will become slightly visible.

Brightness is increased by turning this control knob to the right, and decreased by turning it to the left.

(Adjust from the parts mounting surface)



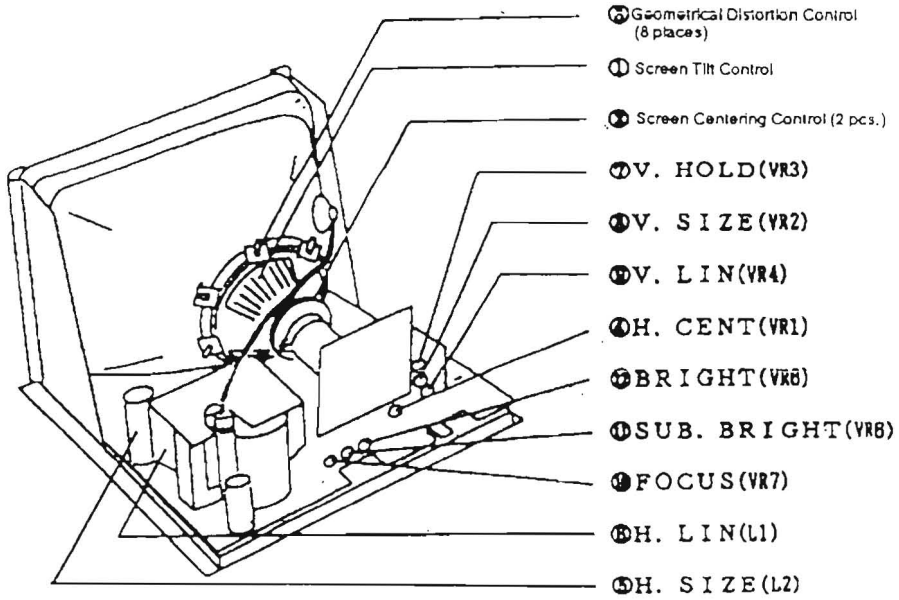
Relations between Control Magnets and Screen Distortion



1-12 BRIGHT (Brightness Control) VR5

Turn the control knob fully to the right.

2. Names and Function of Controls



(1) Screen Tilt Control

Loosen the screw A used for fixing the deflection yoke. Viewing the raster or display screen, adjust the tilt by turning the deflection yoke to the left and right.

(2) Screen Centering Control

Turn the two centering magnets to the left and right so that the raster will e located at the center of the CRT.

(3) Geometrical Distortion Control

Adjust geometrical distortion by turning the control magnets at 8 places. (There are not always 8 magnets provided depending on the relationship between the deflection yoke and CRT.)

(4) H. CENT (VR1)

Make adjustment so that the display screen will be located at the mechanical center of the CRT.

(5) H. SIZE (L2)

Adjust the horizontal size of the display screen.

(6) H. LIN (L1)

Adjust the horizontal linearity of the display screen.

(7) V. HOLD(VR3)

Make adjustment to synchronize with a vertical drive input signal (VD).

(8) V. SIZE (VR2)

Adjust the vertical size of the display screen.

(9) V. LIN (VR4)

Adjust the vertical linearity of the display screen.

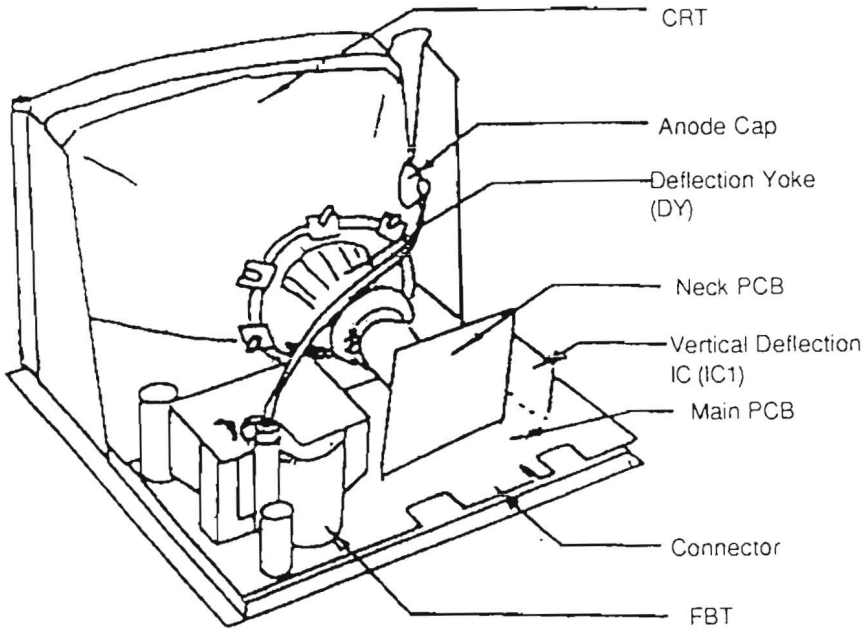
(10) FOCUS (VR7)

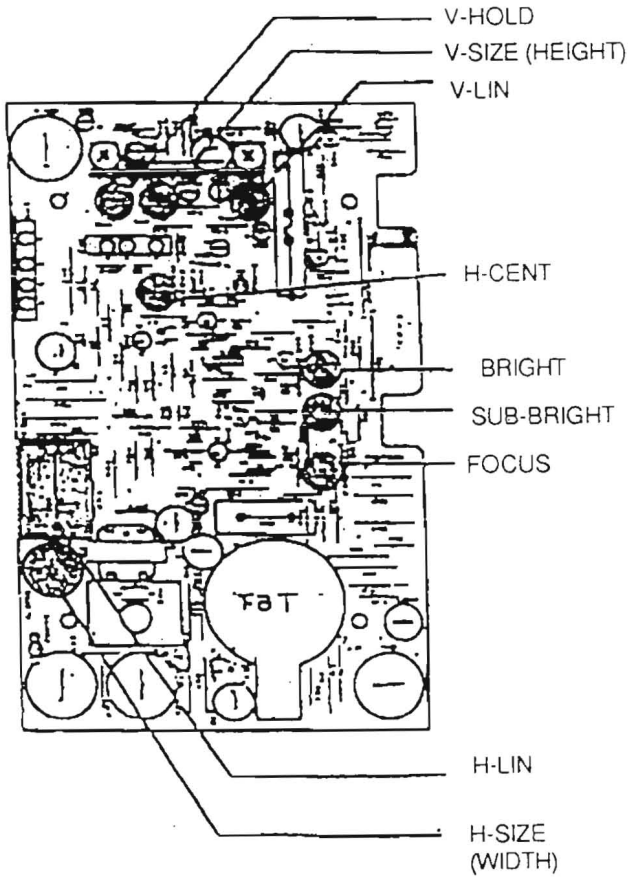
Adjust the focus of the display screen. (internal semi-fixed)

(12) BRIGHT (VR5)

Adjust the brightness of the display screen. (internal semi- fixed)

3. Parts Layout Drawing





4-1-5 Power Unit Adjustment Procedures

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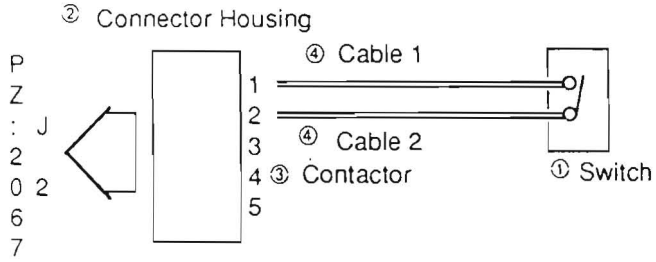
1. Preparation for Power Unit Adjustment

The following measuring instruments and jigs are required for adjustment.

Digital voltmeter	Must be able to display 3.5 digits or more.
Oscilloscope	2-channel input, Frequency band : 20 MHz or more, Voltage input range : 5mV/min.
Oscilloscope probe	10 :1 1 pc., 100 :1 1 pc.
DC power source	Output voltage : Must be variable between 0-15V Output current : 0.5 A or more
Slide transformer	Output voltage : Must be variable between 0-264V. Output current : 2 A or more

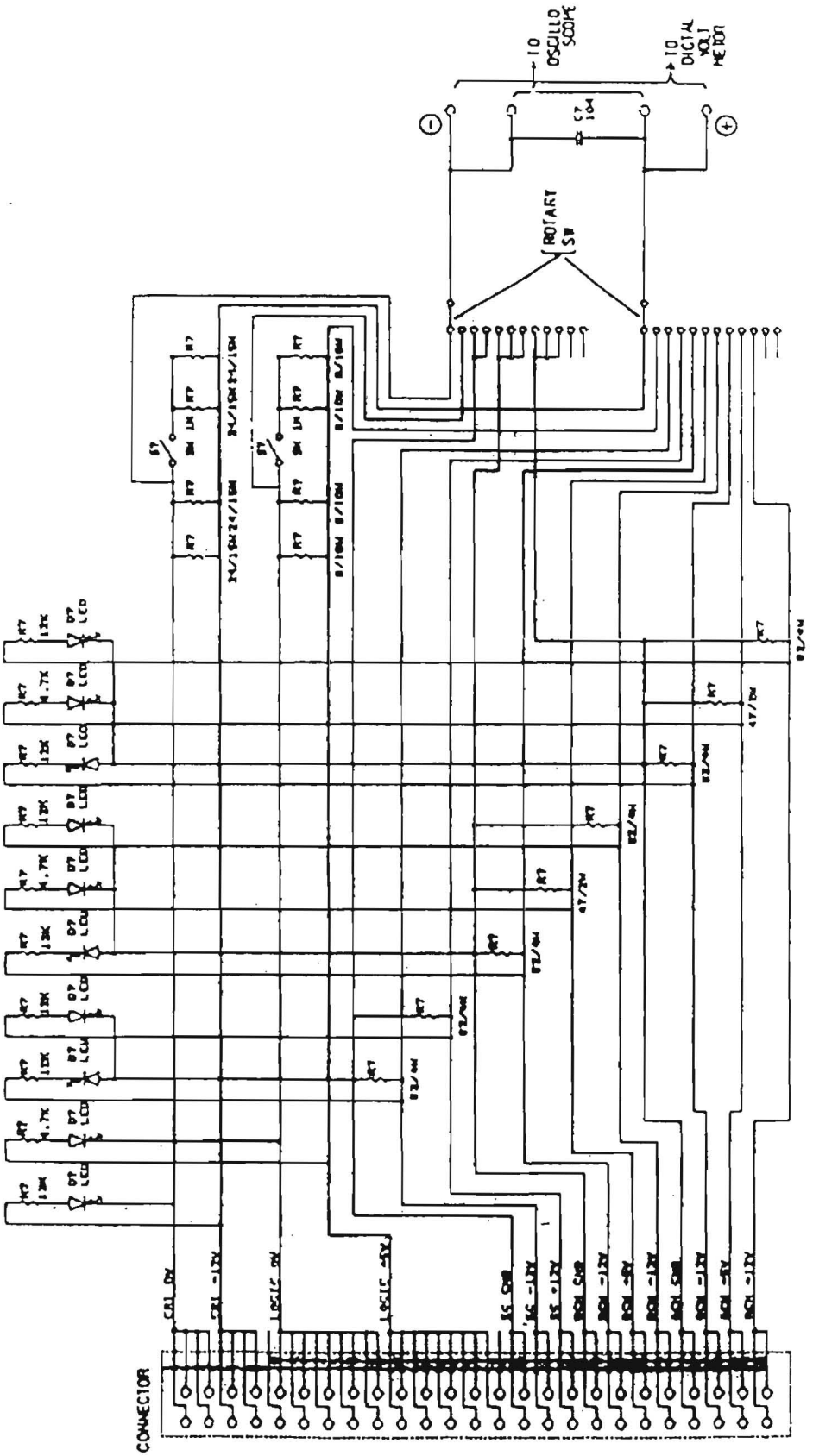
Power ON/OFF switch



Parts Configuration

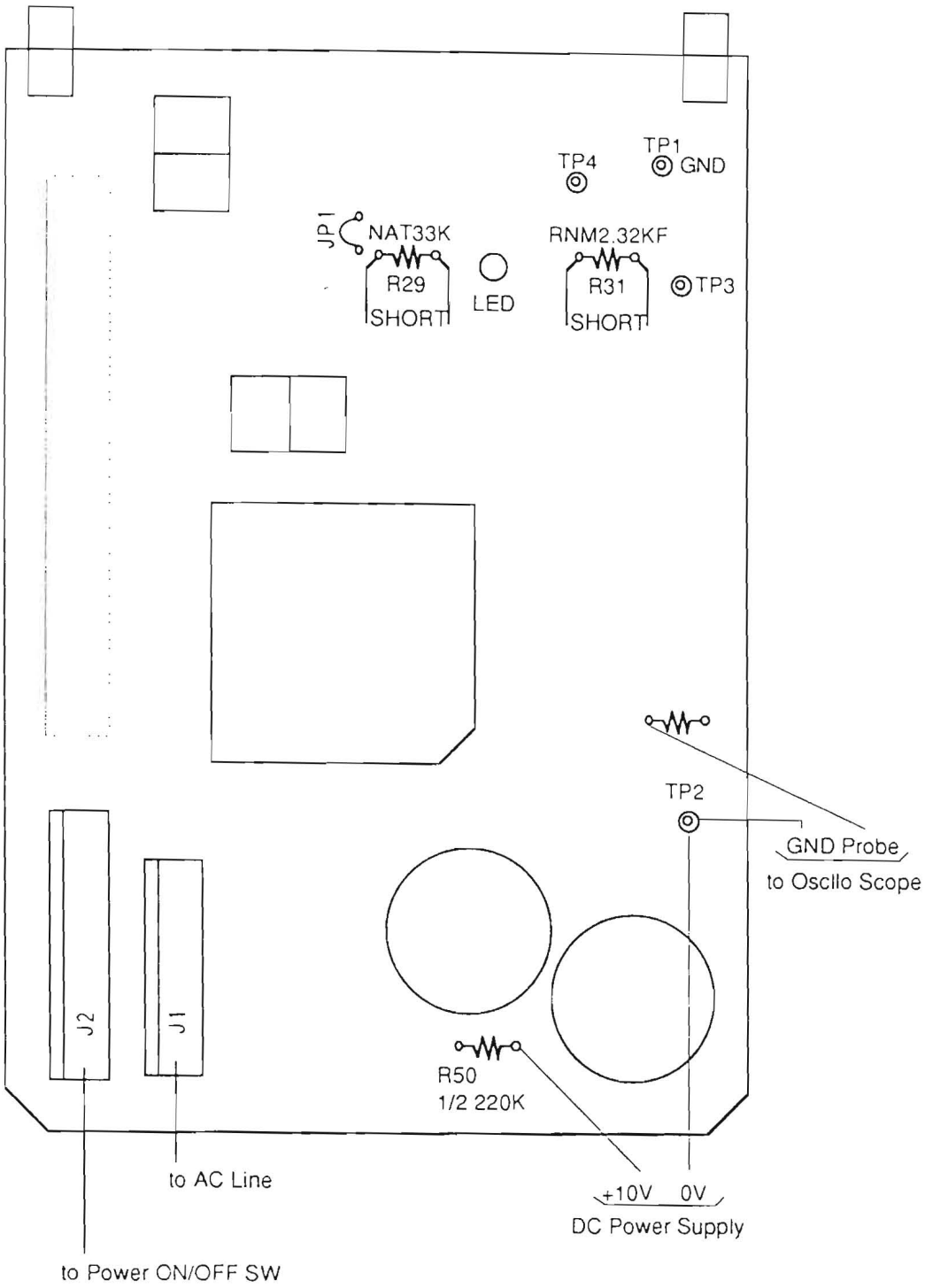
No.	Name	Type (Maker)	Quantity
①	Power switch		x1
②	Connector housing	640250-6(AMP)	x1
③	Contractor	640706(AMP)	x2
④	Cables 1, 2	AWG #20	1=50cmx2

Power loading device
(Refer to the Power Loading Device Circuit Diagram) 1 unit

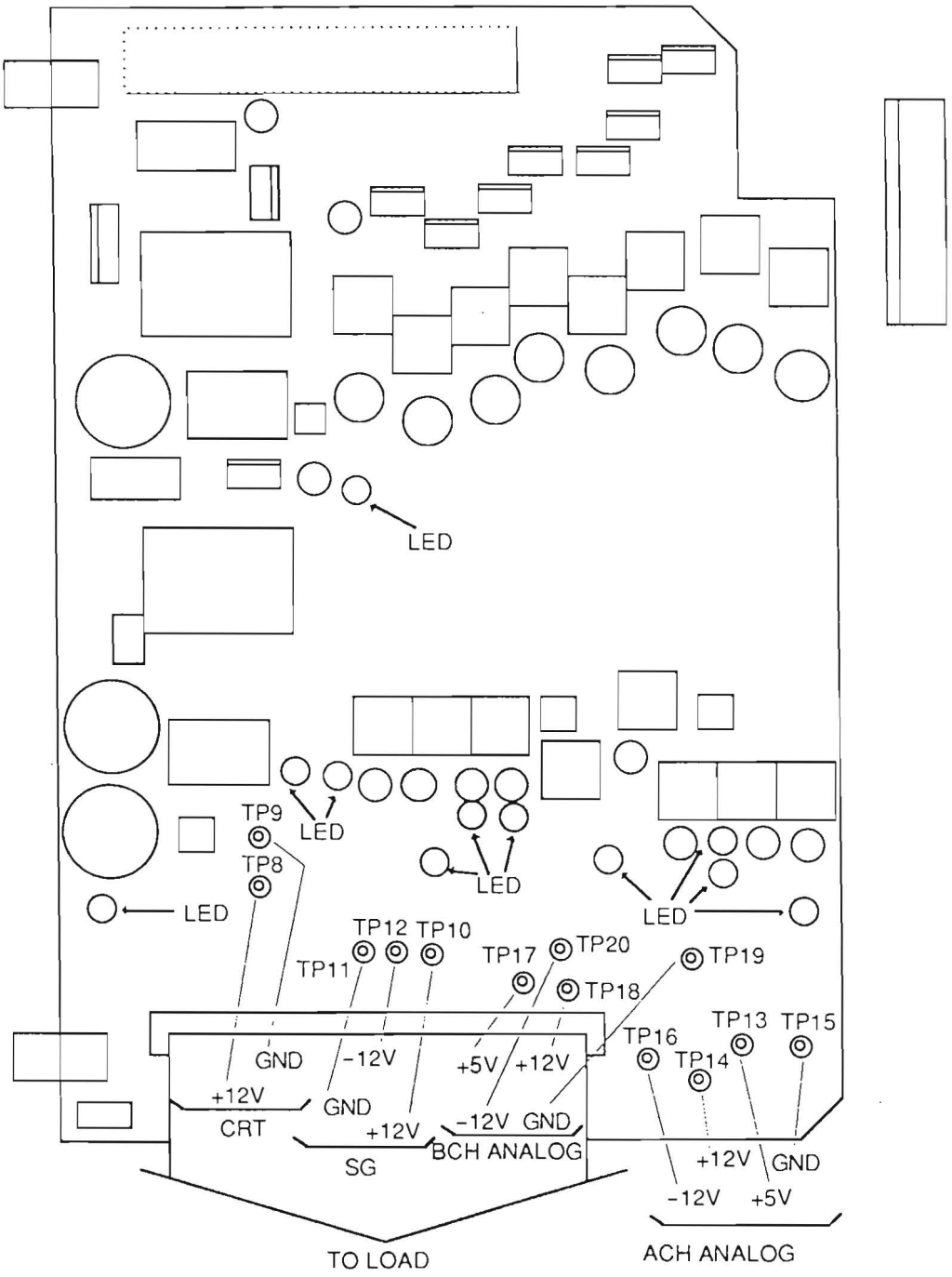

TO OSCILLO SCOPE
TO DIGITAL VOLT METER
ROTARY SW
CONNECTOR

2. Connection of Jig

PZ : 2067 Connection of Jig 1/2



PZ : 2068 Connection of Jig 2/2



3. Adjustment

The power board PZ:2067 has an input power circuit, and PZ:2068 has an output power circuit.

Of the control knobs mounted to the power board, turn R20 fully to the left, and R114, R214, R319, and R338 fully to the right.

3-1 Power Control Circuit Check

Note: Do not connect the power source to the AC line.

① Power line check of the control circuit

Connect the - (minus) side of the DC power source to TP1, and the +(plus) side to TP2, and apply 10V.

When this is done, it is normal if the LED of D17 is illuminated.

② Drive circuit check Control circuit and drive circuit check

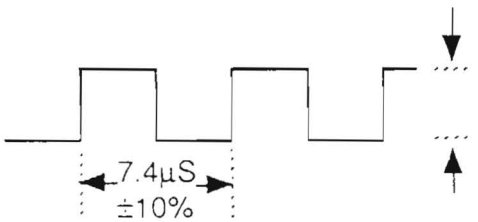
Make the following measurement in the state of ①.

Connect GND of the oscilloscope to TP1, the probe to R11, and short-circuit the both ends of R29 with a short pin or tweezers.

(to stop a low input voltage protective action)

When this is done, the waveform of the oscilloscope must be as follows.

Also, the voltage at R11 must be 0V when the short-circuit of R29 is removed.



③ Power FET check

Connect the probe of the oscilloscope to TP3 (power FET drain), the + (plus) side of the DC power source to the C6 side of R50 (input + DC line), and apply +10V.

With the observation value of the oscilloscope, the value of TP3 must be +10V. If not, the FET could be broken. (because the gate of the FET is 0V)

3-2 Output Check

Apply an AC line voltage to the power input.

When this is done, all the LEDs attached to the secondary-side board PZ:2068 must be illuminated. If there is any LED unilluminated, its corresponding power circuit is defective

3-3 Adjustment of 12V CRT Power

Connect the digital voltmeter to the CRT check terminals of the jig or connect the + pole and - pole of the voltmeter to RP8 and TP9, respectively.

When the control knob R214 is turned and an output voltage exceeds 13.1-15.4V, make sure that an overvoltage protective function works to stop the power source.

With R214, adjust the output voltage to 12.5V.

Measure an output voltage of 12V with the oscilloscope; output voltage ripples must be 100mVp-p except a power source spike noise. Make sure that when an output current of 4.4-6.5 A flows, a current limiting function works to reduce the output voltage.

3-4 Adjustment of 5V Logic Power

Connect the digital voltmeter to the logic check terminals of the jig or connect the + and - poles of the voltmeter to TP6 and TP7, respectively.

When the control knob R114 is turned and an output voltage exceeds 5.8-6.5V, the overvoltage protective function works to stop the power source.

With R114, adjust the output voltage to 5.4V.

Measure a 5V output voltage with the oscilloscope and output voltage ripples must be 100mVp-p or less except power source spike noise. When an output current of 4.4-6.5 A flows, the current limiting function works to reduce the output voltage.

3-5 Adjustment of +5 & ±12V Analog/SG Power

- +5V Adjustment

  Ach Connect the voltmeter to the jig or its +and -sides to TP13 and TP15, respectively.
  Likewise, connect the probe of the oscilloscope. With R319, adjust the output voltage to 5.3-5.5V.
  Output ripples must be within 10mVp-p except power source spike noise.

  Bch Connect the voltmeter to the jig or its + and - sides to TP17 and TP19, respectively.
  Likewise, connect the probe of the oscilloscope. With R338, adjust the output voltage to 5.3-5.5V.
  Output ripples must be within 10mVp-p except power source spike noise.

- ±12V check

  Ach +12V Connect the voltmeter to the jig or its + and - sides to TP14 and TP15, respectively.
  Likewise, connect the oscilloscope.
  The output voltage must be between +12.3 and 12.7V.
  Output ripples must be within 10mVp-p except power source spike noise.

  Ach -12V Connect the voltmeter to the jig or its + and - sides to TP16 and TP15, respective. Likewise, connect the oscilloscope.
  Likewise, connect the oscilloscope.
  The output voltage must be between +12.3 and 12.7V.
  Output ripples must be within 10mVp-p except power source spike noise.

  Bch +12V Connect the voltmeter to the jig or its + and - sides to TP18 and TP19, respectively.
  Likewise, connect the oscilloscope.
  The output voltage must be between +12.3 and 12.7V.
  Output ripples must be 10mVp-p except power source spike noise.

  Bch -12V Connect the voltmeter to the jig or its + and - sides to TP20 and TP19, respectively.
  Likewise, connect the oscilloscope.
  The output voltage must be between -12.3-12.7V. Output ripples must be within 10mVp-p except power source spike noise.

SG +12V Connect the voltmeter to the jig or its + and - sides to TP10 and TP11, respectively.
Likewise, connect the oscilloscope.
The output voltage must be between +12.3-12.7V.
Output ripples must be within 10mVp-p except power source spike noise.

SG -12V Connect the voltmeter to the jig or its + and - sides to TP12 and TP11, respectively.
The output voltage must be between -12.3- 12.7V.
Output ripples must be within 10mVp-p except power source spike noise.

3-6 Input Current Protection Check

Short-circuit the both ends of the resistor R31 of the board PZ:2067, and make sure that the output voltage hardly comes out or the power source stops.

3-7 AC Line Voltage Fluctuation Check

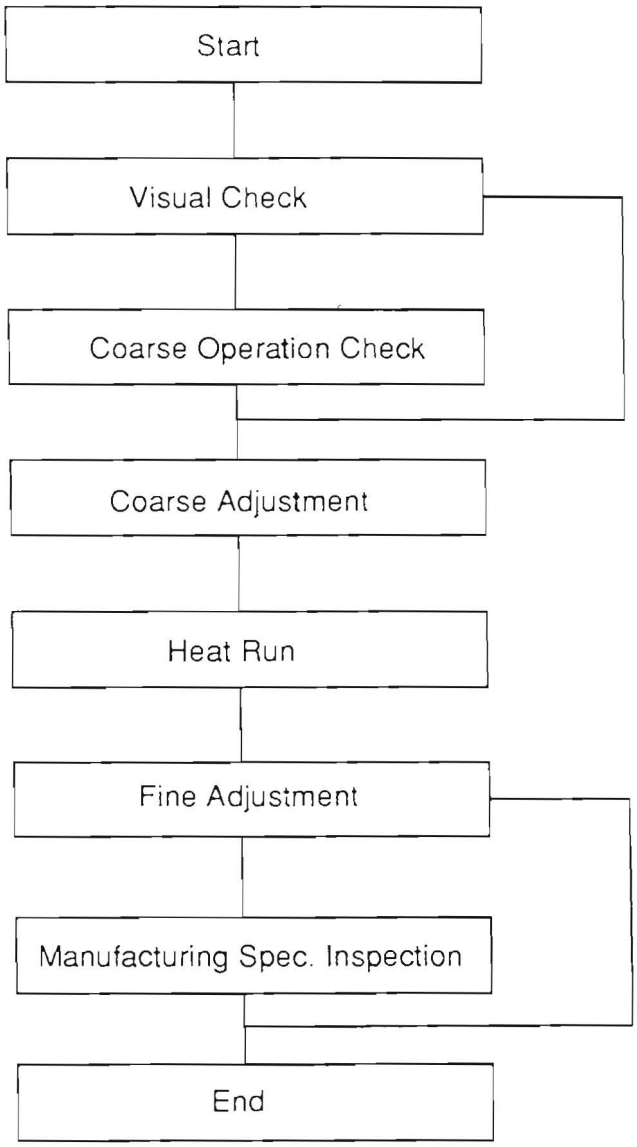
Connect the probe of 100 : 1 to TP3 of the primary-side power board PZ:2067, and GND to TP1. Change and AC line voltage to 90V through 264V with the slide transformer, observe a switching waveform with the oscilloscope, and make sure that the Waveform changes smoothly.

4-1-6 SG Adjustment Procedures

Table of Contents

1. Outline of Adjustment Procedures

The following outlines option SG (Signal Generator) card adjustment procedures.



2. Visual Check

Check for an IC direction.
Note that although the logic block is in a fixed direction, the analog block has various directions.

Check whether the polarities of the tantalum and chemical capacitors match those of the silk. For C56, however, the silk polarities are wrong and the capacitors are mounted opposite the silk.

Check whether each part is properly soldered and its point are not exposed.
If the pons are too long, they may come into contact with the shielding plate of the main body.

On the parts mounting side, check the height of each part.
Make sure that a maximum height is 8-9 mm and not more.
Any parts exceeding this height may come into contact with the shielding plate of the main body.
(Pay particular attention to the height of Q13 and Q14.)

Make sure that each wiring is properly made.

Make sure that the output connector J1 (TMP-J01X-A2) is low enough and not touching the radiating plate. If it is in contact, it may deteriorates performance.

3. Coarse Operation Check

After visual check is completed, turn on the power and check for operation.
First, insert the SG card into the main body slot through the extension board (PZ:2073), and connect the SGOUT cable coming from the front panel to the SG card output connector J1. Connect SGOUT of the main body front panel to the analog input connector ACH INPUT (or BCH INPUT) of the main body to make it ready to monitor SG card output.
(For the slot position of the main body, refer to the figure below)
Then, turn on the power and check the following.

① The LED (D3) must be illuminated.

② View the monitoring screen and the SG output must be around 0V.

③ A sine waveform must be outputted by turning on SG.
(Initially, the mode and level have been set to Sine and 504mV, respectively.)

If the above items are satisfied, you are through with coarse operation check.

4. Coarse Adjustment

After completing the coarse operation check, proceed to coarse adjustment after running for 10-20 minutes at a normal temperature.

4-1 Reference D/A, Signal Generator D/A Block;Offset, Full Scale Adjustment

[Setting] SG-ON MODE : -DC LEVEL: 4.98V

(1) Observing the voltage between TP1 and GND, turn VR1 to adjust it to -4.98V (within ±10mV). When it cannot be fully adjusted with VR1, change over the SW1 in either adjustable direction of 1 or 2.

Note: When setting LEVEL, entering "5V" causes automatic re-setting to 4.98V.

(2) Next, set MODE to +DC. Calculate how many mV a +DC value is shifted from a -DC value in terms of absolute value, and adjust with VR4 so that the absolute +DC value will become equal to the absolute -DC value.(so that the difference will be within ±20mV)

[Example] -DC -4.98V (adjust in 1-1)

+DC +5.04V

Since +DC is larger by 60mV, 60mV/2 = 30mV with VR4, decrease the +DC value. It is ±5.01V here.

(3) Repeat 1-1 to adjust to ±4.98V.

4-2 Filter Block; Offset, Full Scale Adjustment

[Setting] SG-ON MODE: -DC LEVEL: 0V

(1) Observe the voltage between TP2 and GND, and with VR9, adjust it to 0V (within ±1mV).

(2) Next, set LEVEL to 4.98V. With VR6, adjust the voltage between TP2 and GND to 1.57V (within ±10mV).

4-3 Range Amplifier Block; Offset Adjustment

[Setting] SG-ON MODE : -DC LEVEL : 0V

(1) Turn VR8 to adjust the voltage between TP3 and GND to 0V (within ±1mV).

(2) Turn VR 8 to adjust the voltage between TP4 and GND to 0V (within ±1mV).

Note: When an adjustment range is insufficient, connect a regulating resistor to R101 or R 102 in parallel.
(On the soldering surface, use a metal film resistor as the regulating resistor.)
For - directional offset: 680 K for R102 (+1.5mV up)
For + directional offset: 680 K for R101 (-1.5mV down)

4-4 Offset block; Offset, Full Scale Adjustment

[Setting] SG-ON MODE : -DC LEVEL: 0V
OFFSET: ON-0V

(1) Turn on OFFSET, set LEVEL to 0V, and observing the voltage between TP4 and GND, turn VR3 to adjust it to 0V (within ±1mV).

(2) Next, set OFFSET to +4.961V, and turn VR2 to adjust the voltage between TP4 and GND to +4.96V (within 10mV). When it cannot be adjusted by turning VR2, change over the SW2 to either 1 or 2 and make adjustment.

(3) If the full scale is adjusted by performing 4-2, the offset is shifted. Perform 4-1 again.

(4) If the offset is adjusted by performing 4-3, the full scale is shifted. Perform 4-2 again.

(5) Set the level to -5V and make sure that the voltage between TP4 and GND is -5V (within ±20mV).

5.Heat Run

After completing coarse adjustment, turn on the power and perform a heat run for about 6-8 hours in a high-temperature room (40°C).

If the SG running jig is used at this time, up to 6 SG cards can be run at one time.

6.Fine Adjustment

After completing the heat run, perform fine adjustment. Fine adjustment should be also carried out in the similar procedures as coarse adjustment.

Full Scale, Offset	Adjustment
↓	
Offset Block	Adjustment
↓	
Filter Block "Q"	Adjustment
↓	
Filter Block "Wn"	Adjustment
↓	
Amplitude	Check
↓	
Noise	Check
↓	
High Harmonic Distortion Factor	Check
↓	
End	

6-1 Reference D/A, Signal Generator D/A Block; Offset, Full Scale Adjustment

[Setting] MODE : -DC LEVEL : 4.98V OFFSET : OFF

(1) Observing the voltage between TP1 and GND, change over the mode to +DC and -DC alternately, and turn VR4 to adjust both positive and negative outputs almost equal.(The difference must be 0V (within ±10mV). For details, refer to Coarse Adjustment, 1-1.

(2) Next, set LEVEL to 4.98V, and turn VR1 to adjust both positive and negative values to ±4.98V (within ±10mV).

6-2 Filter Block; Offset, Full Scale Adjustment

[Setting] MODE : -DC LEVEL : 4.98V OFFSET : OFF

(1) Turn on SG and turn VR6 to adjust the voltage between TP2 and GND to +1.57V (within ±10mV).

(2) Next, set LEVEL to 0V again and turn VR9 to adjust the voltage between TP2 and GND to 0V (within ±1mV).

6-3 Range Amplifier Block; Offset, Full Scale Adjustment

[Setting] MODE : -DC LEVEL: 0V OFFSET : OFF

(1) Turn on SG and turn VR8 to adjust the voltage between TP4 and GND to 0V (within ±1mV).

(2) Turn on SG and turn VR7 to adjust the voltage between TP4 and GND to 0V (within ±1mV).

(3) Next, set LEVEL to 4.98V and make sure that there is a voltage of 4.98V (±100mV) between TP4 and GND.

6-4 Offset Block; Offset, Full Scale Adjustment

[Setting] MODE : -DC LEVEL : 0V OFFSET : 0V

(1) Observing the voltage between TP4 and GND, turn VR3 to adjust it to 0V (±1mV).

(2) Next, with OFFSET ON and the level at +4.961V, observing the voltage between TP4 and GND, turn VR2 to adjust it to +4.96V (±10mV).

(3) With OFFSET ON and the level at 0V again, turn VR3 to adjust the voltage between TP4 and GND to 0V (within ±1mV).

(4) Repeat 4-2.

(5) Repeat 4-3.

(6) When not converging, repeat 4-2 and 4-3 several times.

6-5 Filter Block; "Q" Adjustment, "Wn" Check

[Setting] CHECK mode (Start up with the NEXT key and turn on CHECK with Version)

MODE : IMPULSE LEVEL : 4.98V

OFFSET : OFF FREE RANGE : 10kHz

AD3521 setting : FREQ RANGE : 100K X-LOG

Filter : ON SENSE : 20dB

(1) Input the impulse waveform of the SG card to the AD3521 and observe its frequency characteristic. Turn VR5 to adjust the ripples to within ±0.3dB.

(2) In the state of 5-1, make sure that the transmission zero point "Wn" is at about 4.5 times 10 K (Fc). Make sure that there is a dip point in the frequency characteristic at 10K x 4.5 = 45K. If the dip point is not at 4.5 times Fc, check for the RC constant around the filter.

6-6 High Harmonic Distortion Factor Check

[Setting] MODE : SIN LEVEL : 4.98V OFFSET : OFF

FREQ1 : 90kHz

Input the output waveform of the SG card to the AD3521 and observe a high harmonic distortion factor.
However, use the AD3521 in the TEST mode.
(To effect the TEST mode, start up the power source, pressing TRIGGER/WINDOW.)

The AD3521 should be set to +20dB, DC coupling, filter OFF, and window = HANNING.

It is O.K.if secondary distortion factor is -60dB.

4-1-8 Envelope Card Adjustment

1. Preparation

Devices and Tools Required

Sensor power unit

- Cable with a miniature plug at one end, and 1kΩ metal-film resistor at the other end
- Cable with a 3-pin 2 mm-pitch connector at one end, and ON/OFF switch at the other end
- Cable with a microdot connector at one end, and 1 k metal-film resistor at the other end
- Voltmeter with accuracy of 1/1,000
- Optional envelope block

Filter envelope

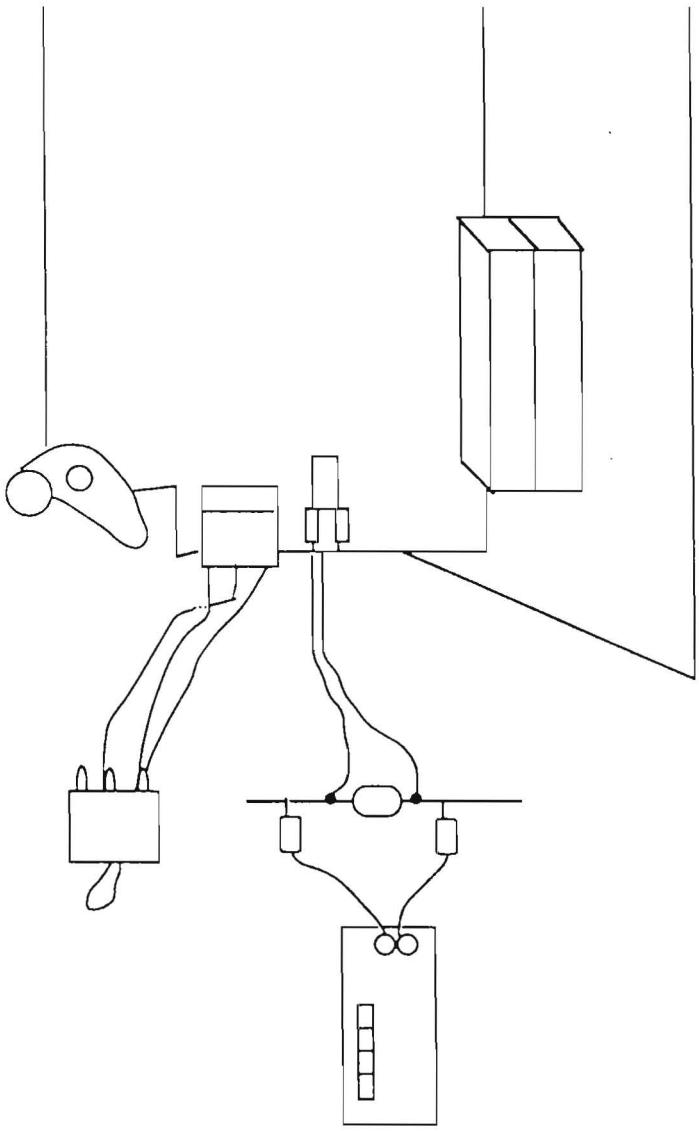
- SG
- FFT
- Oscilloscope
- Oscillator which is capable of modulating
- board (dependig on cases))
- Data setting jig (if available)

Adjustment Method

Sensor power unit (Fig. 1)

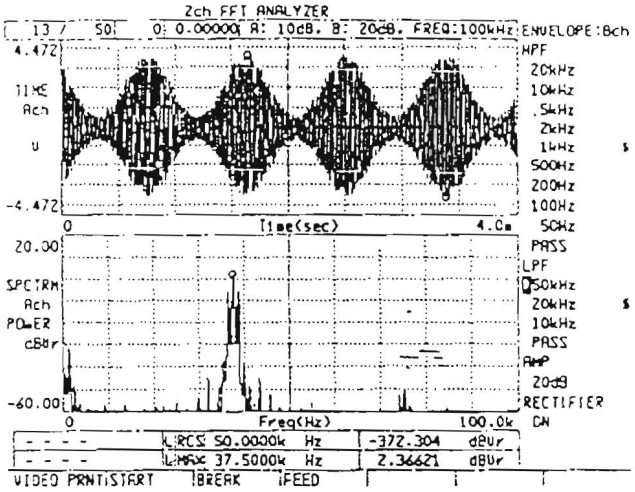
- Connect 2 kinds of cables to the option board to be adjusted, and insert it into the FFT via the power supply board or board and analog board.
- Connect the voltmeter to both ends of the resistor of the cable which has it.
- Set the range of the voltmeter, in which 500mV can be measured as accurately as 1/100.
- Turn off the switch of the cable which has it, turn VR5 to adjust the value of the voltmeter to 495-505mV.
- Next, Set the voltage range in which 2V can be measured as accurately as 1/100.
- Turn on the switch, and turn VR6 to adjust the value of the voltmeter to 1.98-2.02V.

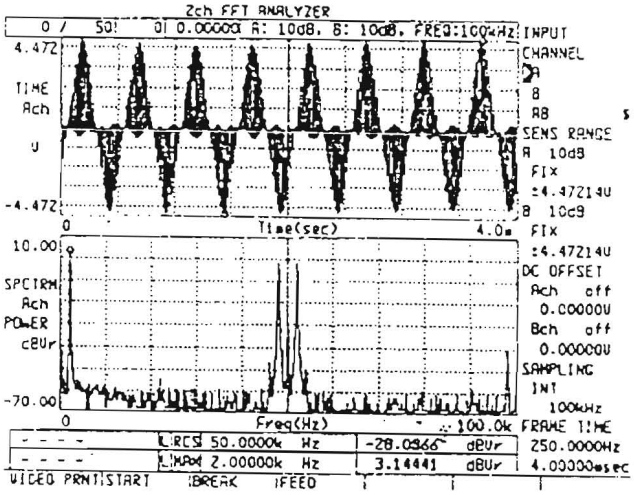
Fig. 1

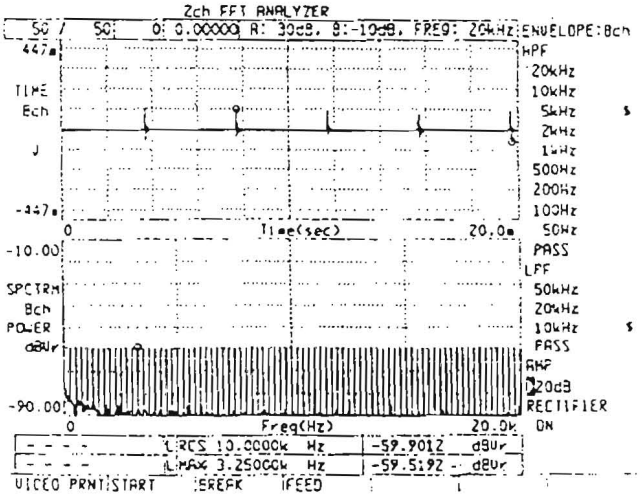


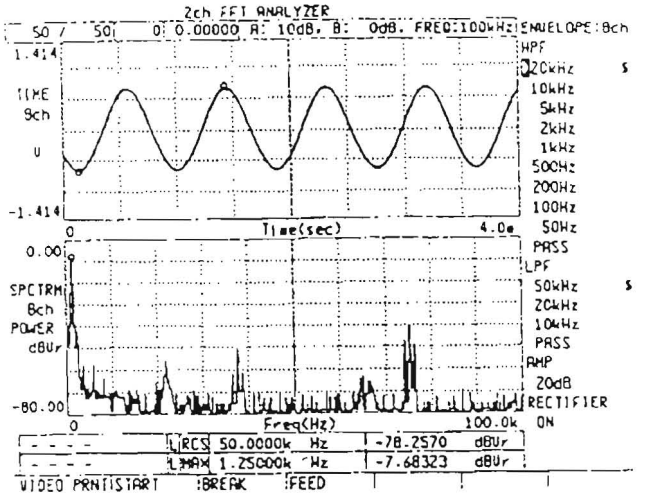
Envelope block (Fig. 2)

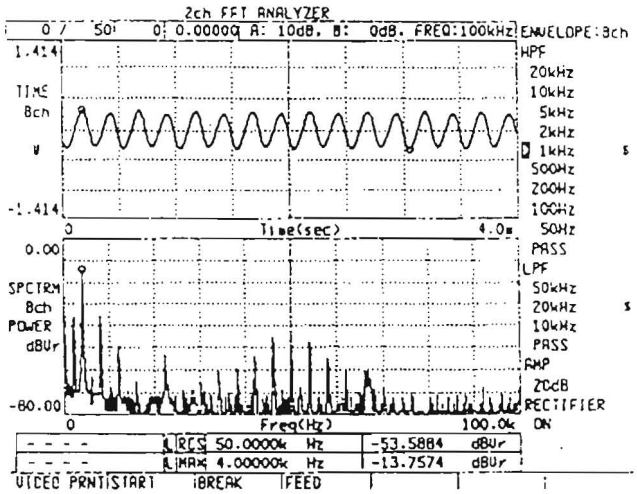
- Make sure that JP6 is connected.
- Connect to the FFT via the analog board and ? board, and turn on the power.
- Connect the SG to the connector which contains the FFT option. Set a sine wave or a triangular wave as an oscillation waveform. Any frequency range and voltage range will do.
- Connect the oscilloscope to TP6.
- Next, set the FFT option.
  - Press [MODE] of [CH INPUT] twice where the option is contained.
  - Press [ENV SET] to the right of the field which indicated the functions of the soft keys located at the bottom of the CRT.
  - The envelope setting items appear on the right side of the CRT. Set the items with [MENU], [▲], [▼], and [ENTER].
  - Set HPF to [2kHz], LPF to [PASS], AMP to [0dB], and RECTIFIER to [ON].
  - Press the soft key [ENV IN].
- When this is done, a full-wave rectified waveform appears on the FFT screen and oscilloscope screen. As the height of peaks differs alternately, turn VR1 to adjust all the peaks to the some height. (See Fig. 3)
- Adjust JP6.

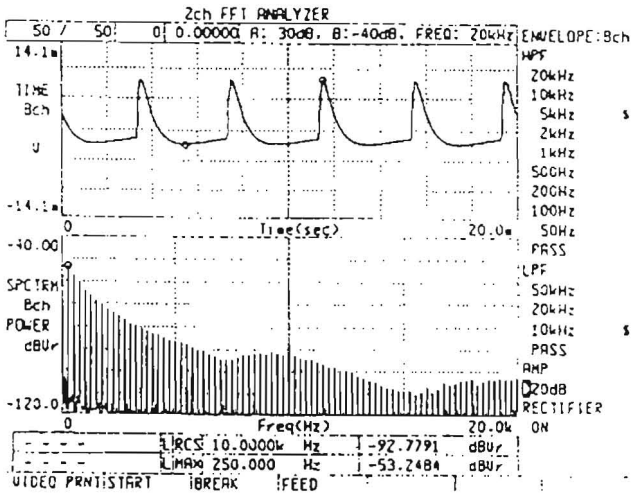

Zch FFT ANALYZER
ENVELOPE:Bch
TIME
Ach
Time(sec)
SPCTRM
Ach
POWER
Freq(Hz)
RECTIFIER
VIDEO PRNT!START
BREAK
FEED


Zch FFT ANALYZER
INPUT
CHANNEL
SENS RANGE
FIX
DC OFFSET
SAMPLING
FRAME TIME
TIME
Ach
Time(sec)
SPCTRM
Ach
POWER
Freq(Hz)
VIDEO PRNT!START
BREAK
FEED


Zch FFT ANALYZER
ENVELOPE:Bch
TIME
Bch
Time(sec)
SPCTRM
Bch
POWER
Freq(Hz)
RECTIFIER
VIDEO PRNT!START
BREAK
FEED


2ch FFT ANALYZER
50 / 50 0 0.00000 A: 10dB, B: 0dB, FREQ:100kHz
ENVELOPE:8ch
1.414
TIME
8ch
V
-1.414
0
Time(sec)
4.0m
0.00
SPCTRM
8ch
POWER
dBVr
-80.00
0
Freq(Hz)
100.0k
HPF
20kHz
10kHz
5kHz
2kHz
1kHz
500Hz
200Hz
100Hz
50Hz
PASS
LPF
50kHz
20kHz
10kHz
PASS
AMP
20dB
RECTIFIER
ON
RCS 50.0000k Hz -78.2570 dBVr
LMAX 1.25000k Hz -7.68323 dBVr
VIDEO PRNT!START !BREAK !FEED


2ch FFT ANALYZER
0 / 50 0 0.00000 A: 10dB, B: 0dB, FREQ:100kHz
ENVELOPE:8ch
1.414
TIME
8ch
V
-1.414
0
Time(sec)
4.0m
0.00
SPCTRM
8ch
POWER
dBVr
-80.00
0
Freq(Hz)
100.0k
HPF
20kHz
10kHz
5kHz
2kHz
1kHz
500Hz
200Hz
100Hz
50Hz
PASS
LPF
50kHz
20kHz
10kHz
PASS
AMP
20dB
RECTIFIER
ON
RCS 50.0000k Hz -53.5884 dBVr
LMAX 4.00000k Hz -13.7574 dBVr
VIDEO PRNT!START !BREAK !FEED


2ch FFT ANALYZER
50 / 50 0 0.00000 A: 30dB, B:-40dB, FREQ: 20kHz
ENVELOPE:8ch
14.1m
TIME
8ch
V
-14.1m
0
Time(sec)
20.0m
-40.00
SPCTRM
8ch
POWER
dBVr
-120.0
0
Freq(Hz)
20.0k
HPF
20kHz
10kHz
5kHz
2kHz
1kHz
500Hz
200Hz
100Hz
50Hz
PASS
LPF
50kHz
20kHz
10kHz
PASS
AMP
20dB
RECTIFIER
ON
RCS 10.0000k Hz -92.7791 dBVr
LMAX 250.000 Hz -53.2484 dBVr
VIDEO PRNT!START !BREAK !FEED

Amplifier block

- Connect to the FFT via the analog board and board, and turn on the power.
- Connect the SG to the connector which contains the FFT option, and connect CLOCK OUT of the FFT to CLOCK IN of the SG. Set the waveform to the multisine one.
- Set the FFT screen.
  - Press [EXTEND] of [MENU].
  - Press [WIND] to the left of the field which indicates the functions of the soft keys located at the bottom of the CRT.
  - The window setting items appear on the right side of the CRT. Set [HANNING] with [▲], [▼], and [ENTER] of [MENU].
  - Display the spectrum on the screen.
- Next, set the FFT option.
  - Press [MODE] of [CH INPUT] twice where the option is contained.
  - Press [ENV SET] to the right of the field which indicates the functions of the soft keys located at the bottom of the CRT.
  - The envelope setting items appear on the right side of the CRT. Set the items with [MENU], [▲], [▼], and [ENTER].
  - Set HPF to [500Hz], LPF to [PASS], AMP to [0dB], and RECTIFIER to [OFF].
  - Press the soft key [ENV IN].
- A picture of flat transfer function appears. Maine this flat surface contain a horizontal cursor.(Fig. 4)
- Press HPF Set HPF to [10kHz] in that state.
- Turn VR2 to adjust the then flat part of the transfer function to the horizontal cursor.
- Make the same adjustment with AMP set to [20dB] by turning VR3.

4-2-1 Inspection Procedures of FFT Main Body

Make this inspection under the following conditions:

- Room temperature of 25 ± 3°C
- Perform running for 2 hours or more after turning ON the power, and then, make measurement.

1. Appearance and Assembly Inspection

- Each screw should be tightened properly.
- The cover should not be opened when the optional floppy disk or printer is not attached. The cover should be opened when the option is attached.

2. Shock Test

- Lift the front part of the FFT, let it fall freely 2 to 3 times, there should be no problem found in the subsequent checks.

3. CRT Screen Check

- Turn ON the power, and screen distortion, offset, blur, and tilt sould be within allowable range.
- Turn the brilliance (INT) control knob on the rear panel to control the brilliance of the screen.

4. Option Status Check

- Press the [HELP] key on the right part of the screen, and soft keys "MEM CLR" and "OPTION". Option names are displayed on the upper right part of the screen. They must match optional specifications.

5. Analog Check

- Set the upper screen for Ach and the lower screen for Bch, select a dual range, and make the spectrum to display.

> [UPPER/LOWER] illuminated, [A/B]; UPPER = Ach
> [UPPER/LOWER] unilluminated, [A/B]; LOWER = Bch
> [DUAL/SING] illuminated, dual display
> Select the spectrum display with the [SPEC] key.

- Set both Ach and Bch to DC and GND.

> Ach INPUT section
> [MODE]
> "AC/DC" unilluminated, DC selected
> "GND" illuminated, GND selected]
> Bch INPUT section
> [MODE]
> "AC/DC" unilluminated, DC selected
> "GND" illuminated, GND selected

- Set WINDOW to RECT.

> MENU section
> [EXTEND]
> "WINDOW"
> Bring ">" to RECT at the upper right part of the screen with the cursor move key of the MENU section, and press the [ENTER] key.
> This displays "$" to the right of RECT.

- In the FREO section, set the maximum frequency range of the FFT.
- The DC spectrum at the left part of the spectrum screen should be -30dB/full scale for input of +10dB, 0dB and -20dB.

6. Noise Level

- Press the [EXTEND] key of the MENU section and the soft key "FFT" POINT. FFT PRECISION appears at the lower right part of the CRT. Set this to 32 bits.
- Set the input voltage and frequency ranges.

20kHz version

Frequency Range	Input Voltage Rangage	Inspection Criteria
100Hz, 1kHz 20kHz	-60dB	
	-20dB	

100kHz version

Frequency Range	Input Voltage Rangage	Inspection Criteria
100Hz, 1kHz 20kHz, 100kHz	-60dB	
	-20dB	

- DISPLAY section
  [AVE/INST] illuminated for both Ach and Bch
- AVE section
  [START/STOP] illuminated
- When the average at the upper left part of the screen becomes 20 or more, make sure that the noise level is within the inspection criteria.

  Note : AC components only
- DISPLAY section
  [AVE/INST] unilluminated for both Ach and Bch
- Change the setting of the input voltage and frequency ranges and repeat.

7. Frequency Characteristic

- Press the [MODE] key of the INPUT section and set GND = OFF with the soft key GND = OFF with the soft key "GND" unilluminated.
- Press the [EXTEND] of the MENU section.
  Pressing the soft key WIND displays "WIND" at the right part of the screen. Using the cursor move key of the MENU section, bring ">" to REC and press the ENTER key. "$" appears to the right of RECT.
- Set the frequency range as shows in Table 1, and inspect the frequency and voltage ranges shown in Table 1.

Table 1-1 20kHz Version

Frequency Range	Measurement Point
20KHz	3 point of 0dB range
10KHz	1/10 F, 9.8/10 F of 0dB
5KHz	Ditto
2KHz	Ditto
1KHz	Ditto
500Hz	Ditto
200Hz	Ditto
100Hz	Ditto
50Hz	Ditto
20Hz	Ditto

Table 1-2 100kHz Version

Frequency Range	Measurement Point
100KHz	Measure all of Table2
50KHz	3 points of 0dB range
20KHz	Ditto
10KHz	1/10 F, 9.8/10 F of 0dB
5KHz	Ditto
2KHz	Ditto
1KHz	Ditto
500Hz	Ditto
200Hz	Ditto
100Hz	Ditto

Table 2 Transmitter Signals and FFT Input Voltage Ranges Setting Table

Frequency / Voltage Range	+10dB	0dB	-10dB	-20dB	-30dB	-60dB
1/10 FRENG	+ 9dB	-1dB	-11dB	-21dB	-31dB	-61dB
5/10 FRENG	+ 9dB	-1dB	-11dB	-21dB	-31dB	-61dB
9.8/10 FRENG	+ 9dB	-1dB	-11dB	-21dB	-31dB	-61dB

- Input the signals shown in Table 2 from the sine wave transmitter to Ach and Bch, and read the maximum frequency and voltage values displayed at the lower part of the screen by the [UPPER/LOWER] key of the CURSOR section.
- Specifications
  Should be within ±0.3dB of input.
  High harmonic distortion should be -0.70dB/full scale or less.

8. Trigger Check

- TRIG section
  [MODE]
  [ARM/FREE] illuminated
  Set to either Ach or Bch the SOURCE at the upper right part of the screen to either Ach or Bch.
- FREQ section
  Set to the maximum frequency range of the FFT.
- INPUT section for Ach/Bch
  Set to 0dB.
- Change TRIG LEVEL and make sure that the trigger point at the center of the screen changes. Also, make sure that the waveform rises and falls by changing SLOP to ±.

  Note: Make sure of this for both Ach and Bch.

9. External Trigger Check

- Same setting as in Paragraph 8 above
- Press the soft key "SOUR EXT".
- Input to TRIG IN of the rear panel the same signal as the input to the front panel.
- Same as in Paragraph 8, change TRIG LEVEL and SLOP, and make sure that the input screen changes as the setting does.

10. GP-IB Check

- Connect the computer and FFT to the GP-IB.
- Prepare the program which operates the FFT from the computer through the GP-IB.
- Press the HELP key on the panel, and then, the soft key INITIAL to initialize.
- MENU section
  [EXTEND]
  Soft key "GP-IB"
  "GP-IB" appears at the upper right part of the screen. Make sure of "FFT MODE DEVICE $".
- Running computer software causes the computer to make setting on the FFT panel through the GP-IB. Make sure that the FFT can be set from the computer.

11. Prior to Completion of Inspection

- Before completing the inspection, press the [HELP] key, and then, soft key "INITIAL" to initialize.

4-2-2 Inspection of SG Card

Table of Contents

1. DC Amplitude Probability, Offset

1-1 DC Amplitude Probability

Set the mode of the SG card to +DC/-DC and check for DC amplitude probability, changing the level.

Measure the SG output voltage with the voltmeter and check to see whether it is within an allowable range. The specifications at ±DC output time are as follows.
(First, set the level, and then, +DC and -DC modes alternately.)

SG Setting OFF LEVEL	Allowable Range	* Turn OFFSET of SG to
±4.98V	±4.98V±50mV	(±4.93V~5.03V)
±1.495V	±1.495V±15mV	(±1.480V~1.510V)
±994mV	±994mV±10mV	(±984mV~1.00V)
±500mV	±500mV±10mV	(±490mV~510mV)
±149mV	±149mV±5mV	(±144mV~154mV)
±50mV	±50mV±3mV	(±47mV~53mV)
±9.94mV	±9.94mV±1mV	(±8.94mV~10.94mV)
0V	Within ±1mV	
At SG-OFF time	Within ±1mV	

Note: The level can be set more easily by key input. If you enter 5, 1.5, 1, 0.15, 50, and 10 m, the level is automatically corrected to the above values and set to them.

1-2 Offset Function Check

An offset voltage of up to ±5V can be applied to the SG output waveform. Check that output voltage.

[SG Setting] MODE : +DC LEVEL : 0V
OFFSET : ON

Offset Setting Voltage	SG Output Voltage Allowable Range	
+4.96V	+4.96V	±20mV
+2.5V	+2.5V	±10mV
+39.1mV	+39.1mV	±2.4mV
0V	0V	±2.4mV
-2.5V	-2.5V	±10mV
-5.00V	-5.0V	±20mV

2. Frequency characteristic Check

Input SG output to the analog board of the main body and check the frequency characteristic within the band in each frequency range.

[SG Setting] MODE : MULTI SIN LEVEL : 4.98V
FREQ1 : 250Hz FREQ2 : 100K
(START) (STOP)

[Main Body Setting]
Coupling : AC coupling Window : RECT
Sense range : +20dB Frequency range : 100kHz

Make the time waveform appear on the upper screen, and the spectrum waveform appear on the lower screen, respectively, and enlarge the Y-scale of the lower screen to such an extent that it does not overflow from the screen. Then, average and observe the spectrum of the lower screen. (20 times) (-22dB to -24dB, 0.2dB/div).
For the 100kHz range or below as well, change the frequency range and make sure that the frequency characteristic is within 0 ±0.5dB. (6 points from 100kHz to 2kHz ranges)

Note: The analog board must have been adjusted.

3. High Harmonic Distortion and Noise Measurement

Input SG output to the analog board of the main body and check for high harmonic distortion and noise.

[SG Setting] MODE : SIN LEVEL : 994mV
FREQ : 10 k

[Main Body Setting]

Coupling	: DC coupling	Window	: RECT
Sense range	: 0dB	Frequency range	: 100kHz
Filter	: ON		

Make the time waveform appear on the upper screen and the spectrum waveform appear on the lower screen, respectively.

Average the spectrum of the lower screen (20 times), and make sure that the peak values of high harmonic distortion and noise components do not exceed a range of -60dB from the peak value of the basic wave.

In the figure below, the horizontal cursor is located at -63.9dB. Viewing from the peak of the waveform, this line is line for; 63.9 - 2.8 = 61.1dB

The filter of the analog board of the main body has been turned on.

Next, set SG to +DC (same level as 994mV), and make sure that the spectrum of non-DC noise components does not exceed a range of -75dB from the peak (DC).(50 times) Refer to the next page.

SIGNAL GENERATOR CHECK SHEET

ITEM	SET-TING	ALLOW-ANCE	RE-SULT	ITEM	SET-TING	ALLOW-ANC	RE-SULT
Amplitu-deproba-bility	±4.98V	±4.98V \ ±5.03V		In-band frequency character-istic	MULTISIN 5V	±0.5dB	
	±1.495V	±1.480V \ ±1.510			100K RNG		
	±994mV	±984mV \ ±1004mV			50K RNG		
	500mV	±490mV \ ±510mV			20K RNG		
	149mV	±144mV \ ±154mV			10K RNG		
	50mV	±47mV \ ±53mV			5K RNG		
	9.94mV	±8.94mV \ ±10.94mV			2K RNG		
	0V	±1mV		High harmonic distortion	SIN 30K 1V	-60dB	
	SG-OFF	±1mV		Noise	+DC 5V	-75dB	
OFFSET	+4.961V	±10mV					
	+2.5V	±5mV					
	+39.1mV	±1mV					
	0V	±1mV					
	-2.5V	±5mV					
	-5.0V	±10mV					

4-2-3 Envelope Card Inspection

1. Check

Check Itemst

Sensor power source block

- Supply power (0.5 mA and 2 mA)
- Sensor supply power noise

Filter block

- Cut-off frequency (LPF, HPF)
- Attenuation factor (LPF, HPF)

Envelope block

- basic functioning

Check Methods

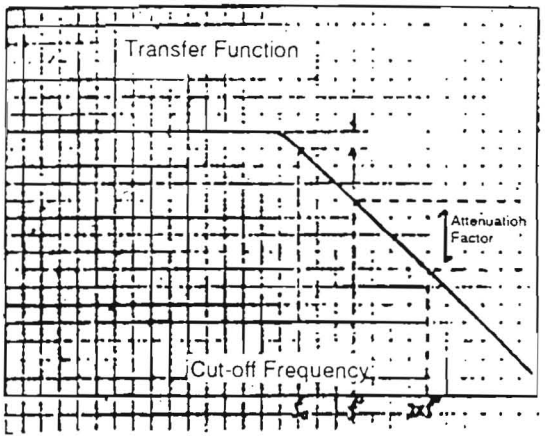
Sensor power (Fig. 5 Connection Diagram)

- Build the sensor power board in the FFT main Body.
  - Connect the connector, which has microdot at one end and a resistor at the other end, to the sensor connector on the rear panel of the FFT main body.
  - Connect the voltmeter to the resistor. Using the rear power selector switch, make sure that the value of the voltmeter is within 495-505mV and 1.98-2.02V, respectively.
- Sensor supply power noise
  - When sensor input is turned OFF by the soft switch, make sure that there is no noise around 100kHz or less.
  - When sensor input is turned ON by the soft switch, make sure that there is no noise around 100kHz or less.

Filter block

- Cut-off frequency (Fig. 6)
  - Connect the SG to the connector which contains the FFT option, and connect CLOCK OUT of the FFT to LOCK IN of the SG. The wave form should be set to MULTI SIN.
  - Set the FFT screen.
    - Press [EXTEND] of [MENU].
    - Press [WIND] to the left of the field which indicates the functions of the soft keys located at the bottom of the CRT.
    - Window setting items appear at the right part of the CRT. Set [HANNING] with [▲], [▼], and [ENTER] of [MENU].
    - Make the spectun appear on the screen.
  - Next, set the FFT option.
    - Press [MODE] of [CH INPUT] where the option is.
    - Press [ENV SET] to the right of the field which indicates the functions of the soft keys located at the bottom of the CRT.
    - Envelope setting items appear at the right part of the CRT. Set the items with [MENU], [▲], [▼], and [ENTER].
    - Press the soft key [ENV IN].
    - Set AMP to [0dB], and RECTIFIER to [OFF].
  - The cut-off frequency should be checked for HPF (20kHz to 50Hz) and LPF (50kHz to 10kHz) individually. That is, when viewing HPF, set LPF to PASS, and vice versa.
  - When this is done, a picture of transfer function appears on the screen. The cut-off frequency is 3dB below the flat part of this picture.
  - Make sure that the then value is within 20% of a a set value.

- Attenuation factor
  - In the linear part of the attenuation area of the picture obtained in checking the "cut-off frequency", select an arbitrary point, and make sure that there is an attenuation amount of 22dB or more between that point and another point where the frequency becomes double that point.

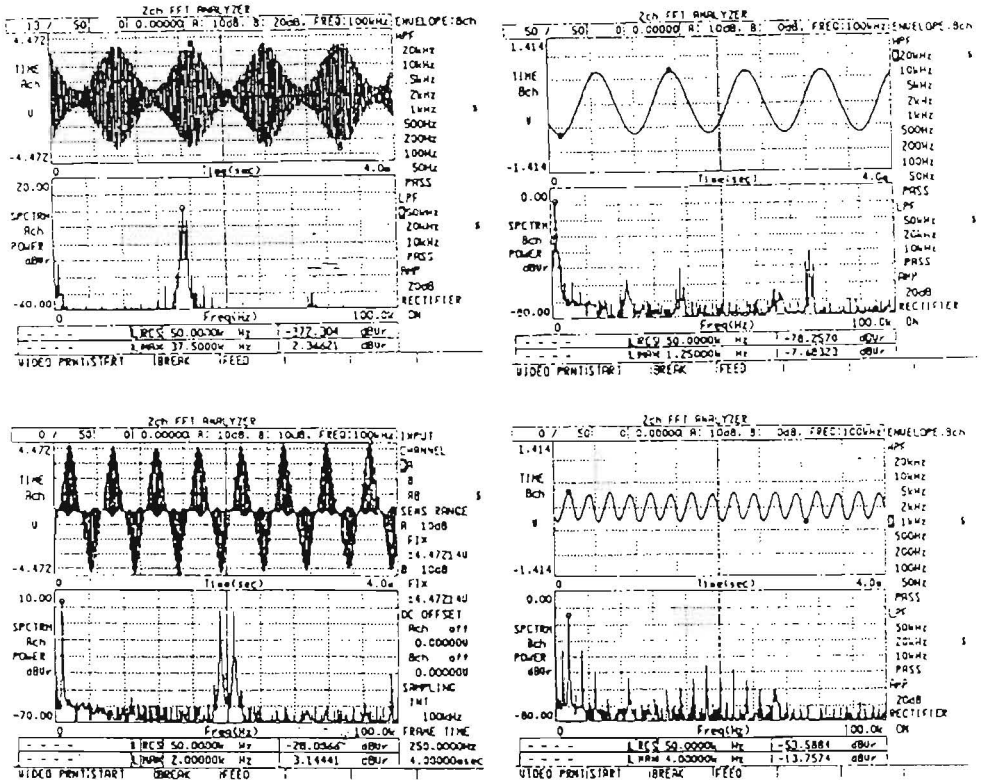


Amplifier block

- The setting of the FFT may be the same as so far.
- Set the FFT option. Set AMP to [0dB], and RECTIFIER to [OFF].
- Make sure that respective gain variations of LPF and HPF are within 1dB.

Envelope block (Fig. 7)

- Check for basic functioning.
- The FFT has been properly set, if the time waveform can be seen.
- Set the FFT option. Set AMP to [20dB], and RECTIFIER to [ON]. Set arbitrary values for HPF and LPF.
- When AM waves (both sine waves) are entered, make sure that a modulated wave is outputted.
- When a modulated wave is entered, which was obtained by the carrier wave of the sine wave and the modulated wave of the square wave, make sure that an output waveform is also changed by altering HPF setting.



2. Check List

Sensor	Sensor Supply Current		100 KHz Noise
	0.5 mA	2 mA	
	OK.NG	OK.NG	OK.NG

Filter	Frequency Range	Cut-off Frequency	Attenuation Factor
	HPF.20kHz	OK.NG	OK.NG
	10kHz	OK.NG	OK.NG
	5kHz	OK.NG	OK.NG
	2kHz	OK.NG	OK.NG
	1kHz	OK.NG	OK.NG
	500Hz	OK.NG	OK.NG
	200Hz	OK.NG	OK.NG
	100Hz	OK.NG	OK.NG
	50Hz	OK.NG	OK.NG
	LPF.50kHz	OK.NG	OK.NG
	.20kHz	OK.NG	OK.NG
	.10kHz	OK.NG	OK.NG

Gain	Envelope
OK.NG	OK.NG

4-2-4 Comparator Card Inspection

1. Inspection

Devices and Tools Required

- FFT main body
- Tester (Optimum if it allows you to vies the output of all 64 channels. Check with the LED, etc. for output continuity)

Check Method

- Insert the board into a specified position and make sure that the status can be read. Press the [HELP] key on the panel, and then, soft keys [EMC CLS] and [OPTION] in that order.
- Set all the comparator to N.G., and make sure that the relay output of the comparator board is of high impedance.
- Next, set all the comparator to O.K., and make sure that the relay output of the comparators has continuity.

4-2-5 Microphone Filter Inspection

1. Inspection

Filter block (When there is no capacitor microphone power source nearby)

- First, connect the power source; +15-+28V to No.3 of J2, and GND to No.4 of J2.
- Connect the AD8621 to the input side of this instrument, and the FFT to the output side. When this is done, set the AD8621 to MULTI SIN and connect CLOCK to CLOCK OUT of the FFT for synchronous operation. At this time, see to it that the FFT displays the spectrum and set WINDOW to RECT.
- Make sure that the cut-off frequency of the frequency characteristic displayed on the screen is 10 Hz, and the attenuation factor is 24dB or more.

Power source block (when shipped together with the filter)

- Connect a tester to the pins A and E of the microphone connector located on the rear panel of the FFT, and make sure that a voltage of 28V is being outputted.

Filter block (when the capacitor microphone power source is at hand)

- Connect the AMZ33 to the microphone terminal located on the rear panel of the FFT.
- Connect the AD8621 to the No.4 signal pin and No.3 earthing pin of the connector in the filter block by any means. When this is done, set the AD8621 to MULTI SIN,and connect CLOCK to CLOCK OUT of the FFT for synchronous operation. At this time, see to it that the FFT displays the spectrum and sets WINDOW to RECT.
- Make sure that the cut-off frequency of the frequency characteristic displayed on the screen is 10kHz, and the attenuation factor is 24dB or more.

Technical Information list

Parts List

Main Board	PZ:2055
Key SW Board	PZ:2056,PZ:2057
CRTC Board	PZ:2058
ROM Board	PZ:2059
A/D Board	PZ:2066A
A/D Board	PZ:2066B
AC P.S Board	PZ:2067
AC P.S Board	PZ:2068
Exploded View-1	
Exploded View-2	
Exploded View-3	

Electrical circuit List

Main Board	PZ:2055
Panel/Soft Key Board	PZ:2056,PZ:2057
CRTC Board	PZ:2058
ROM Board	PZ:2059
Analog Board	PZ:2066A/B,PZ:2059
P.S board	PZ:2067,PZ:2068

Assembly List

Main Board	PZ:2055
Panel Key Board (P Key Board)	PZ:2056
S Key Board (S Key Board)	PZ:2057
CRTC Board	PZ:2058
ROM Board	PZ:2059
Analog Board	PZ:2066A/B
P.S Board IN	PZ:2067
P.S Board OUT	PZ:2068
Exploded View-1	
Exploded View-2	
Exploded View-3	

PARTS LIST

AD-3524/25 MAIN BOARD 1/5

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2055	MAIN BOARD AD3524/25	1
C6,9,12,29~36,38 C40,42~46,48~50 C52~60,62~70 C72~73,88	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	41
C27,79	CC:0.001U	CERAMIC CAPACITOR 0.001μF	2
	CC:0.0022U	CERAMIC CAPACITOR 0.0022μF	1
C2,3,4	CC:0.01U	CERAMIC CAPACITOR 0.01μF	3
C28,71	CC:0.022U	CERAMIC CAPACITOR 0.022μF	2
C13	CC:10P	CERAMIC CAPACITOR 10PF	1
C15,16	CC:33P	CERAMIC CAPACITOR 33PF	2
C80	CC:330P	CERAMIC CAPACITOR 330PF	1
C86,87	CM:E6104KF	FILM CAPACITOR 0.1μF 630V	2
C5,10,11,14,17,18 C22,26,37,39,41 C81,81~84	CT:1A4R7	TANTALM CAPACITOR 4.7μF 10V	16
	CT:1C100	TANTALM CAPACITOR 10μF 16V	2
C74	CT:1C220	TANTALM CAPACITOR 22μF 16V	1
C8,20,21,23~25	CT:1D2R2	TANTALM CAPACITOR 2.2μF 20V	5
	CT:1VR33	TANTALM CAPACITOR 0.33μF 35V	5
D4	DI:EK04	SCHOTTKY DIODE	1
D1~3,6~16,19,20	DI:1SI588	DIODE	16
D5,17,18	DZ:05Z5.6	ZENER DIODE 5.6V	3
BT1	EB:N-50SB3		1
BZ1	ET:20Z-32C-5V-N		1
J20	JA:4470-01-1111		1
J22	JA:57LE-20240		1
	JI:700A2	CONNECTOR	4
J13	JI:704J026-AU/0	CONNECTOR	1
J11	JI:704J040-AU/0	CONNECTOR	1
J14	JI:704J050-AU/0	CONNECTOR	1
J10,12	JI:704Q050-AU/M	CONNECTOR	2
J16~19	JJ:TMP-J01X-V6		4
	JS:XR3G-6401	IC SOCKET	2
J15	JT:1-172429-2		1

PARTS LIST

AD—3524/25 MAIN BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2055	MAIN BOARD AD3524/25	1
J1～9	JT:166621-8		9
	K0:523A-008		1
	K0:523A-025		3
	PC:2055C	PRINT BOARD	1
	PC:2251A	PRINT BOARD	1
U1	UC:HC08F	CMOS IC	1
U2	UC:HC74F	CMOS IC	1
Q1.2	QT:C1815Y	TRANSISTOR	2
R1,9,15	RC:NAT1.2K	CARBON RESISTOR 1.2KΩ 1/4W	3
R45,54	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	2
U23.43,44,58	RC:NAT10K	CARBON RESISTOR 10KΩ 1/4W	4
R50.53,62	RC:NAT100K	CARBON RESISTOR 100KΩ 1/4W	3
R6～8,51	RC:NAT100R	CARBON RESISTOR 100Ω 1/4W	4
R64,65	RC:NAT12R	CARBON RESISTOR 12Ω 1/4W	2
R60	RC:NAT150R	CARBON RESISTOR 150Ω 1/4W	1
R59,60	RC:NAT180K	CARBON RESISTOR 180KΩ 1/4W	2
R48	RC:NAT2.2K	CARBON RESISTOR 2.2KΩ 1/4W	1
R52	RC:NAT22K	CARBON RESISTOR 22KΩ 1/4W	1
R74	RC:NAT22R	CARBON RESISTOR 22Ω 1/4W	1
R63	RC:NAT220K	CARBON RESISTOR 220KΩ 1/4W	1
R3.5,13,24.66	RC:NAT220R	CARBON RESISTOR 220Ω 1/4W	5
R11,14	RC:NAT270R	CARBON RESISTOR 270Ω 1/4W	2
R19,34,35	RC:NAT330R	CARBON RESISTOR 330Ω 1/4W	3
R2,4,36,75,76	RC:NAT4.7K	CARBON RESISTOR 4.7KΩ 1/4W	5
R20,25,30～33 R38～42,67	RC:NAT47R	CARBON RESISTOR 47Ω 1/4W	12
R16,22,27,37,49 R68,73	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	7
R70,72	RC:NAT5.6K	CARBON RESISTOR 5.6KΩ 1/4W	2
R71	RC:NAT56R	CARBON RESISTOR 56Ω 1/4W	1
R18	RC:NAT560R	CARBON RESISTOR 560Ω 1/4W	1
R10,26	RC:NAT680R	CARBON RESISTOR 680Ω 1/4W	2
R17	RC:NAT75R	CARBON RESISTOR 75Ω 1/4W	1
R12	RC:NAT82R	CARBON RESISTOR 82Ω 1/4W	1

PARTS LIST

AD—3524/25 MAIN BOARD 3/5

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2055	MAIN BOARD AD3524/25	1
R28	RM:RNM1.5KF	METALIZED RESISTOR 1.5KΩ 1/4W	1
	RM:RNM1KF	METALIZED RESISTOR 1KΩ 1/4W	1
R55,61	RM:RNM2.40KF	METALIZED RESISTOR 2.40KΩ 1/4W	2
	RM:RNM220KF	METALIZED RESISTOR 220KΩ 1/4W	1
R47	RM:RNM4.53KF	METALIZED RESISTOR 4.53KΩ 1/4W	1
R57	RM:RNM5.36KF	METALIZED RESISTOR 5.36KΩ 1/4W	1
R56	RM:RNM5.9KF	METALIZED RESISTOR 5.9KΩ 1/4W	1
R46	RM:RNM523KF	METALIZED RESISTOR 523KΩ 1/4W	1
R29	RM:RNM909RF	METALIZED RESISTOR 909Ω 1/4W	1
RA3	RN:IHR-4-471MA	RESISTOR NETWORK 470Ω	1
RA5,18,20	RN:IHR-4-472MA	RESISTOR NETWORK 4.7KΩ	3
RA4,8~17,19	RN:IHR-8-103MA	RESISTOR NETWORK 10KΩ	12
RA6,7	RN:IHR-8-223MA	RESISTOR NETWORK 22KΩ	2
VR3	RV:H102	POTENTIOMETER 1KΩ	1
VR2	RV:H501	POTENTIOMETOR 500Ω	1
VR1	RV:RK09111		1
RL1,2,3	SL:KCR-105	RELAY	3
	SS:2NB2X2AG		1
TP1~47,51~54	TM:LC-2-G-0	TEST PIN	52
U58	UA:C311C	OP AMP	1
U10	UA:MB3771	VOLTAGE COMPARATOR	1
U59	UA:TL072CP	OP AMP	1
U97	UC:AC00SJ	CMOS IC	1
U7,8,62,83,91	UC:AC04PC	CMOS IC	5
U20,25	UC:AC08PC	CMOS IC	2
U22	UC:AC10PC	CMOS IC	1
U75,78	UC:AC138PC	CMOS IC	2
U3	UC:AC14PC	CMOS IC	1
U77	UC:AC240SJ	CMOS IC	1
U29,34,37,40,47 U51,70,74	UC:AC244SJ	CMOS IC	8
U31,35,57,60	UC:AC245SJ	CMOS IC	4
U43,50,54,92	UC:AC32PC	CMOS IC	4
U32,36	UC:AC373SJ	CMOS IC	2

PARTS LIST

AD-3524/25 MAIN BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2055	MAIN BOARD AD3524/25	1
U33	UC:D65006GF-232	CMOS IC	1
U61	UC:D65031GF-218	CMOS IC	1
U71,72	UC:D71054G	CMOS IC	2
U79,80	UC:D71055G	CMOS IC	2
U98	UC:HC00F	CMOS IC	1
U99	UC:HC03F	CMOS IC	1
U15,17	UC:HC04	CMOS IC	2
U93	UC:HC08F	CMOS IC	1
U65	UC:HC138	CMOS IC	1
U16	UC:HC148	CMOS IC	1
U95	UC:HC153F	CMOS IC	1
U24	UC:HC157	CMOS IC	1
U26	UC:HC174	CMOS IC	1
U13	UC:HC32	CMOS IC	1
U63	UC:HC393	CMOS IC	1
U85,86,87	UC:HC4052	CMOS IC	3
U73,81	UC:HC4538	CMOS IC	2
U64,67,84	UC:HC595	CMOS IC	3
U6,96	UC:HC74	CMOS IC	2
U82	UC:RP93C46	CMOS IC	1
U44,45	UC:43257GU-10L	CMOS IC	2
U46	UC:62421A	CMOS IC	1
	UC:68HC000PS10	CPU	1
U38,39,41,42,48 U49,52,53	UC:81C4256-12PZ	CMOS IC	8
U68	UC:82C79F	CMOS IC	1
U66	UF:BA9221	D/A CONVERTER	1
U5	UN:7210C		1
U88	UR:TA78L005AP	SWITCHING REGULATOR	1
U89	UR:TA79L005P	SWITCHING REGULATOR	1
U94	UT:F00		1
U11	UT:F163		1
U4,9,14,16,21	UT:F38PC		5
U12,76	UT:LS38		2

PARTS LIST

AD—3524/25 MAIN BOARD 5/5

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2055	MAIN BOARD AD3524/25	1
U30	UT:1431AP-G		1
U1	UT:75160		1
U2	UT:75162		1
U90	XT:1336B	CRYSTAL	1
XT1	XT:240C-6R		1
	02:A48900A		1
	05:A40331		1

PARTS LIST

AD－3524／25 KEY SW BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2056	PANEL KEY SW BOARD AD3524/25	1
C2～5	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	4
C1	CT:1A4R7	TANTALM CAPCITOR 4.7μF 10V	1
D19,22,24	DL:PG4652KY	LED	3
D12～14,18,21,23	DL:PR4652K	LED	6
J1	JI:704P050-AU/M	CONNECTOR	1
J2	JT:1-172429-2		1
J3	JT:172429-8		1
	PC:2056A	PRINT BOARD	1
Q1～4	QT:A1020Y	TRANSISTOR	4
R8～10,19	RC:NAT330R	CARBON RESISTOR 330Ω 1/4W	4
R11～18	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	8
R1～7	RC:NAT56R	CARBON RESISTOR 56Ω 1/4W	8
S5,6,8～17,20～21 S24～26,28～30 S32～37,39,41～46 S48～52.54～56	SK:TR1-01	SWITCH	41
S1～4.7,18,19,22 S23,27,31,38,40 S47,53	SK:TR2-01-L2	SWITCH	15
U1	UA:TD62503BP	TRANSISTOR ARRAY	1

PARTS LIST

AD—3524/25 KEY SW BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2057	SOFT KEY SW BOARD AD3524/25	1
	K0:440-12S30		1
	K0:440-8S30		1
	PC:2057	PRINT BOARD	1
S1~8	SK:TR2-01-L2	SWITCH	8

PARTS LIST

AD－3524／25 CRTC BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2058	CRTC BOARD AD3524/25	1
C3～14	CC:0.022U-C	CERAMIC CAPACITOR 0.022μF	12
C1.2,15～17	CT:1C2R2-C	TANTALUM CAPACITOR 2.2μF	5
J1	JI:724P040-AU/W	CONNECTOR	1
J2	JI:724P050-AU/W	CONNECTOR	1
	PC:2058B	PC BOARD	1
R4～6	RC:1/10W101J	CARBON RESISTOR 100Ω 1/10W	5
	RC:1/10W153J	CARBON RESISTOR 15KΩ 1/10W	3
RN3,4	RP:RR152	RESISTOR NETWORK	2
RN1,2	RP:RR153	RESISTOR NETWORK	2
	TM:LC-2-G-0	TEST PIN	6
U20,21	UC:AC157SJ	CMOS IC	2
U16～18	UC:AC373SJ	CMOS IC	3
U22	UC:D65013GF-318	CMOS IC	1
U19	UC:HC04F	CMOS IC	1
U3～6	UC:HC245F	CMOS IC	4
U9	UC:S3484CP6	CMOS IC	1
U7,8,10～15	UN:81464-12P5		8
U2	UT:F163SJ	TTL	1
U1	XT:13358		1

PARTS LIST

AD—3524/25 ROM BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2059	ROM BOARD AD3524/25	1
C6～26	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	21
C1～5	CT:1A4R7	TANTALUM CAPACITOR 4.7μF 10V	5
	ET:CRP04		2
J1	JI:96P-2.54DS	CONNECTOR	1
J1～16	JS:10332-01-445	SOCKET	16
	PC:2059	PRINT BOARD	1
R1	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	1
R4～21	RC:NAT82R	CARBON RESISTOR 82Ω 1/4W	18
R2,3	RN:1HR-8-103MA	RESISTOR NETWORK	2
U18	UC:AC04PC	CMOS IC	1
U21	UC:AC138PC	CMOS IC	1
U20,22,23	UC:AC244PC	CMOS IC	3
U17,18	UC:AC245PC	CMOS IC	2
	UC:27C1001D-15	ROM	16

PARTS LIST

AD—3524 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2066A	A/D BOARD 20K AD3524	1
U14	MF:AMZ26	HYBRID IC	1
U13	MF:AMZ28	HYBRID IC	1
C5,6,7,34,35 C45～49,55,56 C94～97	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	16
C69～76	CC:F1H104K	CERAMIC CAPACITOR	8
C3	CC:0.001U	CERAMIC CAPACITOR 0.001μF	1
	CC:0.0033U	CERAMIC CAPACITOR 0.0033μF	1
C59,60,89	CC:10P	CERAMIC CAPACITOR 10PF	3
C31	CC:100P	CERAMIC CAPACITOR 100PF	1
C91	CC:150P	CERAMIC CAPACITOR 150PF	1
C90	CC:22P	CERAMIC CAPACITOR 22PF	1
C2	CD:10C010D5		1
C36,37,51～54,57	CK:KMA16VB100	ERECTROLYTIC CAPACITOR 100μF 16V	7
C8～11,24～28	CK:SRA10VB220MS	ERECTROLYTIC CAPACITOR 220μF 10V	10
C1	CM:E2334KS	FILM CAPACITOR	1
C4	CM:P1103JZ		1
C22	CM:V1H684JZ2		1
C12,13,16～21 C32,33,38～40 C65,66,77～80 C85～87	CT:1C220	TANTALUM CAPACITOR 22μF 16V	22
	CT:1D100	TANTALUM CAPACITOR 10μF 20V	3
C14,29,30,41～44 C63,64,67,68	CT:1E1R5-C	TANTALUM CAPACITOR	11
C50,58,81～84 C88,92,93,99	CT:1VR33	TANTALUM CAPACITOR 0.33μF 35V	10
VC2	CV:TZ03Z100YR		1
VC1	CV:TZ03Z2R3YR		1
PH6	DF:TLP521-3		1
PH1～5	DF:6N137		5
D4,5,7,8,16,17	DI:1SS53	DIODE	6
D9,10	DI:1SS97	SCHOTTKY DIODE	2
D13	DI:1S1588	DIODE	1

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PARTS LIST

AD—3524 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2066A	A/D BOARD 20K AD3524	1
	DZ:RD5.6FB		2
D3,6	DZ:05Z5.6	ZENER DIODE 5.6V	2
D11,12	DZ:05Z8.2	ZENER DIODE 8.2V	2
	ET:CRP04	BUZZER	1
J3	JA:XC5F-3222		1
J2	JI:96P-2.54DS	CONNECTOR	1
J1	JJ:TMP-J01X-A2		1
	JS:14120-01		2
L2～6,13	LL:LF1-220K	INDUCTOR	6
L7～9	LL:LF1-560K	INDUCTOR	3
	NF:FB-43-101		4
L10,11	NF:ZBF253S-01		2
	PC:2066C	PRINT BOARD	1
Q1	QF:A70A-SI	FET	1
Q23,24	QT:A965	TRANSISTOR	2
Q2,3,16～20	QT:C1815Y	TRANSISTOR	7
Q21,22	QT:C2235	TRANSISTOR	2
Q5,7,9,11,13,15	QT:FB1L3N-L	TRANSISTOR	6
Q4,6,8,10,12,14	QT:FP1L3N-L	TRANSISTOR	6
R5,37	RC:NAT1.2K	CARBON RESISTOR 1.2KΩ 1/4W	2
R45,55～60,64～67 R70,78～80	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	15
R2,21	RC:NAT1M	CARBON RESISTOR 1MΩ 1/4W	2
R63	RC:NAT1R	CARBON RESISTOR 1Ω 1/4W	1
R41～44	RC:NAT10K	CARBON RESISTOR 10KΩ 1/4W	4
R81	RC:NAT100K	CARBON RESISTOR 100KΩ 1/4W	1
R9,10,12	RC:NAT2.7K	CARBON RESISTOR 2.7KΩ 1/4W	3
R1,7,11,13,14,18 R19,34,35,38,39 R71,72,85～96	RC:NAT27R	CARBON RESISTOR 27Ω 1/4W	25
R84	RC:NAT270R	CARBON RESISTOR 270Ω 1/4W	1
R76,77	RC:NAT3.3K	CARBON RESISTOR 3.3KΩ 1/4W	2
R75,99～101	RC:NAT33K	CARBON RESISTOR 33KΩ 1/4W	4
R15,20	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	2

PARTS LIST

AD—3524 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2066A	A/D BOARD 20K AD3524	1
R24～26	RC:NAT560R	CARBON RESISTOR 560Ω 1/4W	3
R82	RC:NAT82R	CARBON RESISTOR 82Ω 1/4W	1
R6	RE:FMR2B472K		1
R3	RF:RR129	CARBON RESISTOR NETWORK	1
R16,17	RF:RR130A	CARBON RESISTOR NETWORK	2
R8	RF:RR142	CARBON RESISTOR NETWORK	1
	RF:91RRF	CARBON RESISTOR NETWORK	2
R23	RM:RNM1.24KF	METALIZED RESISTOR 1.24KΩ	1
R31,32	RM:RNM1.74KF	METALIZED RESISTOR 1.74KΩ	2
R22,27	RM:RNM1KF	METALIZED RESISTOR 1KΩ	2
R61,62,73,74	RM:RNM10KF	METALIZED RESISTOR 10KΩ	4
R28	RM:RNM2.74KF	METALIZED RESISTOR 2.74KΩ	1
R30,33	RM:RNM20.5KF	METALIZED RESISTOR 20.5KΩ	2
R97,98	RM:RNM3.9KF	METALIZED RESISTOR 3.9KΩ	2
R36,46～54	RM:RNM470RF	METALIZED RESISTOR 470Ω	10
R40	RN:IHR-4-153MA	RESISTOR NETWORK	1
VR2	RV:TM7S-500R	POTENTIOMETER 500Ω	1
VR1	RV:TM7S100R	POTENTIOMETER 100Ω	1
VR4	RV:V202	POTENTIOMETER 2KΩ	1
VR3	RV:V203	POTENTIOMETER 20KΩ	1
VR5,6	RV:V502	POTENTIOMETER 5KΩ	2
K2,5,6	SL:AG2119	RELAY	3
K1,3,4	SL:AG2129	RELAY	3
SW1	SS:2NB2X2AG		1
L1,12	TF:367		2
TP0～8	TM:LC-2-G-0	TEST PIN	9
U6,11	UA:CX20197		2
U12	UA:C393G2		1
U4,23	UA:LF357M		2
U22	UC:AC04SJ	CMOS IC	1
U2,3,7～10	UC:DG211CY	CMOS IC	6
U25,31	UC:HC00F	CMOS IC	2
U24	UC:HC04F	CMOS IC	1
U15,16	UC:HC14F	CMOS IC	2

PARTS LIST

AD—3524 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2066A	A/D BOARD 20K AD3524	1
U28,29	UC:HC166F	CMOS IC	2
U5	UC:HC4052F	CMOS IC	1
U17~20	UC:HC595	CMOS IC	4
U30	UC:HC74F	CMOS IC	1
U26,27	UC:HC85F	CMOS IC	2
U21	UR:TA79L005P	SWITCHING REGULATOR	1
	ET:CRP04		1
	04:A34766D	ANALOG CASE A	1
	04:A34767C	ANALOG CASE B	1
	04:A49163A		1
	05:A40701	6.5mm SPACER	6

PARTS LIST

AD—3524/25 AC P.S BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2067	AC P.S BOARD IN AD3524/25	1
C13,15,16,21	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	4
C1,2,5,27	CC:0.001U2KV	CERAMIC CAPACITOR 0.001μF	4
C11	CC:0.01U1KV	CERAMIC CAPACITOR 0.01μF	1
C3,9	CC:220P	CERAMIC CAPACITOR 220PF	2
C12	CC:220P1KV	CERAMIC CAPACITOR 220PF	1
C6,7	CK:SMG400VN330	ELECTROLYTIC CAPACITOR 330μF	2
C110,210	CK:SM160VB10	ELECTROLYTIC CAPACITOR 10μF 160V	2
C24	CK:SM450VB1	ELECTROLYTIC CAPACITOR 1μF 450V	1
C111,211	CK:SXE25VB10	ELECTROLYTIC CAPACITOR 10μF 25V	2
C14,22	CK:9120	ELECTROLYTIC CAPACITOR 120μF 25V	2
C19	CM:5002102J1	FILM CAPACITOR 1000PF 50V	1
C26	CM:5002104K1	FILM CAPACITOR 0.1μF 50V	1
C3,4	CM:6003104K	FILM CAPACITOR 0.01μF 600V	2
C25	CT:1D2R2	TANTALUM CAPACITOR 2.2μF 20V	1
C10,23,109,209	CT:1V010	TANTALUM CAPACITOR 1μF 35V	4
C20	CT:1V100	TANTALUM CAPACITOR 10μF 35V	1
D16	DF:TLP521-1	PHOTO COUPLER	1
D14,15	DF:TLP541G	PHOTO COUPLER	2
D7,8,12,13 D108,208	DI:AL01Z	DIODE	6
D5,6	DI:RG4C	DIODE	2
D9	DI:TFR1L	DIODE	1
D2,3,18	DI:1SS97	SCHOTTKY DIODE	3
D11,109,209	DI:1S1588	DIODE	3
D0	DI:4J4B44	DIODE BRIDGE	1
D17	DL:TLR102A	LED	1
D1	DT:5P5M	SCR	1
D110,210	DZ:05Z15	ZENER DIODE 15V	2
D4	DZ:05Z20	ZENER DIODE 20V	1
D10	DZ:05Z9.1	ZENER DIODE 9.1V	1
Z1	ET:SNR-391KD14		1
	HT:6073PB	HEAT SINK	2

PARTS LIST

AD—3524/25 AC P.S BOARD 2/3

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2067	AC P.S BOARD IN AD3524/25	1
J5	JT:173145-5	CONNECTOR	1
J1	JT:172369-5		1
J2	JT:172369-6		1
L3	LL:LH1-101K	INDUCTOR	1
L4	LL:LH1-682K	INDUCTOR	1
L301,304,307,310 L313,316,319,322	LL:MA10-21T	INDUCTOR	8
L1	LR:UF3834SH502Y	INDUCTOR	1
P1	PC:2067C	PRINT BOARD	1
	QA:AC254-1674	COOL SHEET	2
	QA:AC256-1674	COOL SHEET	2
	QA:AC316A	WASHER	2
Q5	QF:K534	FET	1
Q8	QT:A1015Y	TRANSISTOR	1
Q1	QT:A562	TRANSISTOR	1
Q4	QT:S65	TRANSISTOR	1
Q2	QT:C1959	TRANSISTOR	1
Q102,202	QT:C2073	TRANSISTOR	2
Q3	QT:C2235	TRANSISTOR	1
Q7	QT:D799	TRANSISTOR	1
R15	RC:NES125RJ	CARBON RESISTOR 25Ω	1
R3,221	RC:NAT1.2K	CARBON RESISTOR 1.2KΩ 1/4W	2
R25,26	RC:NAT1.5K	CARBON RESISTOR 1.5KΩ 1/4W	2
R13	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	1
R17	RC:NAT1M	CARBON RESISTOR 1MΩ 1/4W	1
R30	RC:NAT100K	CARBON RESISTOR 100KΩ 1/4W	1
R51,126	RC:NAT15K	CARBON RESISTOR 15KΩ 1/4W	2
R34,38,40	RC:NAT2.2K	CARBON RESISTOR 2.2KΩ 1/4W	3
R121	RC:NAT2.7K	CARBON RESISTOR 2.7KΩ 1/4W	1
R123,223	RC:NAT22K	CARBON RESISTOR 22KΩ 1/4W	2
R14	RC:NAT220R	CARBON RESISTOR 220Ω 1/4W	1
R11	RC:NAT3.3R	CARBON RESISTOR 3.3Ω 1/4W	1

PARTS LIST

AD—3524/25 AC P.S BOARD 3/3

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2067	AC P.S BOARD IN AD3524/25	1
R120,125	RC:NAT3.9K	CARBON RESISTOR 3.9KΩ 1/4W	2
R5.6,18.27.29	RC:NAT33K	CARBON RESISTOR 33KΩ 1/4W	5
R16,52	RC:NAT39K	CARBON RESISTOR 39KΩ 1/4W	2
R4,7,19.37,41,42	RC:NAT4.7K	CARBON RESISTOR 4.7KΩ 1/4W	6
R24,35	RC:NAT47K	CARBON RESISTOR 47KΩ 1/4W	2
R8,9,118,218	RC:NAT47R	CARBON RESISTOR 47Ω 1/4W	4
R119,219	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	2
R220	RC:NAT5.6K	CARBON RESISTOR 5.6KΩ 1/4W	1
R2	RC:NAT560R	CARBON RESISTOR 560Ω 1/4W	1
R21	RC:NAT680K	CARBON RESISTOR 680KΩ 1/4W	1
R28	RC:NAT750R	CARBON RESISTOR 750Ω 1/4W	1
R22	RC:NAT9.1K	CARBON RESISTOR 9.1KΩ 1/4W	1
R10	RC:1/2100K	CARBON RESISTOR 100KΩ 1/2W	1
R48,49,50,53	RC:1/2220K	CARBON RESISTOR 220KΩ 1/2W	4
R32,33	RE:MOS1/2R22		2
	RE:RGB5-10R	FUSE RESISTOR 10Ω	2
R40	RM:RNM2.2KF	METALIZED RESISTOR 2.2KΩ 1/4W	1
R31	RM:RNM2.32KF	METALIZED RESISTOR 2.32KΩ 1/4W	1
R39	RM:RNM5.62KF	METALIZED RESISTOR 5.62KΩ 1/4W	1
R36	RM:RNM9.31KF	METALIZED RESISTOR 9.31KΩ 1/4W	1
R20	RV:H102	POTENTIOMETER 1KΩ	1
	TF:3320	TRANSFORMER	1
TP1,2.3.4	TM:LC-2-G-0	TEST PIN	4
U2	UA:M33761	COMPARATOR	1
U1	UA:3759P-G	REGURATOR CONTROLLER	1
U103,203	UR:TL431CLPB	SWITCHING REGULATOR	2
	05:A40331	13mm SPACER	2
	05:A40410	21mm SPACER	2
	05:B41495	HEAT SINK	1
	10:D39	BOARD HOLDER	2

PARTS LIST

AD—3524/25 AC P.S BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2068	AC P.S BOARD CUT AD3524/25	1
C104,105,204,205	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	4
C303,308,316,320 C329,333	CC:0.001U	CERAMIC CAPACITOR 0.001μF	6
C107,206,305,322 C335	CC:0.001U2KV	CERAMIC CAPACITOR 0.001μF 2KV	5
C312,325	CC:0.0033U	CERAMIC CAPACITOR 0.0033μF	2
C336,338,341,343 C346,348	CC:0.01U	CERAMIC CAPACITOR 0.01μF	6
C101,201,301,306 C310,314,318,323 C327,331	CC:330P	CERAMIC CAPACITOR 330PF	10
C102,106	CK:SXE10VB3300	ELECTROLYTIC CAPACITOR 3300μF 10V	2
C311,324	CK:SXE10VB560	ELECTROLYTIC CAPACITOR 560μF 10V	2
C302,307,315,319 C328,332	CK:SXE16VB680	ELECTROLYTIC CAPACITOR 680μF 16V	6
C202,206	CK:9119	ELECTROLYTIC CAPACITOR 1200μF 16V	2
C108,209,304,309 C313,317,321,326 C330,334	CK:9120	ELECTROLYTIC CAPACITOR 120μF 25V	10
C203	CM:5002332K1	FILM CAPACITOR 3300PF 50V	1
C103	CM:5002472K1	FILM CAPACITOR 4700PF 50V	1
C120,121,220,221	CT:1D2R2	TANTALUM CAPACITOR 2.2μF 20V	4
C112,212	CT:1V010	TANTALUM CAPACITOR 1μF 35V	2
D102,202,302,304 D306,308,310,312 D314,316	DI:4L01Z	DIODE	10
D101	DI:ESC87-009	SCHOTTKY DIODE	1
D103～105,107 D203～205,207	DI:1S1588	DIODE	8
D201	DI:10DL2CZ41A	DIODE	1
D301,303,305,307 D309,311,313,315	DI:5DL2CZ41A	DIODE	8
D106,111,206,211 D401～408	DL:TLR102A	LED	12

PARTS LIST

AD—3524/25 AC P.S BOARD 2/3

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2068	AC P.S BOARD OUT AD3524/25	1
	JI:2-173146-0	CONNECTOR	1
	JI:700A2	CONNECTOR	2
J4	JI:704Q050-AU/M	CONNECTOR	1
	JT:171825-3		1
L104,204	LL:LF1-101K	INDUCTOR	2
L302,303,305,306 L308,309,311,312 L314,315,317,318 L320,321,323,324	LL:LH1-471K	INDUCTOR	16
L101	LL:MA18-14D	INDUCTOR	1
L201	LL:MA18-14S	INDUCTOR	1
L202	LR:CY26X16X10SA	INDUCTOR	1
L102	LR:CY26X16X10SB	INDUCTOR	1
L103,203	LR:SF-T12-36	INDUCTOR	2
L401,402,403	NF:D-08CZ	NOISE FILTER	3
	PC:2068C	PRINT BOARD	
	QA:AC254-1674	COOL SHEET	1
	QA:AC256-1674	COOL SHEET	1
Q301,302,303,304 Q305,306,307,308	QT:A965	TRANSISTOR	8
Q101,201	QT:A968Y	TRANSISTOR	2
R103,115,318,337	RC:NAT1.2K	CARBON RESISTOR 1.2KΩ 1/4W	4
R113,215,317,336	RC:NAT1.5K	CARBON RESISTOR 1.5KΩ 1/4W	4
R122,222,304,310 R323,329,342,348	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	8
R102	RC:NAT10R	CARBON RESISTOR 10Ω 1/4W	1
R109,208	RC:NAT100R	CARBON RESISTOR 100Ω 1/4W	2
R203,217,401,402 R404,405,407,408	RC:NAT12K	CARBON RESISTOR 12KΩ 1/4W	8
R124,125,224	RC:NAT15K	CARBON RESISTOR 15KΩ 1/4W	3
R202,315,334	RC:NAT180R	CARBON RESISTOR 180Ω 1/4W	3
R106,107,110,206 R209,210	RC:NAT2.2K	CARBON RESISTOR 2.2KΩ 1/4W	6
R104,204	RC:NAT2.7K	CARBON RESISTOR 2.7KΩ 1/4W	2

PARTS LIST

AD—3524/25 AC P.S BOARD 3/3

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2068	AC P.S BOARD OUT AD3524/25	1
R316,335	RC:NAT330R	CARBON RESISTOR 330Ω 1/4W	2
R303,309,322,328 R341,347	RC:NAT390R	CARBON RESISTOR 390Ω 1/4W	6
R117,403,406	RC:NAT4.7K	CARBON RESISTOR 4.7KΩ 1/4W	3
R112,116,212,216	RC:NAT47R	CARBON RESISTOR 47Ω 1/4W	4
R104,204,302,303 R308,309,321,322 R327,328,340,341 R346,347	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	14
R105,205	RC:NAT5.6K	CARBON RESISTOR 5.6KΩ 1/4W	2
R101,201,301,307 R313,314,320,326 R332,339,345,360	RC:NAT56R	CARBON RESISTOR 56Ω 1/4W	12
R213	RC:NAT6.8K	CARBON RESISTOR 6.8KΩ 1/4W	1
	RC:NAT9.1K	CARBON RESISTOR 9.1KΩ 1/4W	1
R306,312,325,331 R344,350	RM:RNM2.32KF	METALIZED RESISTOR 2.32KΩ	6
R305,311,324,330 R343,349	RM:RNM9.42KF	METALIZED RESISTOR 9.42KΩ	6
R108,114,207,214 R319,338	RV:H501	POTENTIOMETER 500Ω	6
R111,211	RW:RR149		2
TP6～20	TM:LC-2-G-0	TEST PIN	15
U101,201	UA:BA728	OP AMP	2
U102,202,301,302 U303,304,305,306 U307,308	UR:TL431CLPB	SWITCHING REGULATOR	10
	05:A497933		1
	07:B42408	BOARD SPACER	2
	10:D39	BOARD HOLDER	2

PARTS LIST

AD—3525 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:20668	A/D BOARD 100K AD3525	1
	MF:AMZ27		1
	MF:AMZ28		1
U1	MF:AMZ29		1
C5,6,7,34,35 C45～48,55,56 C94～97	CC:FK16Y5V1H104	CERAMIC CAPACITOR 0.1μF	16
C69～76	CC:F1H104K	CERAMIC CAPACITOR	8
C3	CC:0.001J	CERAMIC CAPACITOR 0.001μF	1
	CC:0.0033J	CERAMIC CAPACITOR 0.0033μF	1
C59,60,89	CC:10P	CERAMIC CAPACITOR	3
C31	CC:100P	CERAMIC CAPACITOR 100PF 50V	1
C91	CC:150P	CERAMIC CAPACITOR	1
C90	CC:22P	CERAMIC CAPACITOR	1
C2	CD:10C010D5		1
C36,37,51,52,53 C54,57	CK:KMA16VB100	ERECTROLYTIC CAPACITOR 100μF 35V	7
C8～11,23～28	CK:SRA10VB220MS	ERECTROLYTIC CAPACITOR 220μF 10V	10
C1	CM:E2334KS	FILM CAPACITOR	1
C4	CM:P1103JZ	FILM CAPACITOR	1
C22	CM:V1H684JZ2	FILM CAPACITOR	1
C12,13,16～21,32 C33,38～40,65,66 C77～80,85～87	CT:1C220	TANTALUM CAPACITOR 22μF 16V	22
	CT:1D100	TANTALUM CAPACITOR	3
C14,29,30,41～44 C63,64,67,68	CT:1E1R5-C	TANTALUM CAPACITOR	11
C50,58,61,81～84 C88,92,93	CT:1VR33	TANTALUM CAPACITOR 0.33μF 35V	10
VC2	CV:TZ03Z100YR	CAPACITOR	1
VC1	CV:TZ03Z2R3YR	CAPACITOR	1
PH6	DF:TLP521-3	PHOTO COUPLER	1
PH1～5	DF:6N137	PHOTO COUPLER	5
D4,5,7,8,16,17	DI:1SS53	DIODE	6
D9,10	DI:1SS97	SCHOTTKY DIODE	2

PARTS LIST

AD—3525 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:20668	A/D BOARD 100K AD3525	1
D13	DI:1S1588	DIODE	1
D3,6	DZ:RD5.6FB	DIODE	2
D14,15	DZ:05Z5.6	DIODE 5.6V	2
D11,12	DZ:05Z8.2	DIODE 8.2V	2
	ET:CRP04	BUZZER	1
J3	JA:XC5F-3222		1
J2	JI:96P-2.54DS	CONNECTOR	1
J1	JJ:TMP-J01X-A2		1
J4	JS:14120-01	IC SOCKET	2
L2～6,13	LL:LF1-220K	INDUCTOR	6
L7,8,9	LL:LF1-560K	INDUCTOR	3
NF1～4	NF:FB-43-101		4
NF10,11	NF:ZBF253S-01		2
	PC:2066C	PRINT BOARD	1
Q1	QF:A70A-SI	FET	1
	QF:A70A	FET	1
Q23,24	QT:A965	TRANSISTOR	2
Q2,3,16～20	QT:C1815Y	TRANSISTOR	7
Q21,22	QT:C2235	TRANSISTOR	2
Q5,7,9,11,13,15	QT:FB1L3N-L	TRANSISTOR	6
Q4,6,8,10,12,14	QT:FP1L3N-L	TRANSISTOR	6
R5,37	RC:NAT1.2K	CARBON RESISTOR 1.2KΩ 1/4W	2
R4,45,55～60 R64～67,78～80	RC:NAT1K	CARBON RESISTOR 1KΩ 1/4W	15
R2,21	RC:NAT1M	CARBON RESISTOR 1MΩ 1/4W	2
R63	RC:NAT1R	CARBON RESISTOR 1Ω 1/4W	1
R41～44	RC:NAT10K	CARBON RESISTOR 10KΩ 1/4W	4
R81	RC:NAT100K	CARBON RESISTOR 100KΩ 1/4W	1
R9,10,12	RC:NAT2.7K	CARBON RESISTOR 2.7KΩ 1/4W	3
R1,7,11,13,14,18 R19,34,35,38,39 R71,72,85～96	RC:NAT27R	CARBON RESISTOR 27Ω 1/4W	25
R84	RC:NAT270R	CARBON RESISTOR 270Ω 1/4W	1
R76,77	RC:NAT3.3K	CARBON RESISTOR 3.3KΩ 1/4W	2

PARTS LIST

AD—3525 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:2066B	A/D BOARD 100K AD3525	1
R75,99～101	RC:NAT33K	CARBON RESISTOR 33KΩ 1/4W	4
R15,20	RC:NAT470R	CARBON RESISTOR 470Ω 1/4W	2
R24～26	RC:NAT560R	CARBON RESISTOR 560Ω 1/4W	3
R82	RC:NAT82R	CARBON RESISTOR 82Ω 1/4W	1
R6	RE:FMR2B472K		1
R3	RF:RR129	CARBON RESISTOR NETWORK	1
R16,17	RF:RR130A	CARBON RESISTOR NETWORK	2
R8	RF:RR142	CARBON RESISTOR NETWORK	1
R68,69	RF:91RRF	CARBON RESISTOR NETWORK	2
R23	RM:RNM1.24KF	METALIZED RESISTOR 1.24KΩ 1/4W	1
R31,32	RM:RNM1.74KF	METALIZED RESISTOR 1.74KΩ 1/4W	2
R22.27	RM:RNM1KF	METALIZED RESISTOR 1KΩ 1/4W	2
R61,62,73,74	RM:RNM10KF	METALIZED RESISTOR 10KΩ 1/4W	4
R28	RM:RNM2.74KF	METALIZED RESISTOR 2.74KΩ 1/4W	1
R30.33	RM:RNM20.5KF	METALIZED RESISTOR 20.5KΩ 1/4W	2
R97,98	RM:RNM3.9KF	METALIZED RESISTOR 3.9KΩ 1/4W	2
R36,46～54	RM:RNM470RF	METALIZED RESISTOR 470Ω 1/4W	10
R40	RN:IHR-4-153MA	RESISTOR NETWORK	1
VR2	RV:TM7S-500R	POTENTIOMETER 500Ω	1
VR1	RV:TM7S100R	POTENTIOMETER 100Ω	1
VR4	RV:V202	POTENTIOMETER 2KΩ	1
VR3	RV:V203	POTENTIOMETER 20KΩ	1
VR5,6	RV:V502	POTENTIOMETER 5KΩ	2
LK2,5,6	SL:AG2119	RELAY	3
LK1,3,4	SL:AG2129	RELAY	3
SW1	SS:2NB2X2AG		1
L1.12	TF:367		2
TP0～8	TM:LC-2-G-0	TEST PIN	9
U6,11	UA:CX20197		2
U12	UA:C393G2		1
U4,23	UA:LF357M		2
U22	UC:AC04SJ	CMOS IC	1
U2,3,7～10	UC:DG2111CY	CMOS IC	6
U25,31	UC:HC00F	CMOS IC	2

PARTS LIST

AD—3525 A/D BOARD

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
	7PZ:20668	A/D BOARD 100K AD3525	1
U15,16	UC:HC14F	CMOS IC	2
U28,29	UC:HC166F	CMOS IC	2
U5	UC:HC4052F	CMOS IC	1
U17~20	UC:HC595	CMOS IC	4
U30	UC:HC74F	CMOS IC	1
U26,27	UC:HC85F	CMOS IC	2
U21	UR:TA79L005P	SWITCHING REGULATOR	1

AD3524/25 EXPLODED VIEW-1

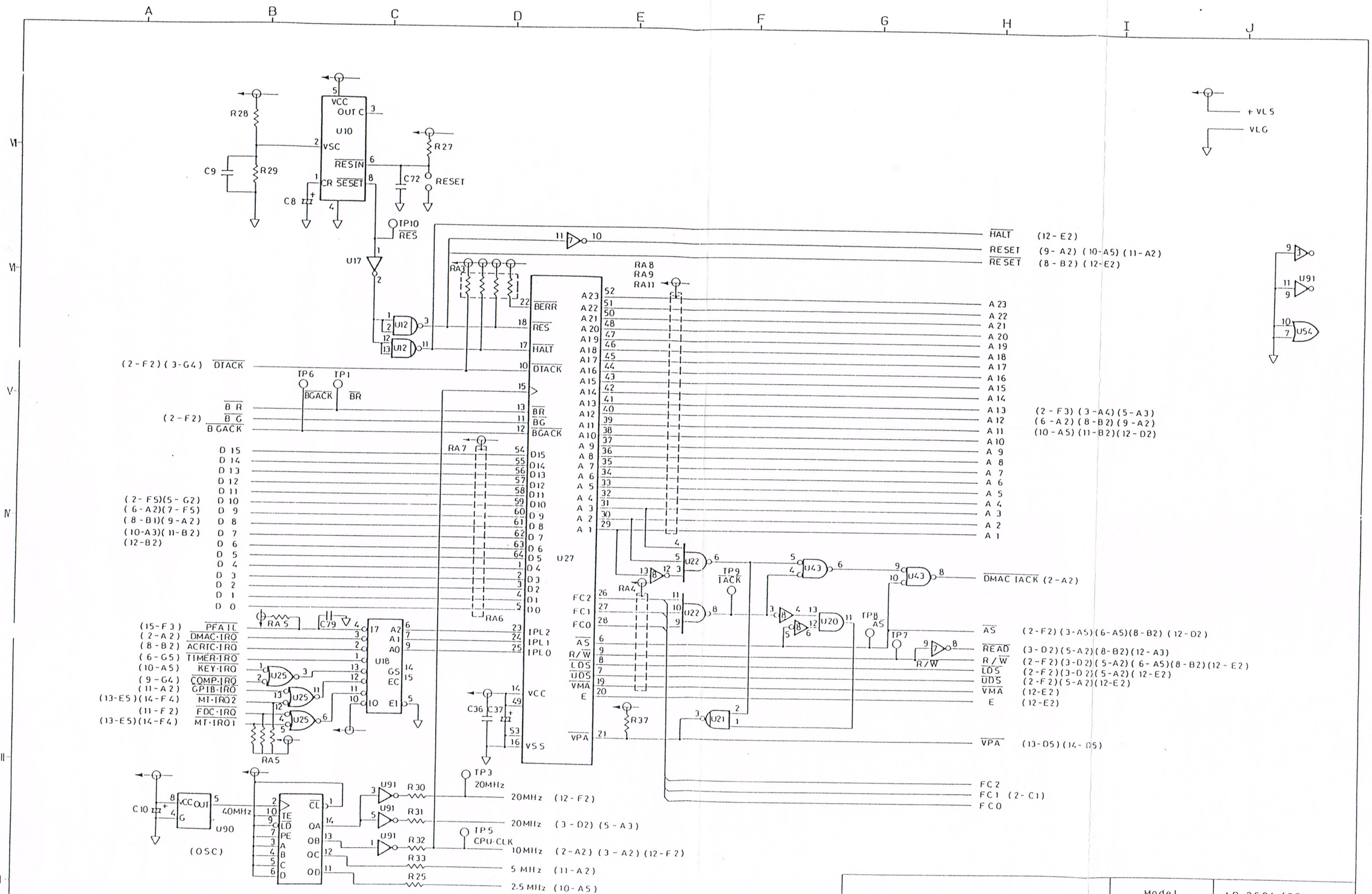
CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
1	04:A20132B	SUB PANEL	1
2	04:A48934A	P.SW FITTING PLATE	1
3	SP:SDS3P	POWER SWITCH	1
4	10:NO3142	PULL UP HANDLE	1
5	02:A48933-1B	GRIP SUPPORT AD	1
6	05:A35167A	SIDE FRAME	2
7	07:A30526	MOLE END	2
8	04:A34786A	CHASSIS	1
9	05:A40701	6.5㎜ SPACER (M3)	17
10	07:A45729	INSULATION COLLAR	4
11	07:A48936-1	FLOATING PLATE A	1
12	07:A48936-2	FLOATING PLATE B	1
13	ET:TM070Q1B	CRT	1
14	04:A34785B	CRT CASE	1
15	07:A47230	INSULATING PLATE B	3
16	04:A34768A	CENTER FRAME	1
17	07:A34770A	BOARD GUIDE A	1
18	10:50-4020	GUIDE RAIL	1
19	04:A34764	SG SHIELD PLATE	1
20	04:A34769	A/D SHIELD PLATE	2
21	10:D39	BOARD HOLDER	4
22	07:A48908	BOARD GUIDE C	2
23	07:A48907	BOARD GUIDE B	1
24	01:A34888	REAR PANEL	1
25	02:A49157	OP BLANK PANEL (B)	1
26	02:A49156	OP BLANK PANEL (A)	2
27	07:A49164A	REAR FOOT	4
28	02:A49155-1A	MASK LINE	1
a	M3×6	W SEMUSU (S)	18
b	M3×8	W SEMUSU (S)	12
c	M3×10	W SEMUSU (S)	33
d	M4×8	W SEMUSU (L)	4
e	M4×10	W SEMUSU (S)	8
f	M4×25		4
g	M3×6	FLAT SCREW	9
h	M3×8	FLAT SCREW	10
i	M2.6×6	FLAT SCREW	4
j	M5	HEXAGON NUT	2
k		SPRING WASHER	2
l		FLAT WASHER (L)	4

AD3524/25 EXPLODED VIEW-2

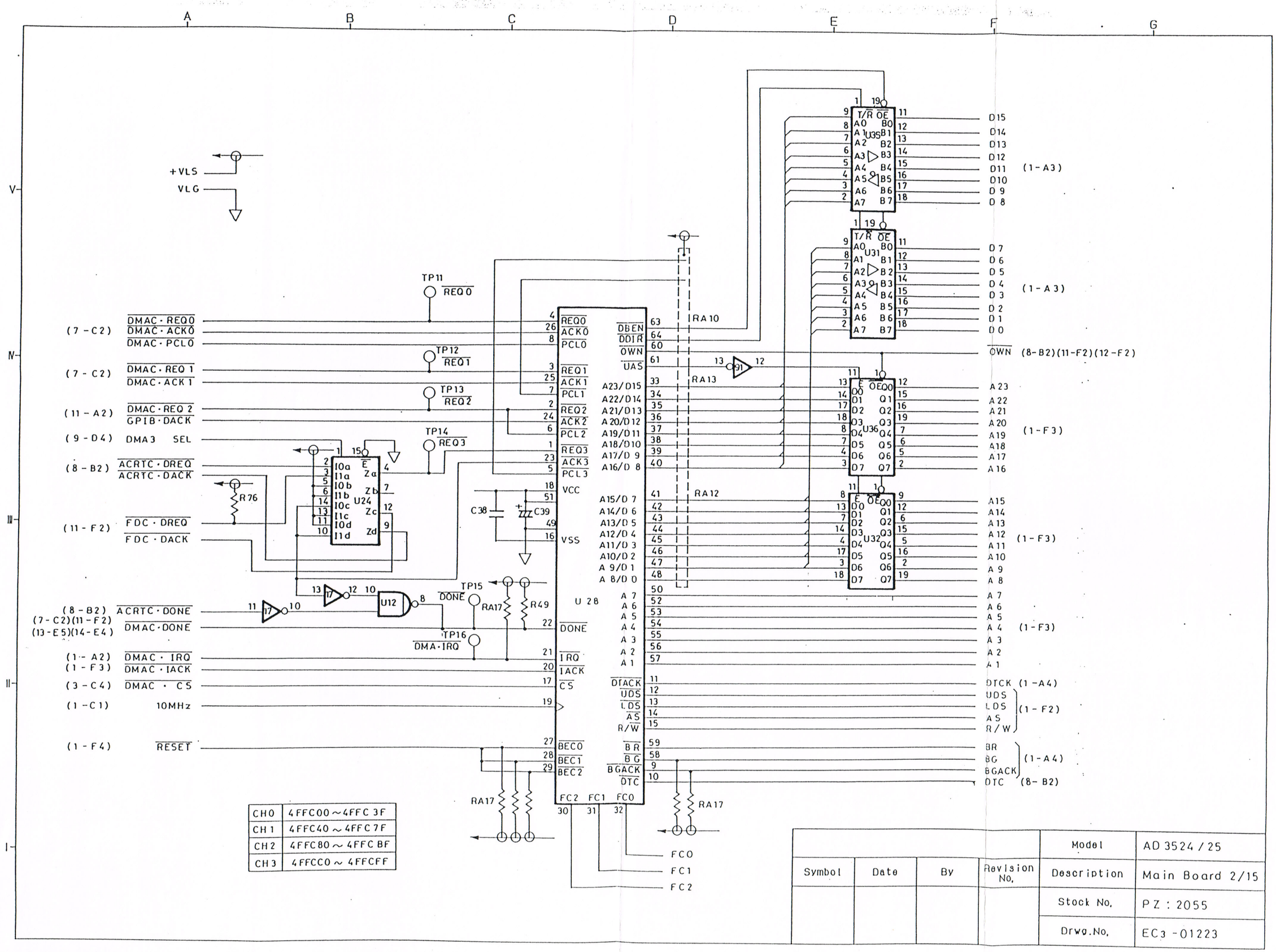
CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
1	09:A35166-1A	FRONT FRAME	1
2		FRONT COVER	1
3		MINI LATCH (S)	1
4		SPONGE	1
5	JC:BNC216	BNC CONNECTOR	3
6	04:A49151A	SHIELD PLATE	1
7	PZ:2057	FRONT KEY SW BOARD	1
8	01:A34886	FRONT PANEL	1
9		BOARD	1
10	04:A49152	PANEL SUPPORT (A)	1
11	04:A49153	PANEL SUPPORT (B)	1
12	04:A48935B	PANEL HOLDER	2
a	M2.6×6	TAPPING SCREW	9
b	M3×6	W SEMUSU	5
c	M3×6	SEMUSU	6
d	M3	OVAL LUG	2

AD3524/25 EXPLODED VIEW-3

CIRCUIT SYMBOL or DRWG. NO.	PARTS NAME	DESCRIPTION	Q'TY
1	02:A34784-1～nE	UPPER CASE	1
2	02:A34783-1～nC	LOWER CASE	1
3	10:3786-7001	FOOT STAND	1
4	10:3786-7001	FOOT STAND	1
5	10:3786-7002	HOLDING LEG	2
6	10:SJ-5023	RUBBER FOOT	4
7	10:K-18	RUBBER FOOT	2
8	09:A35361-1～n	PRINTER UNIT	1
9	02:A48823-1～nB	PRINTER BLANK PANEL	1
10	10:NO.3931	THUMB	2
11	07:B41242	MESH	2
12	06:B40366A	BOARD SUPPORT	1

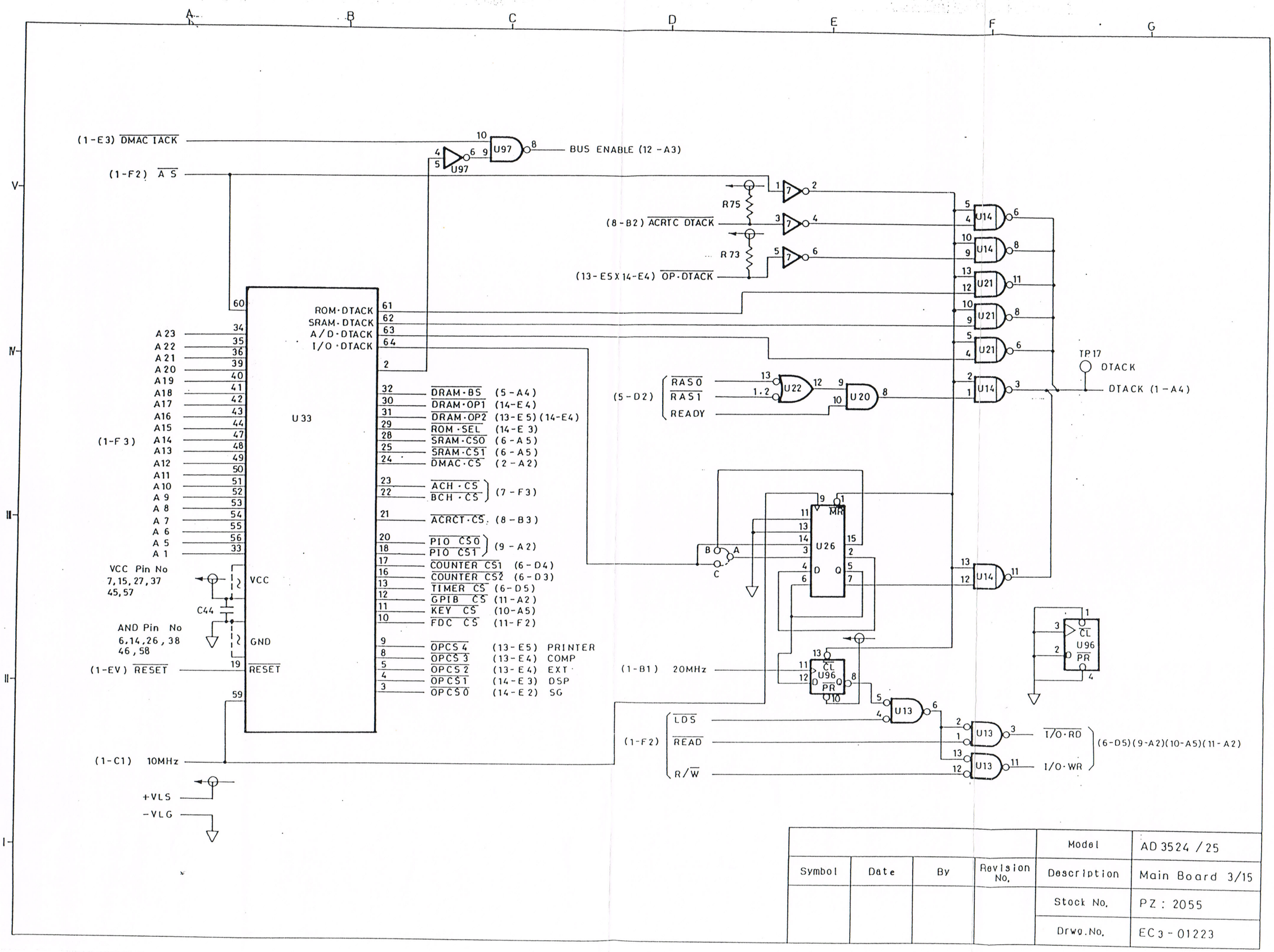


				Model	AD 3524/25
Symbol	Date	By	Revision No.	Description	Main Boad 1/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3-01223

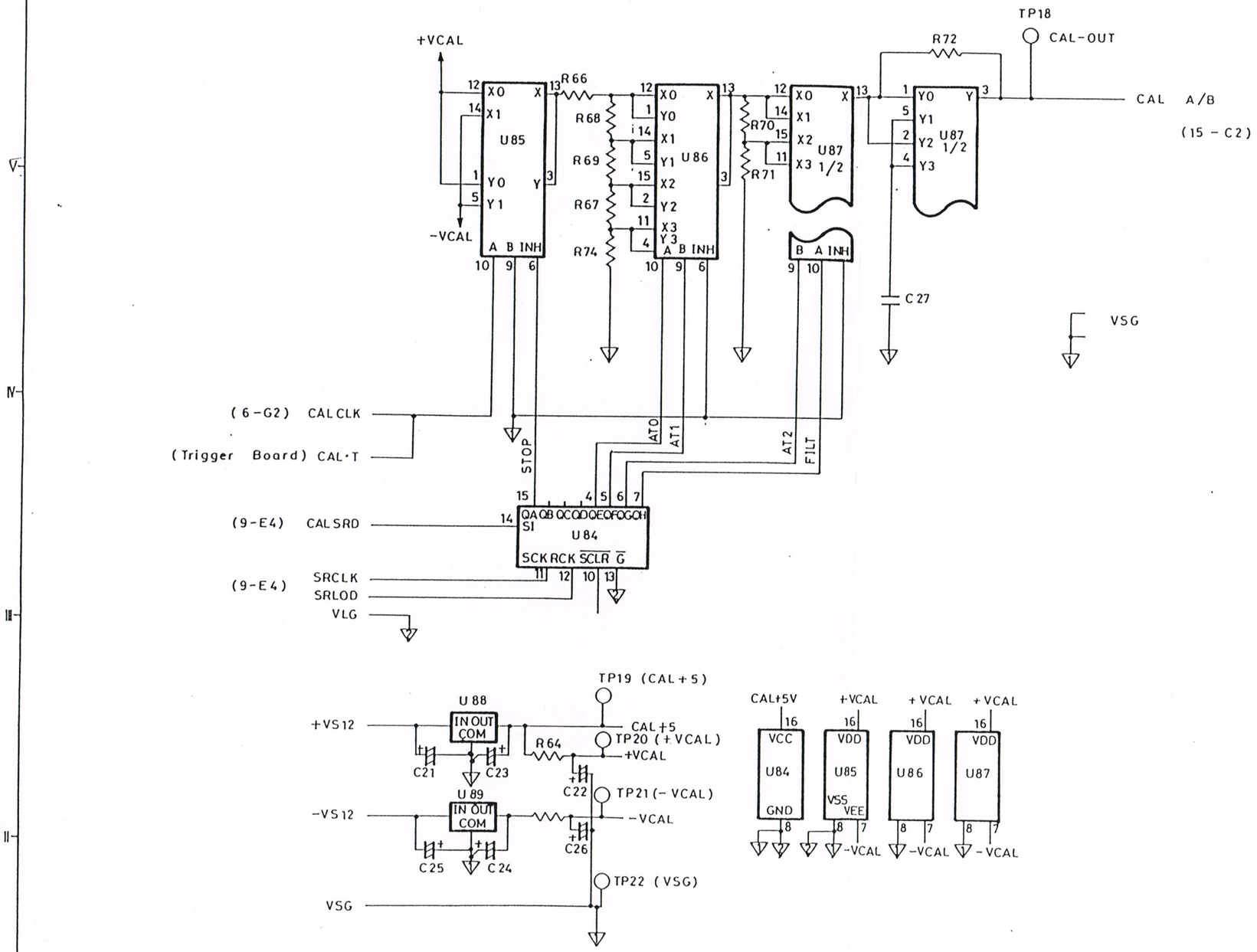


CH0	4FFC00～4FFC3F
CH1	4FFC40～4FFC7F
CH2	4FFC80～4FFCBF
CH3	4FFCC0～4FFCFF

Symbol	Date	By	Revision No.	Model	AD 3524/25
				Description	Main Board 2/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3-01223



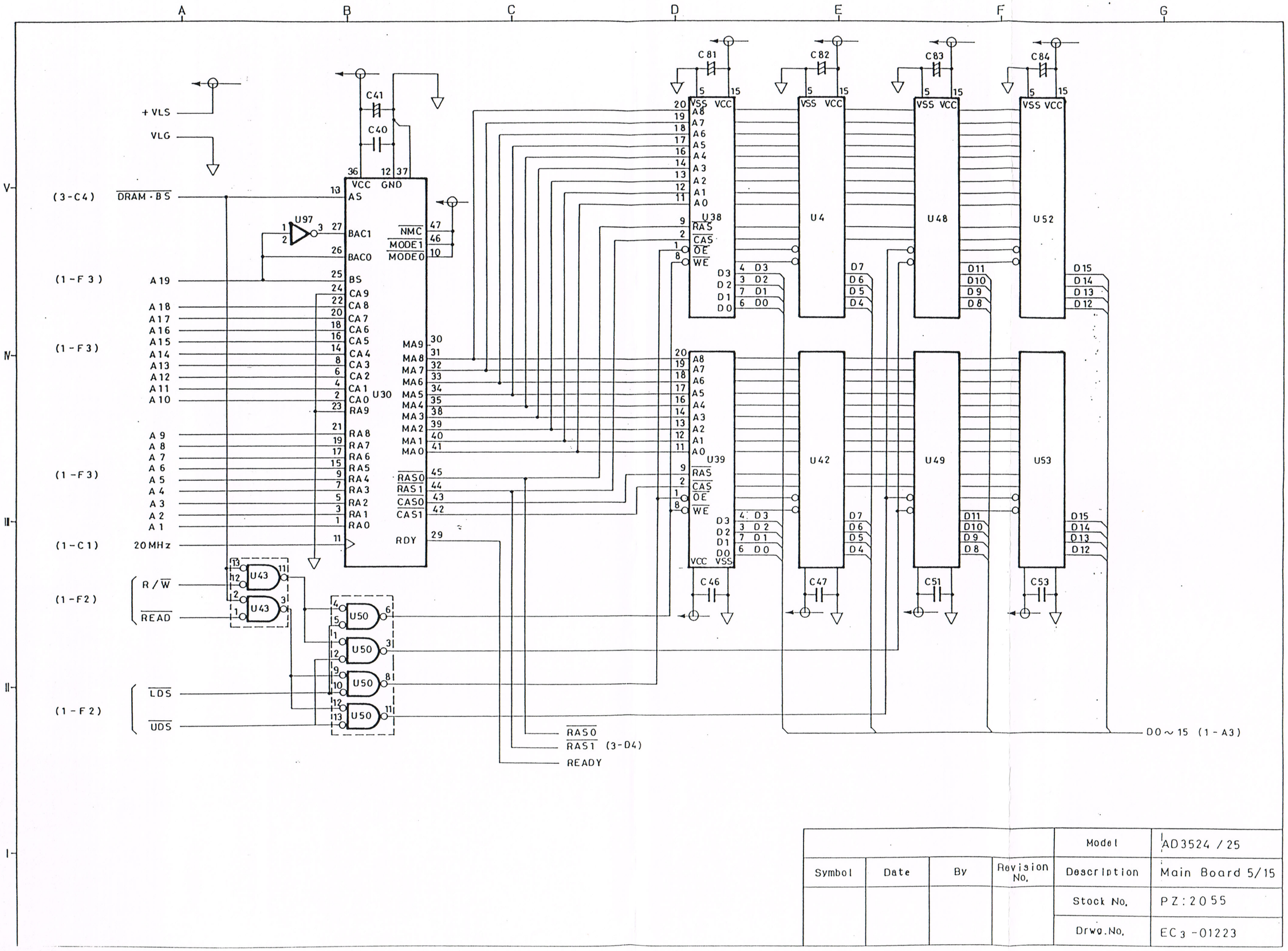
				Model	AD 3524 / 25
Symbol	Date	By	Revision No.	Description	Main Board 3/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3-01223



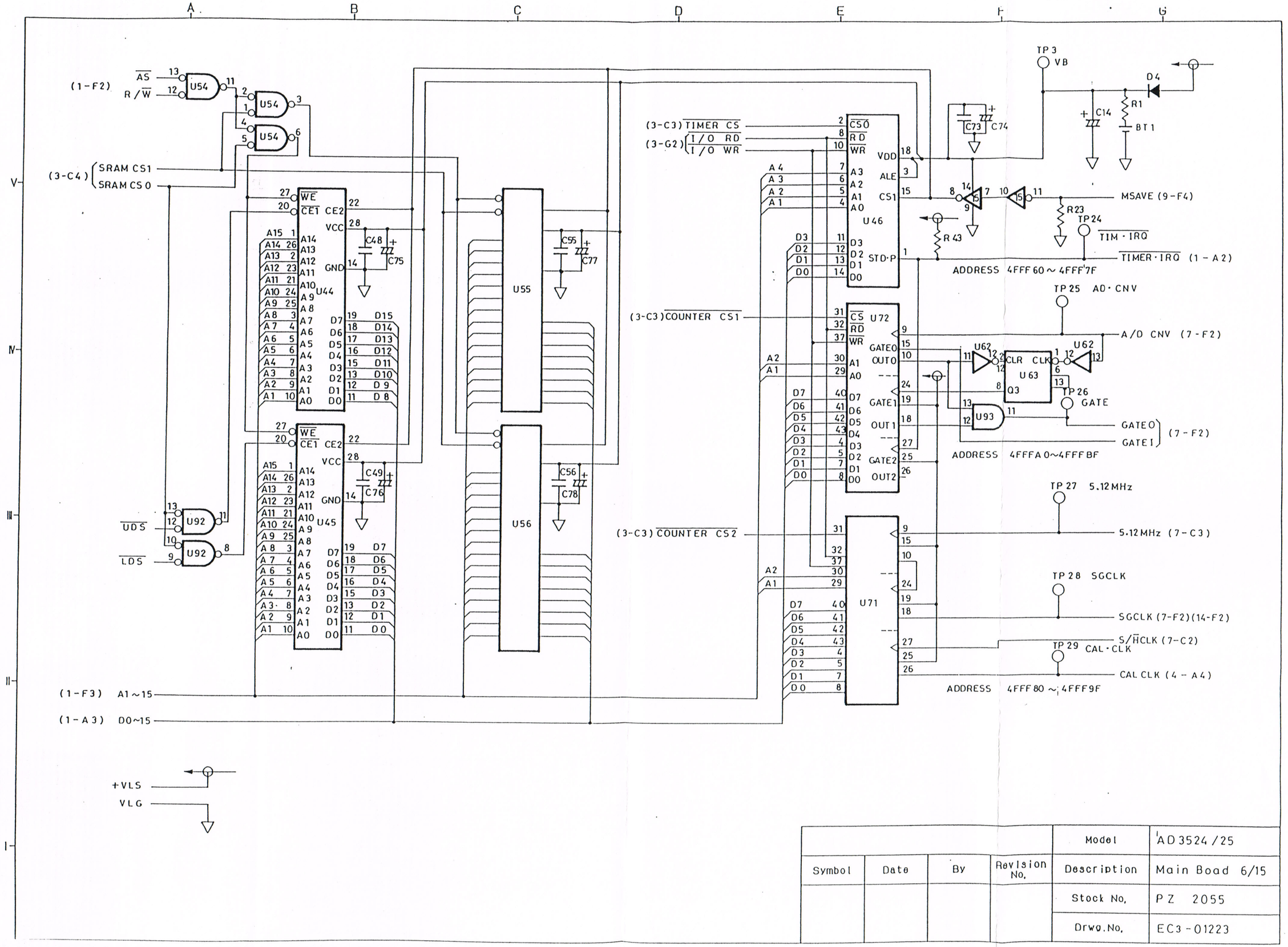
Ampli-tude (VP-P)	AT		
	0	1	2
10	0	0	0
3	1	0	0
1	0	1	0
0.3	0	0	1
0.1	1	0	1
0.03	0	1	1
0.00	1	1	1

FILT	
ON	1
OFF	0

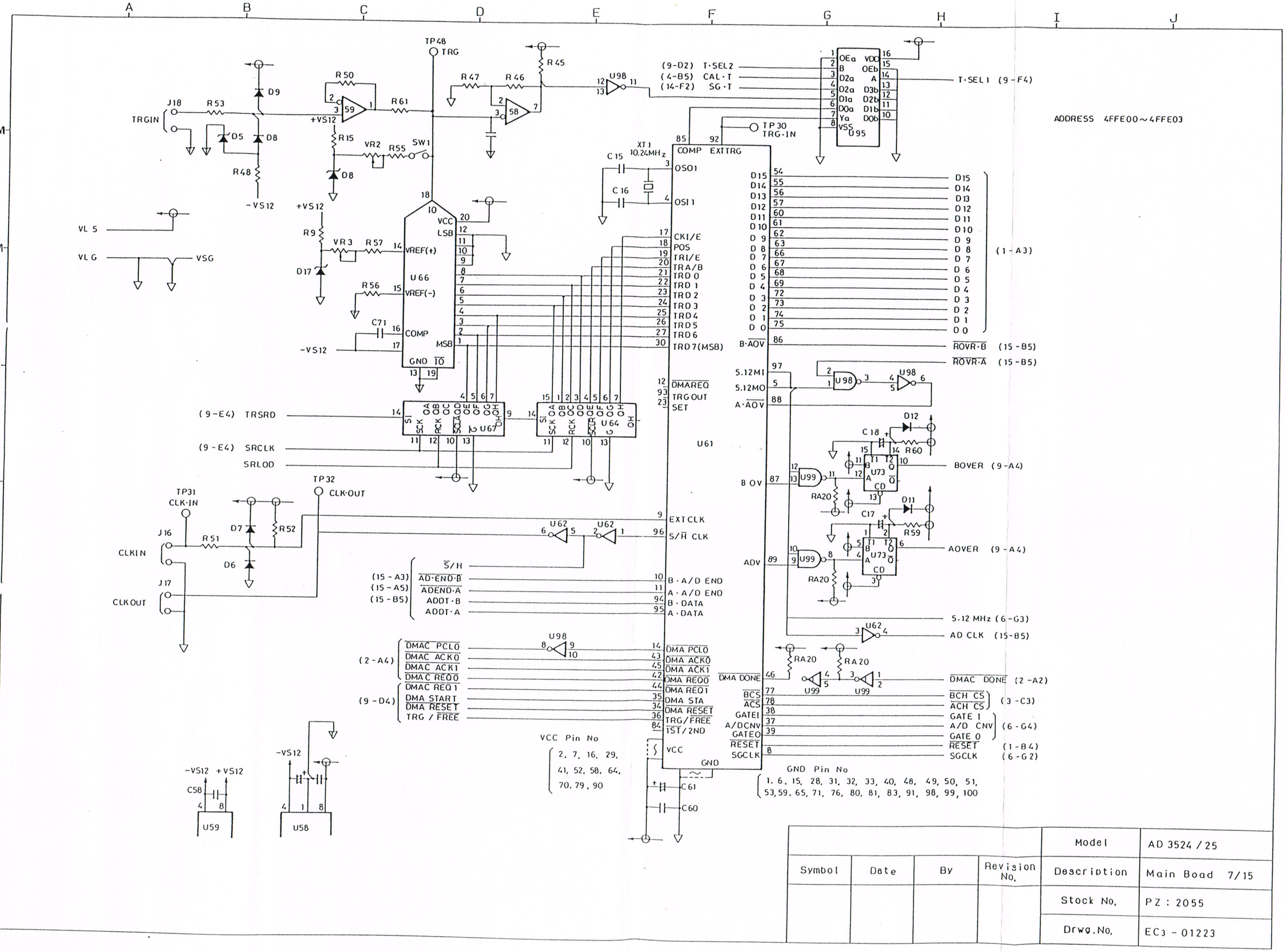
Symbol	Date	By	Revision No.	Model	AD3524/25
				Description	Main Board 4/15
				Stock No.	PZ:2055
				Drwg.No.	EC3-01223



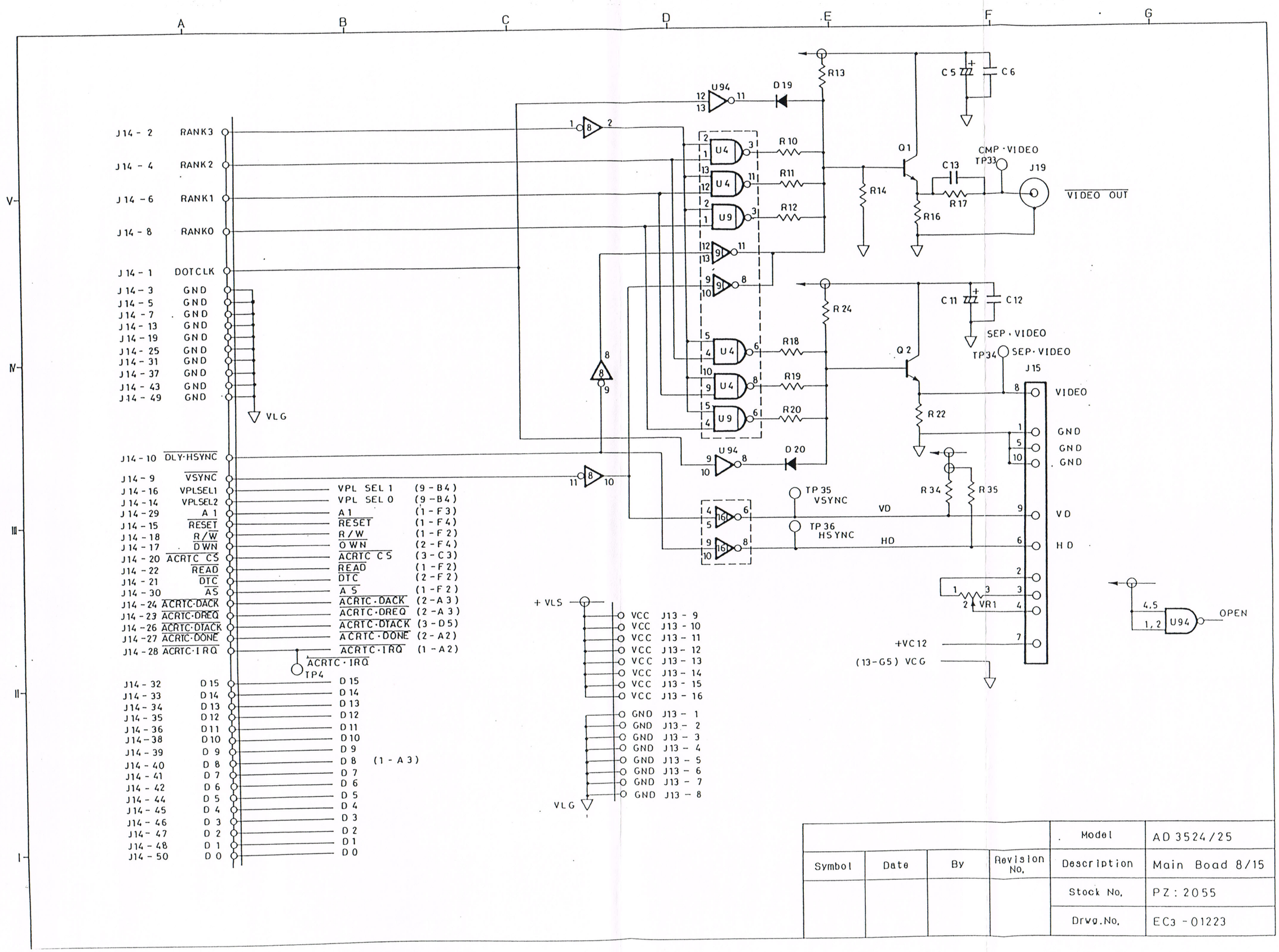
				Model	AD3524 / 25
Symbol	Date	By	Revision No.	Description	Main Board 5/15
				Stock No.	PZ:2055
				Drwg.No.	EC3-01223



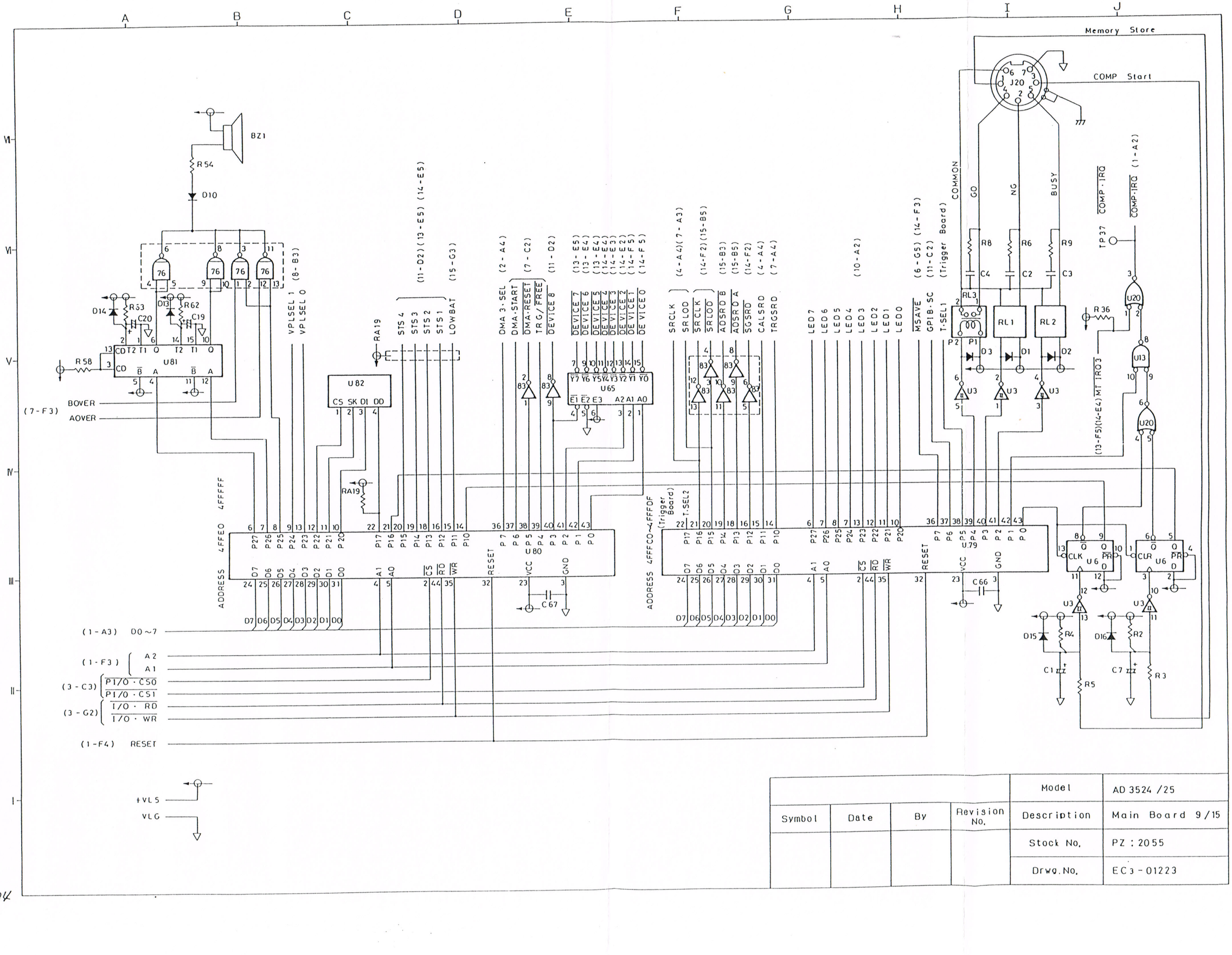
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	Main Boad 6/15
				Stock No.	PZ 2055
				Drwg.No.	EC3-01223



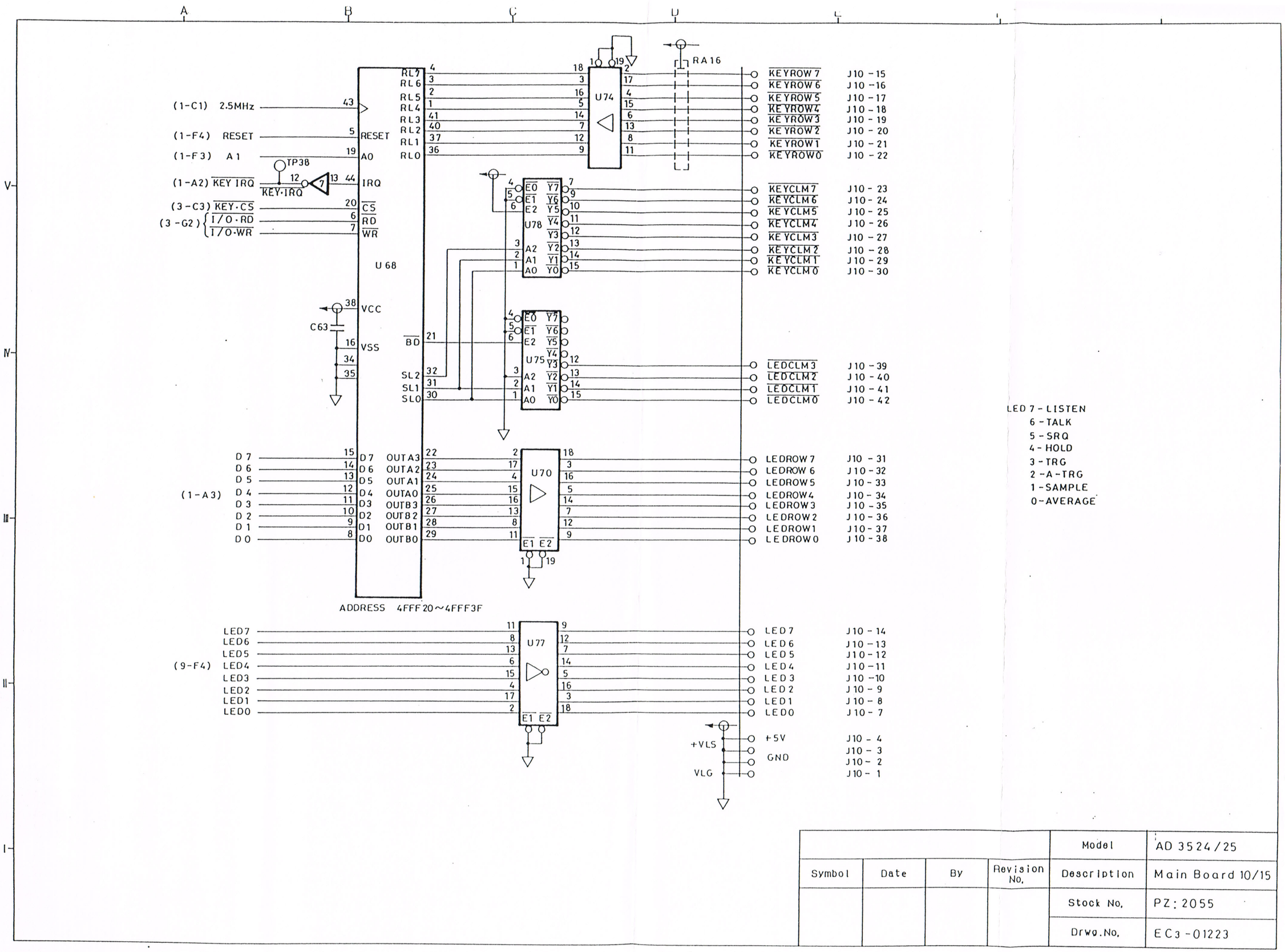
				Model	AD 3524 / 25
Symbol	Date	By	Revision No.	Description	Main Boad 7/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3 - 01223



				Model	AD 3524/25
Symbol	Date	By	Revision No.	Description	Main Boad 8/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3 - 01223



				Model	AD 3524 /25
Symbol	Date	By	Revision No.	Description	Main Board 9/15
				Stock No.	PZ : 2055
				Drwg. No.	EC3-01223



LED 7 - LISTEN
6 - TALK
5 - SRQ
4 - HOLD
3 - TRG
2 - A-TRG
1 - SAMPLE
0 - AVERAGE

				Model	AD 3524/25
Symbol	Date	By	Revision No.	Description	Main Board 10/15
				Stock No.	PZ: 2055
				Drwg.No.	EC3-01223

Model	AD 3524/25
Description	Main Boad 11/15
Stock No,	PZ : 2055
Drwg.No,	EC3 - 01223

Symbol	Date	By	Revision No,

TP40 FDC·IRQ

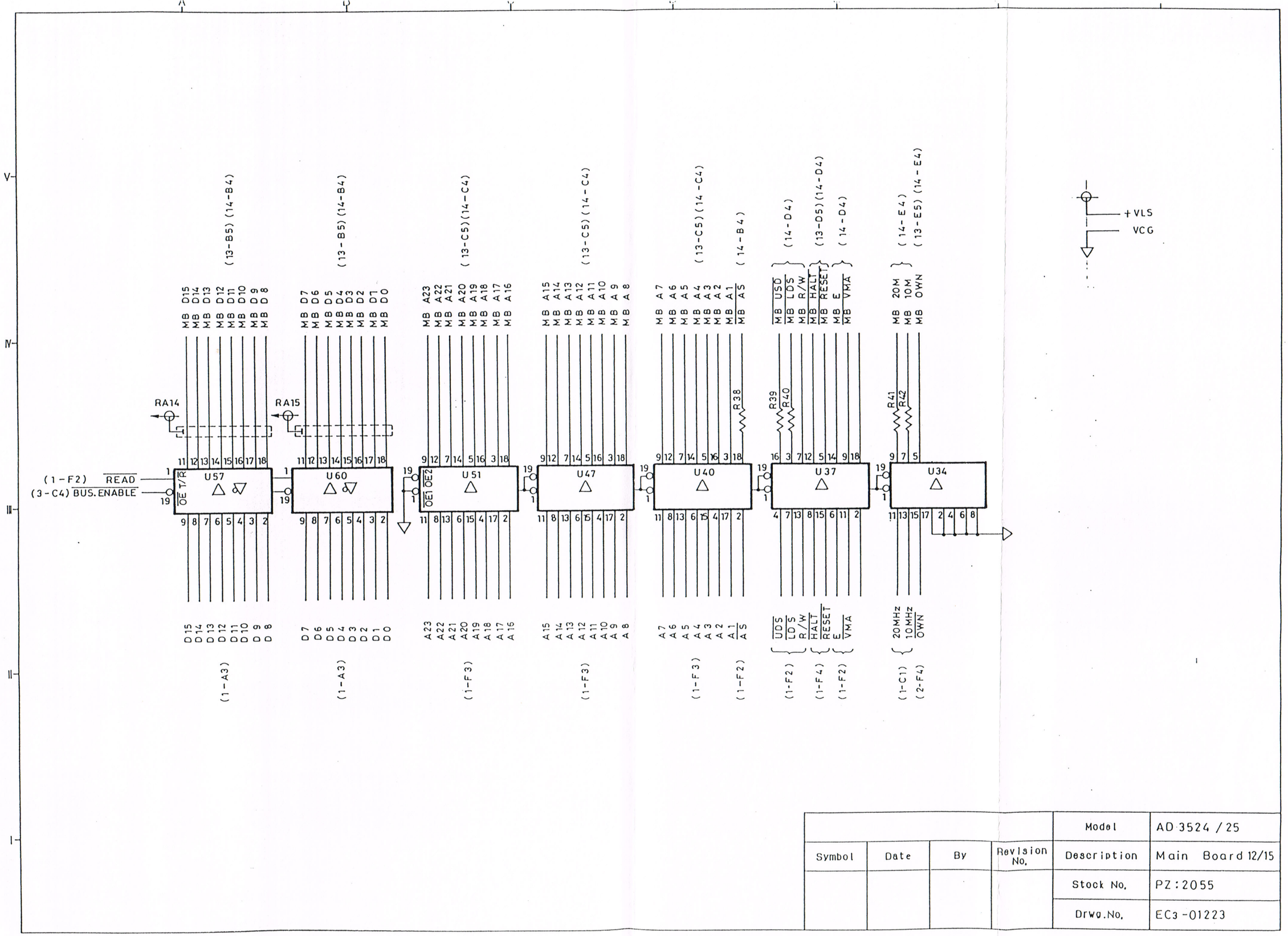
(1 - A2) FDC·IRQ — J11 - 34 FDC·IRQ
(2 - A2) DMAC·DONE — J11 - 32 DMAC·DONE
(2 - A3) FDC·DACK — J11 - 31 FDC·DACK
(2 - A3) FDC·DREQ — J11 - 30 FDC·DREQ
(2 - F4) OWN — J11 - 28 OWN
J11 - 27 RESET
J11 - 26 I/O·WE
J11 - 24 I/O·RD
(3 - C3) FDC·CS — J11 - 23 FDC·CS
J11 - 15 A1
J11 - 14 A2
J11 - 12 A3
J11 - 36 GND
J11 - 35 GND
J11 - 33 GND
J11 - 29 GND
J11 - 25 GND
J11 - 21 GND
J11 - 17 GND
J11 - 13 GND
J11 - 9 GND
J11 - 5 GND
J11 - 1 GND — VLG
J11 - 40 VCC
J11 - 39 VCC
J11 - 38 VCC
J11 - 37 VCC — +VLS
(9 - D4) DEVICE8 — J11 - 16 DEVICE8
(9 - C4) STS4 — J11 - 18 STS4
(9 - C4) STS3 — J11 - 19 STS3
(9 - C4) STS2 — J11 - 20 STS2
(9 - C4) STS1 — J11 - 22 STS1
J11 - 11 D0
J11 - 10 D1
J11 - 8 D2
J11 - 7 D3
J11 - 6 D4
J11 - 4 D5
J11 - 3 D6
J11 - 2 D7

(9 - F4) GPIB SC
(1 - A3) D0 D1 D2 D3 D4 D5 D6 D7
(1 - F3) A1 A2 A3
(1 - F4) RESET
(3 - G2) I/O·WR I/O·RD
(3 - C3) GPIB·CS
(2 - A4) GPIB·DACK
(2 - A4) DMAC·REQ2
(1 A2) GPIB·IRQ
(1 - C1) 5MHz

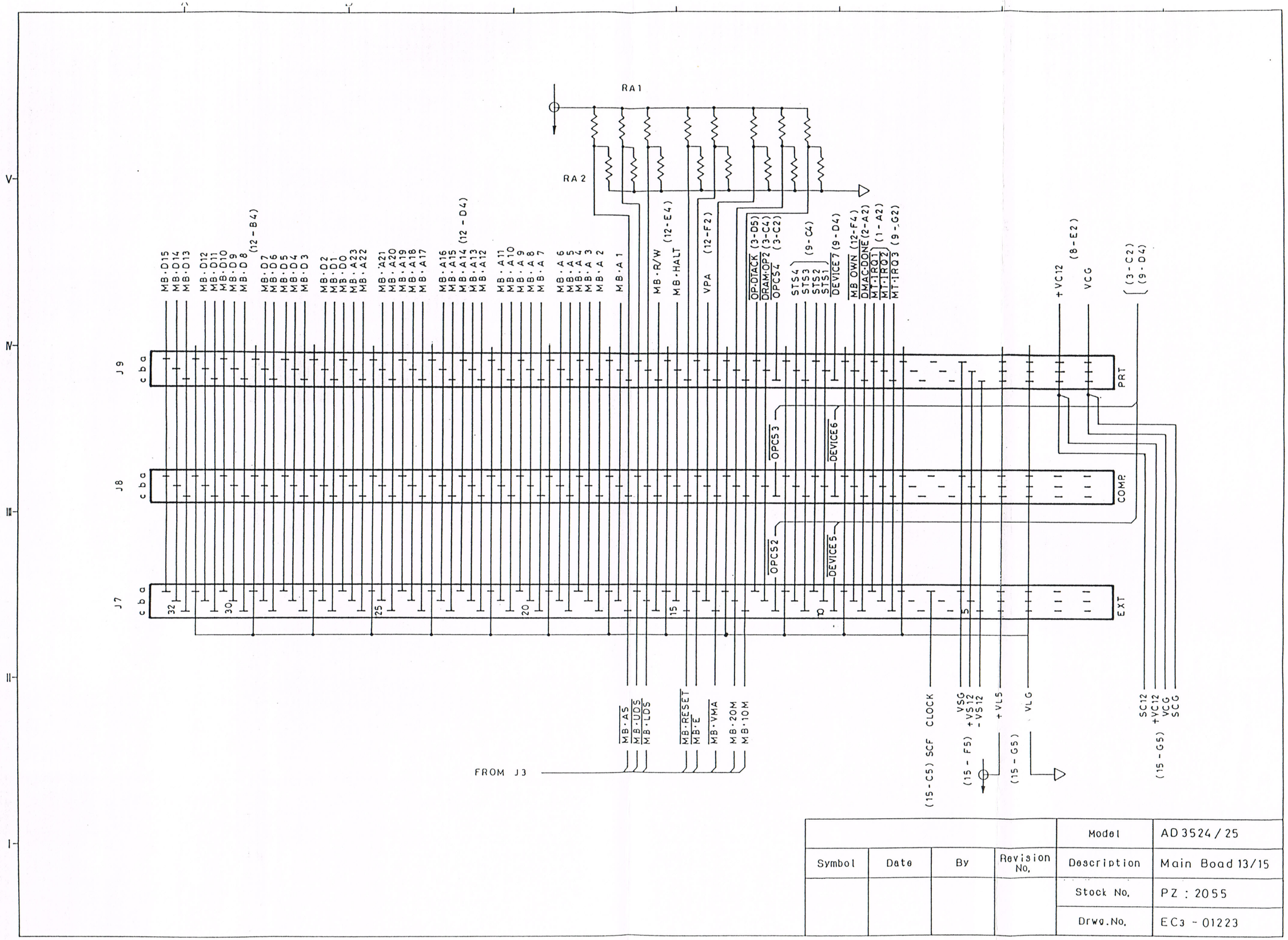
J22 - 12 FG
J22 - 24 LG
J22 - 23 SG
J22 - 22 SG
J22 - 21 SG
J22 - 20 SG
J22 - 19 SG
J22 - 18 SG
J22 - 10 SRQ
J22 - 11 ATN
J22 - 5 EOI
J22 - 6 DAV
J22 - 7 NRFD
J22 - 8 NDAC
J22 - 9 IFC
J22 - 17 REN
J22 - 1 DIO1
J22 - 2 DIO2
J22 - 3 DIO3
J22 - 4 DIO4
J22 - 13 DIO5
J22 - 14 DIO6
J22 - 15 DIO7
J22 - 16 DIO8

U1 U2 U5 U7 RA18 R26 C80 C20 TP39

ADDRESS 4FFF40 ~ 4FFF5F



				Model	AD-3524 / 25
Symbol	Date	By	Revision No.	Description	Main Board 12/15
				Stock No.	PZ:2055
				Drwg.No.	EC3-01223



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	Main Boad 13/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3 - 01223

J3 J4 J5 J6

c b a

32 30 25 20 15 10 5

MB·D15
MB·D14
MB·D13
MB·D12
MB·D11
MB·D10
MB·D9
MB·D8 (12-B4)
MB·D7
MB·D6
MB·D5
MB·D4
MB·D3
MB·D2
MB·D1
MB·D0
MB·A23
MB·A22
MB·A21
MB·A20
MB·A19
MB·A18
MB·A17
MB·A16
MB·A15
MB·A14 (12-D4)
MB·A13
MB·A12
MB·A11
MB·A10
MB·A9
MB·A8
MB·A7
MB·A6
MB·A5
MB·A4
MB·A3
MB·A2
MB·A1
MB·AS (12-D4)
MB·USD
MB·LDS
MB·R/W (12-E4)
MB·HALT
MB·RESET
MB·E
VPA (1-F2)
MB·VMA (12-E4)
MB·20M
MB·10M (12-F4)
OP·DTACK (3-D5)
DRAM·OP2 (3-C4)
DRAM·OP1 (3-C4)

MB·AS
MB·UDS
MB·LDS
MB·RESET
MB·E
MB·VMA
MB·25M
MB·12.5M

OPCS0
ROM·SEL
OPCS1
DEVICE2
DEVIE3
SGSRD
SRLOD
SRCLK
SGCLK

TO J7
(Trigger Board)
T SG
RA4
VSG (15-F5)
+VS12
-VS12
+VL5 (15-G5)
VLG

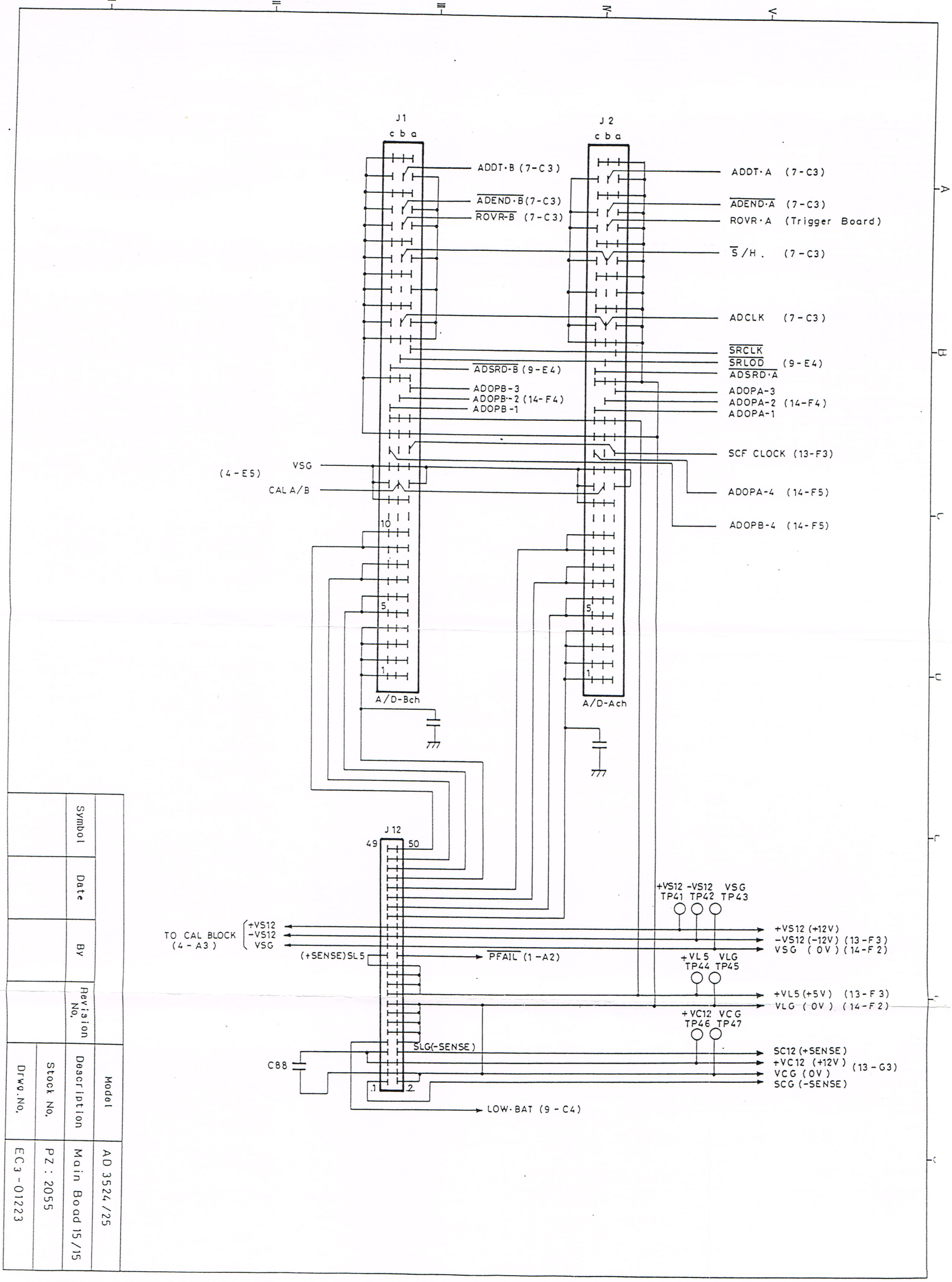
STS4
STS3
STS2
STS1 (9-C4)
DEVICE4 (9-D4)
MB·OWN (12-F4)
DMAC DONE (2-A2)
MT·IRQ1
MT·IRQ2 (1-A2)
MT·IRQ3 (9-G2)
ADOPB4
ADOPB3
ADOPB2
ADOPB1 (15-B3)
ADOPA4
ADOPA3
ADOPA2
ADOPA1 (15-B5)
U29
G1
G2
DEVICE0
DEVICE1 (9-D4)
MSAVE (9-F4)

SG ROM DSP RAM

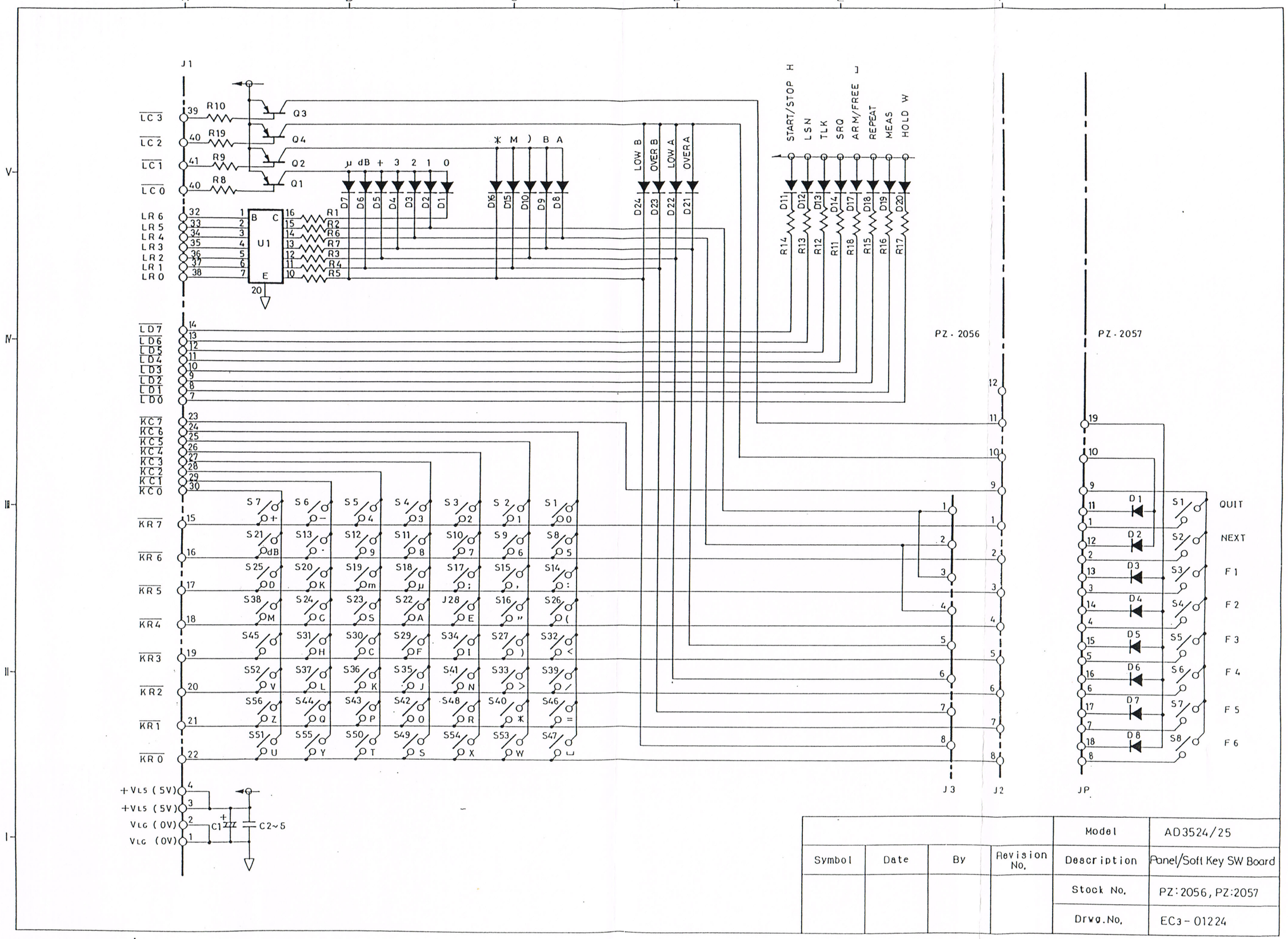
(3-C2)(3-C4)(6-G2)
(9-D4)(9-E4)

Symbol	Date	By	Revision No.

Model	AD 3524/25
Description	Main Board 14/15
Stock No.	PZ : 2055
Drwg.No.	EC3-01223

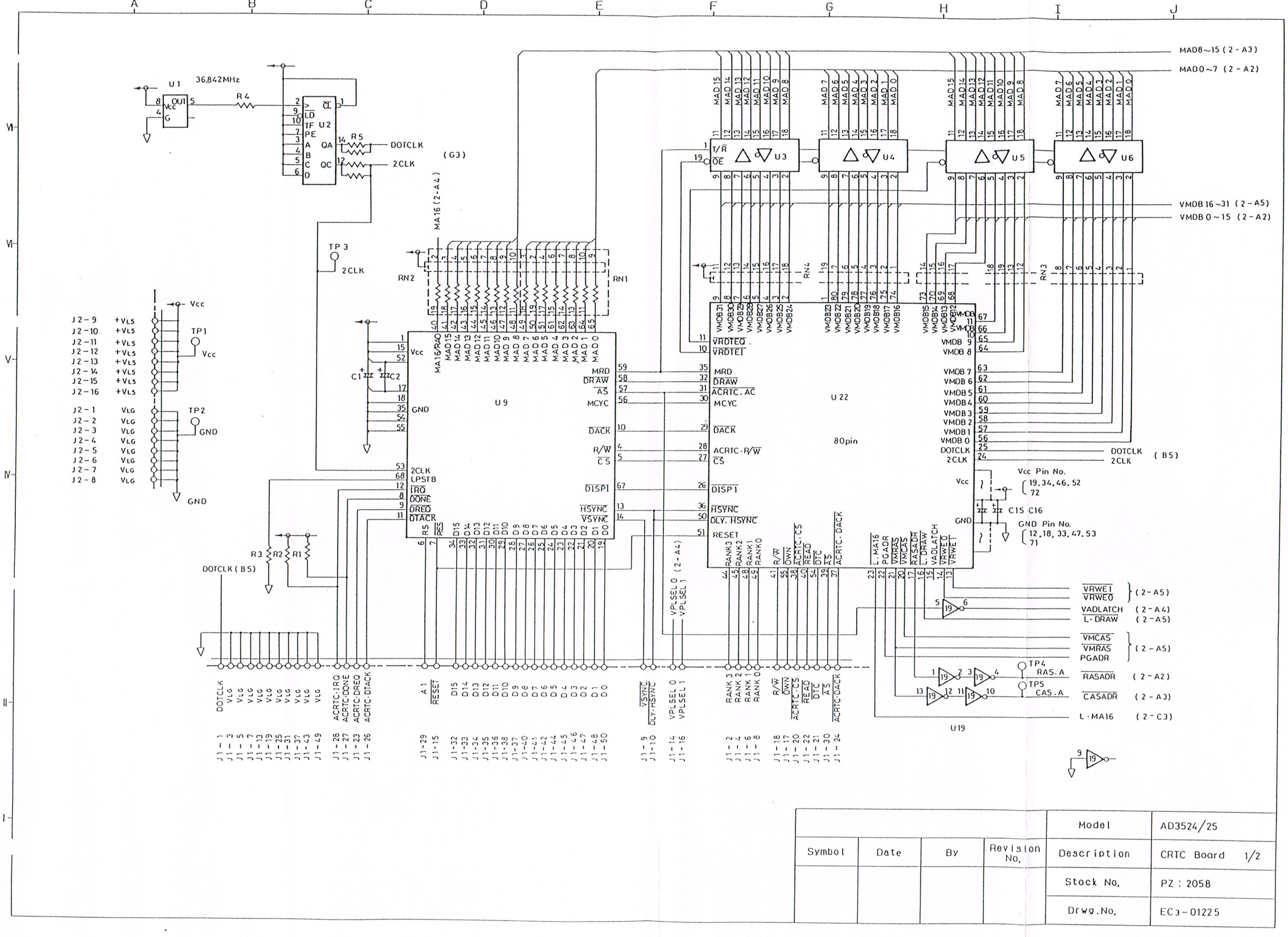


Symbol	Date	By	Revision No.	Model	AD 3524/25
				Description	Main Boad 15/15
				Stock No.	PZ : 2055
				Drwg.No.	EC3-01223



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	Panel/Soft Key SW Board
				Stock No.	PZ:2056, PZ:2057
				Drwg.No.	EC3-01224

4/



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	CRTC Board 1/2
				Stock No.	PZ : 2058
				Drwg.No.	EC3-01225

42

(1-G5) VMDB16~31

(1-G2) VMRAS, VMCAS, VRWE1, VRWE0, L.DRAW

(1-G2) PGADR

(1-D3) VPLSEL 1, VPLSEL 0

TP6 VADL

(1-G2) VADLATCH

(1-C5) MA16

(1-G5) MAD 15, MAD 14, MAD 13, MAD 12, MAD 11, MAD 10, MAD 9, MAD 8

(1-G2) CASADR

(1-G5) MAD 7, MAD 6, MAD 5, MAD 4, MAD 3, MAD 2, MAD 1, MAD 0

(1-G2) RASADR

(1-G5) VMDB0~15

U21, U18, U17, U16, U20

L·MA16

LCC-18p-M02

U8, U7

C8, C7, C11, C9, C13, C10, C14, C12

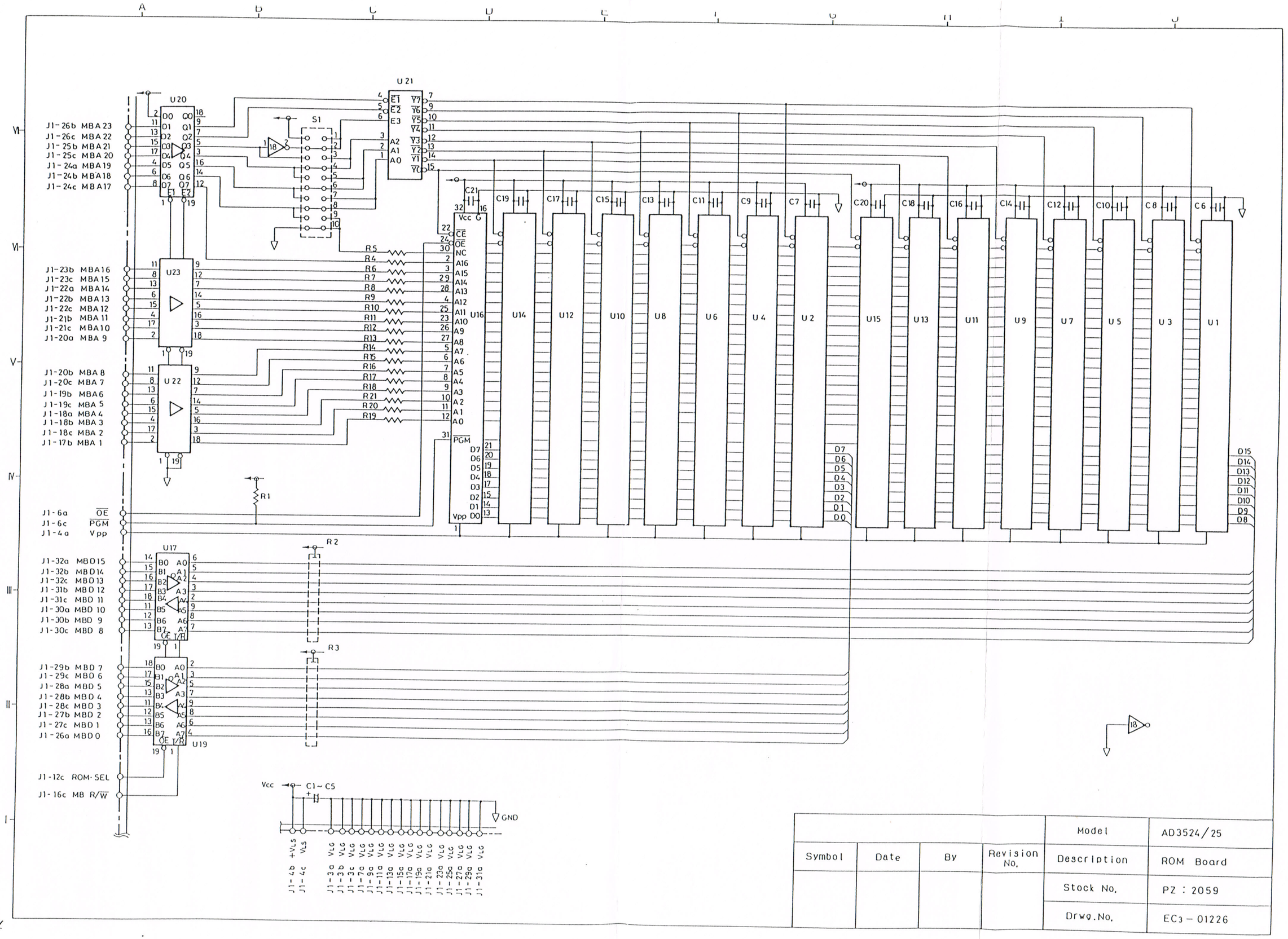
U11, U13, U15, U10, U12, U14

VMDB16, VMDB17, VMDB18, VMDB19, VMDB20, VMDB21, VMDB22, VMDB23, VMDB24, VMDB25, VMDB26, VMDB27, VMDB28, VMDB29, VMDB30, VMDB31

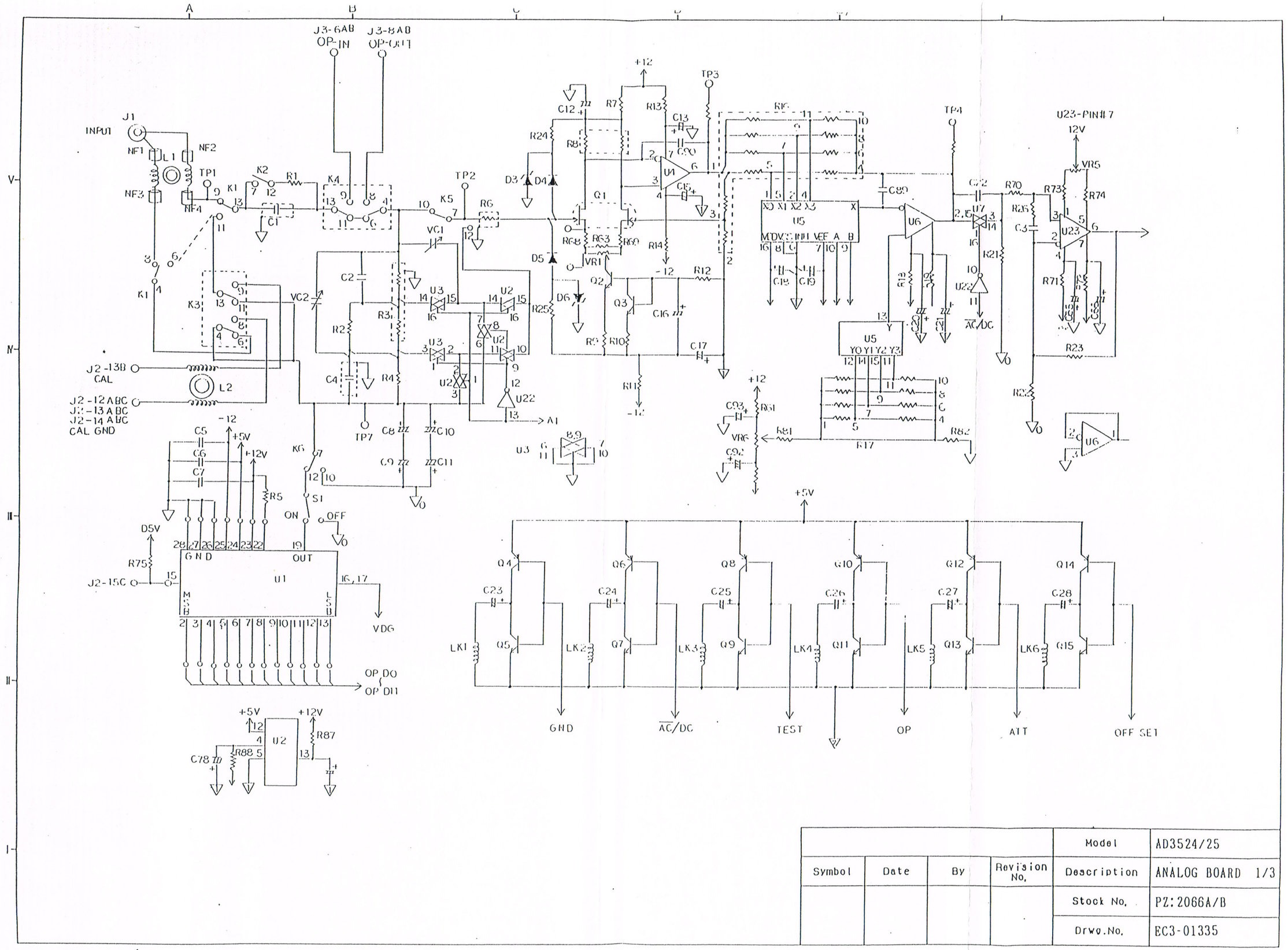
VMDB0, VMDB1, VMDB2, VMDB3, VMDB4, VMDB5, VMDB6, VMDB7, VMDB8, VMDB9, VMDB10, VMDB11, VMDB12, VMDB13, VMDB14, VMDB15

Vcc, GND

				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	CRTC Board 2/2
				Stock No.	PZ:2058
				Drwg.No.	EC3-01225

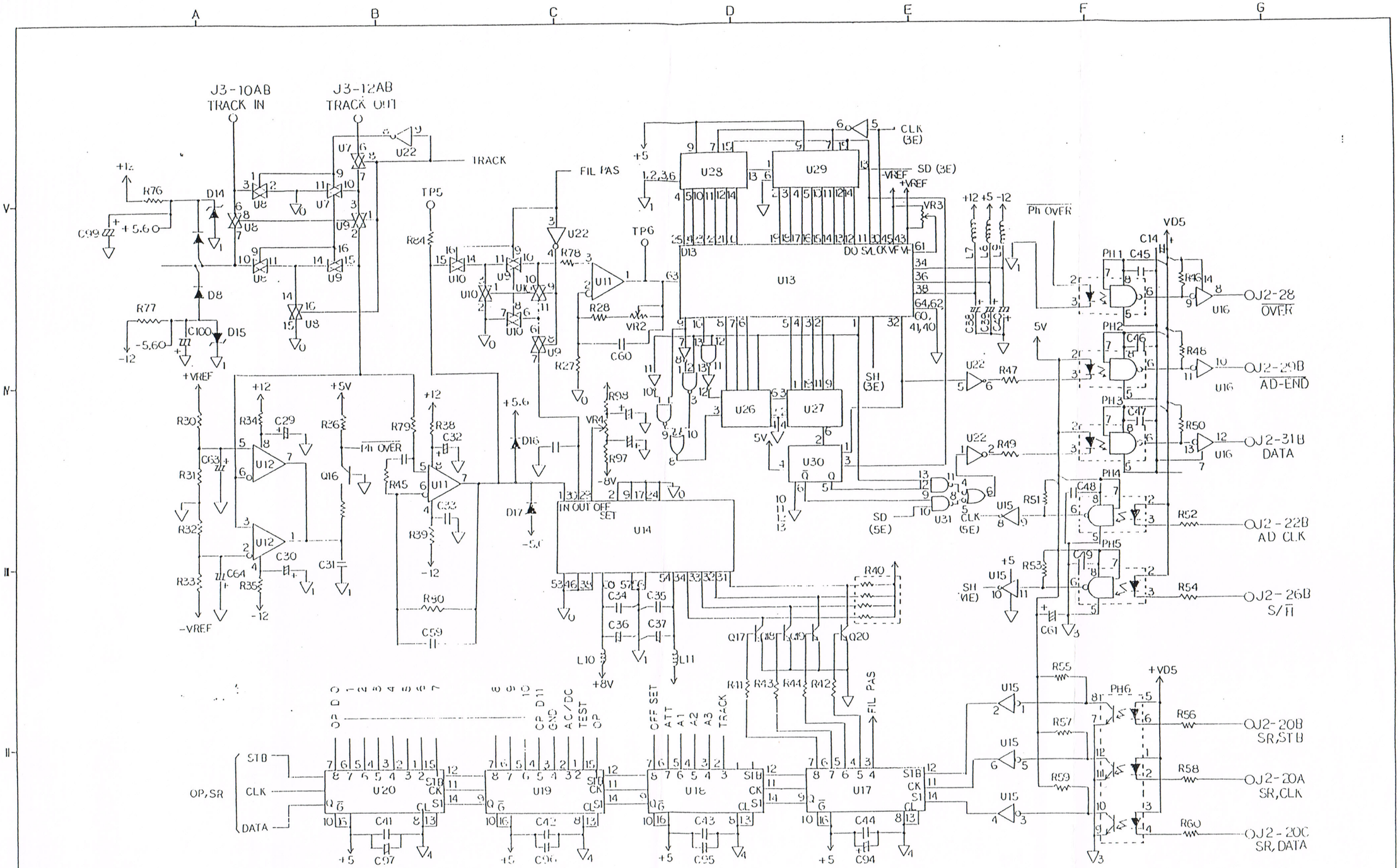


				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ROM Board
				Stock No.	PZ : 2059
				Drwg.No.	EC3 – 01226

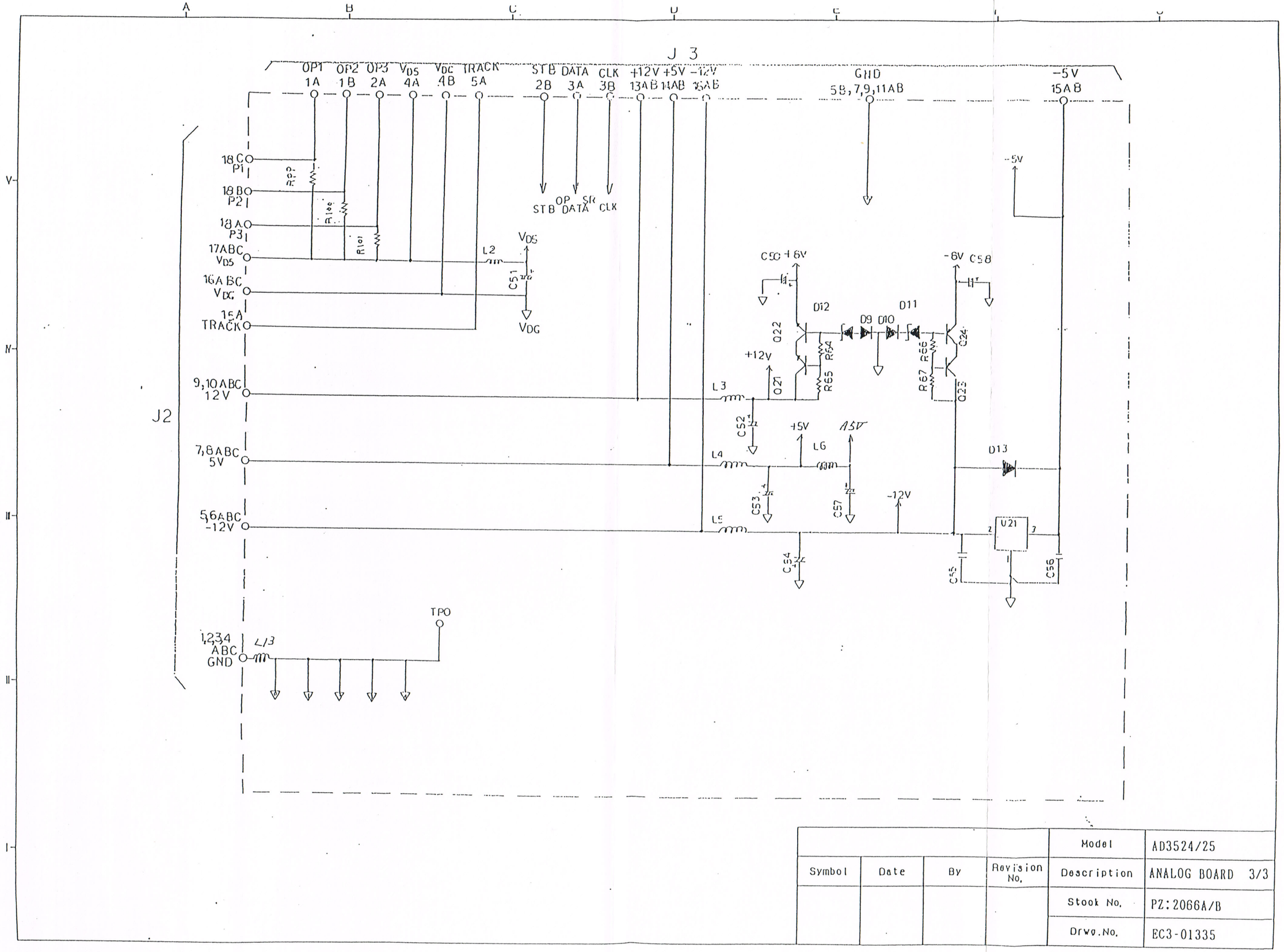


				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ANALOG BOARD 1/3
				Stock No.	PZ:2066A/B
				Drwg.No.	EC3-01335

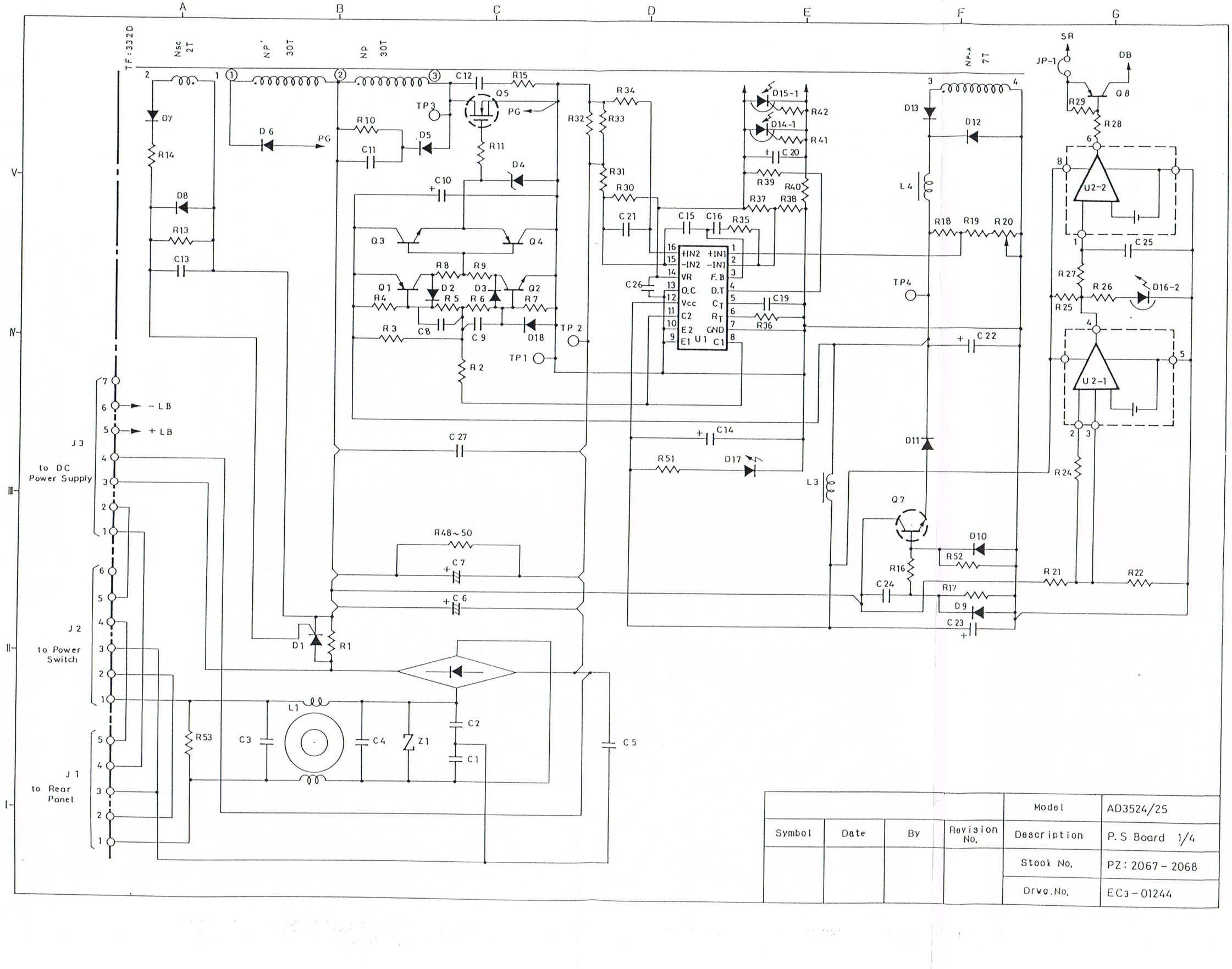
45



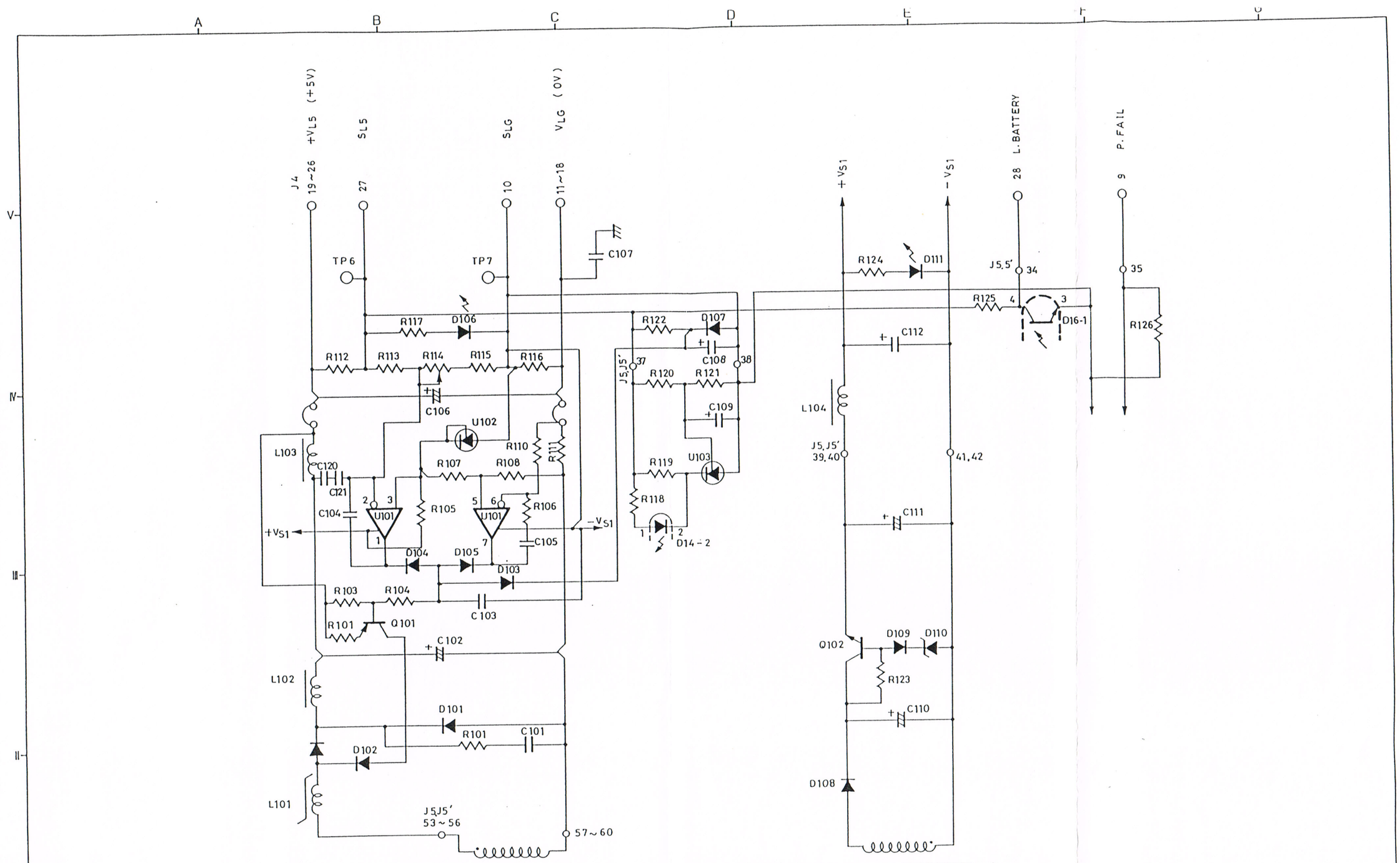
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ANALOG BOARD 2/3
				Stock No.	PZ:2066A/B
				Drwg.No.	EC3-01335



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ANALOG BOARD 3/3
				Stock No.	PZ:2066A/B
				Drwg.No.	EC3-01335

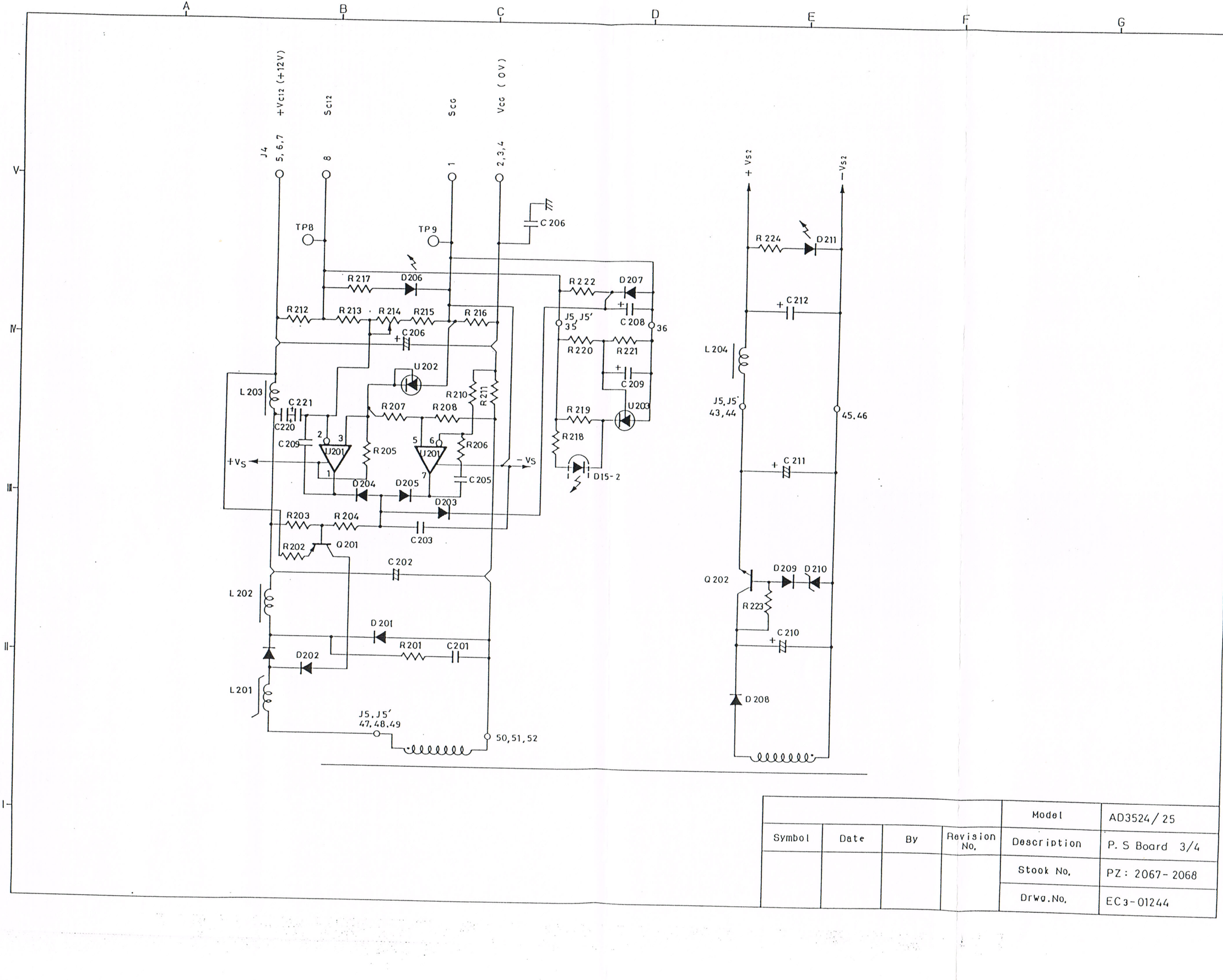


				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P.S Board 1/4
				Stock No.	PZ: 2067 - 2068
				Drwg.No.	EC3 - 01244

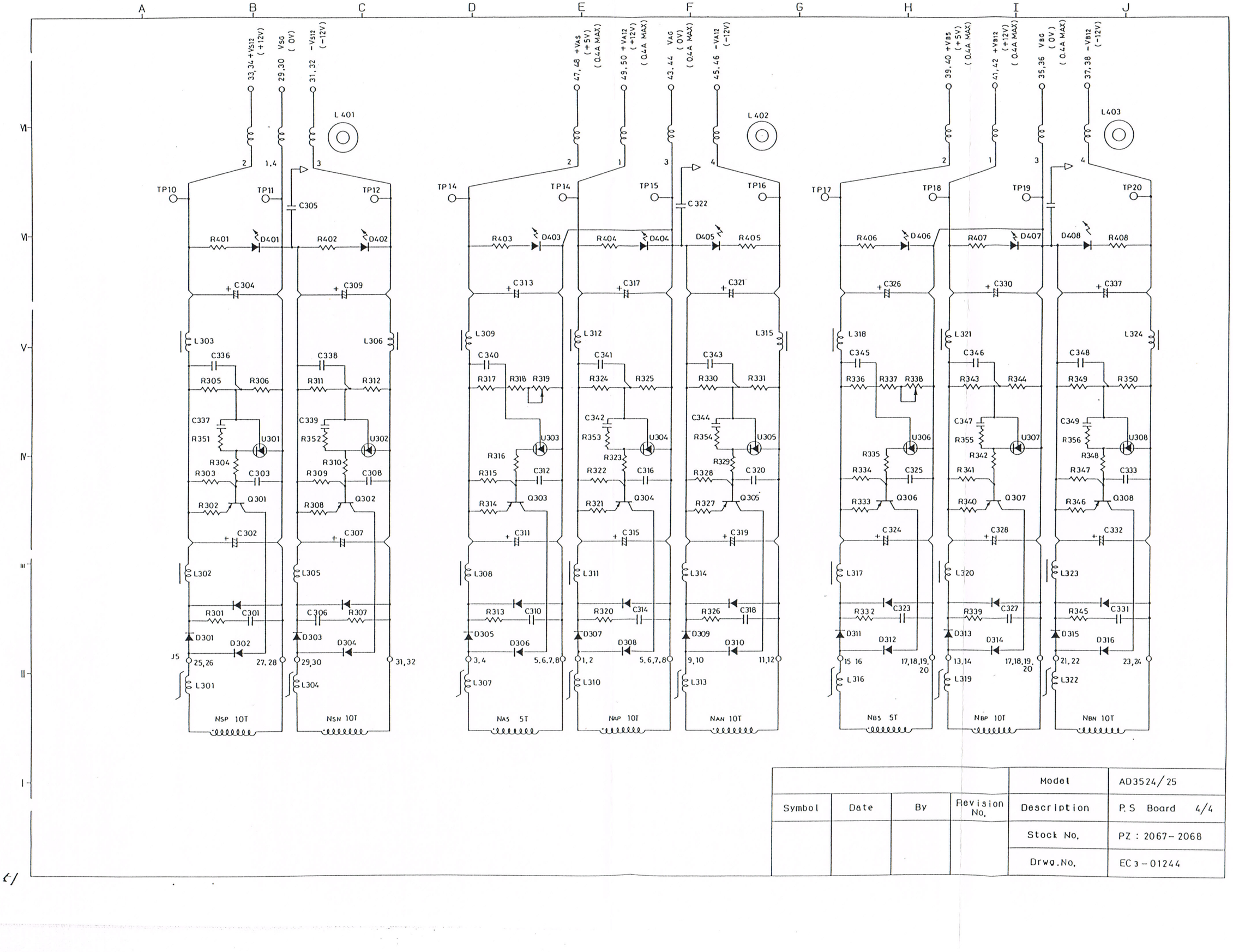


				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P.S Board 2/4
				Stock No.	PZ : 2067-2068
				Drwg.No.	EC3-01244

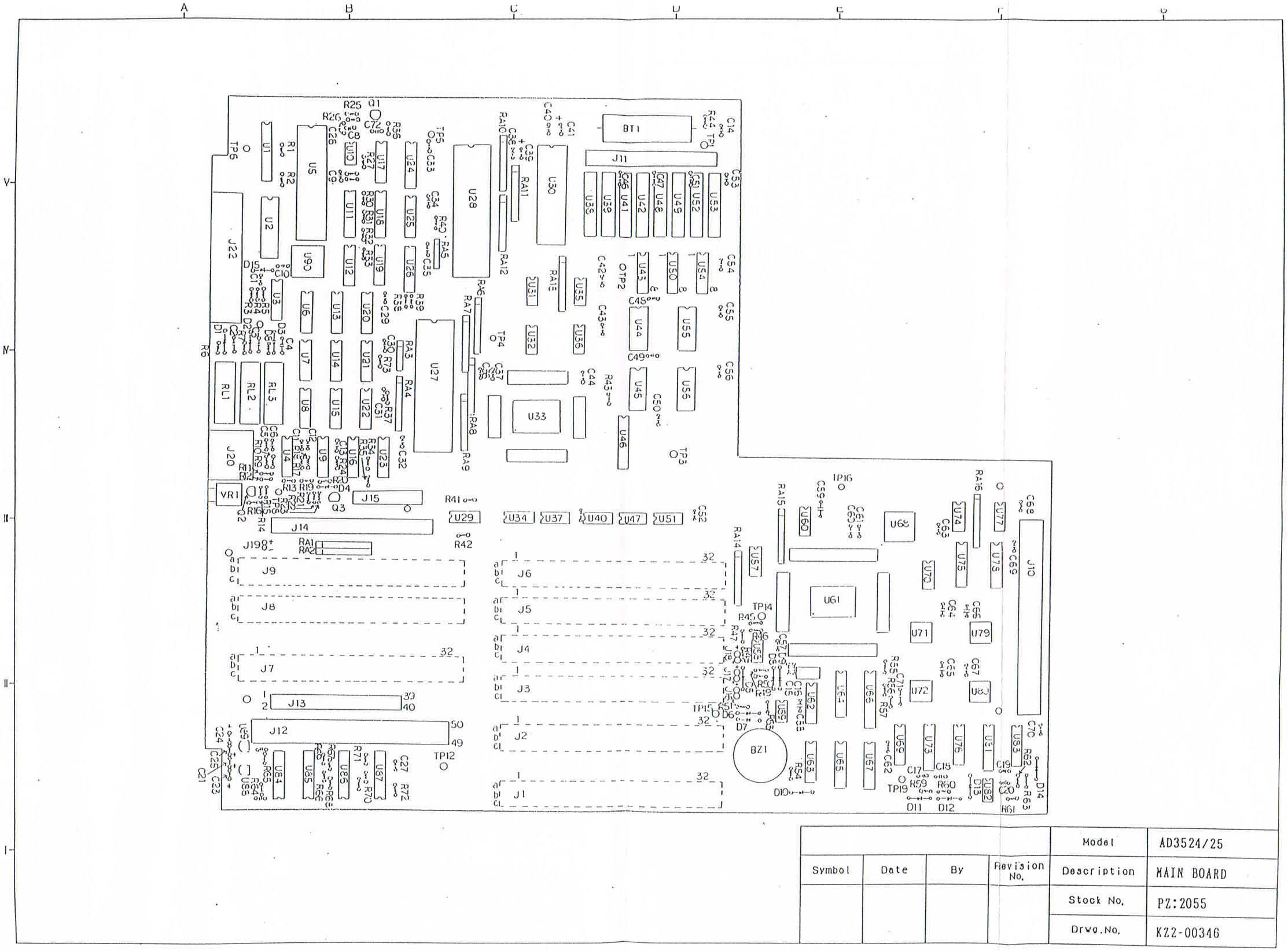
4/



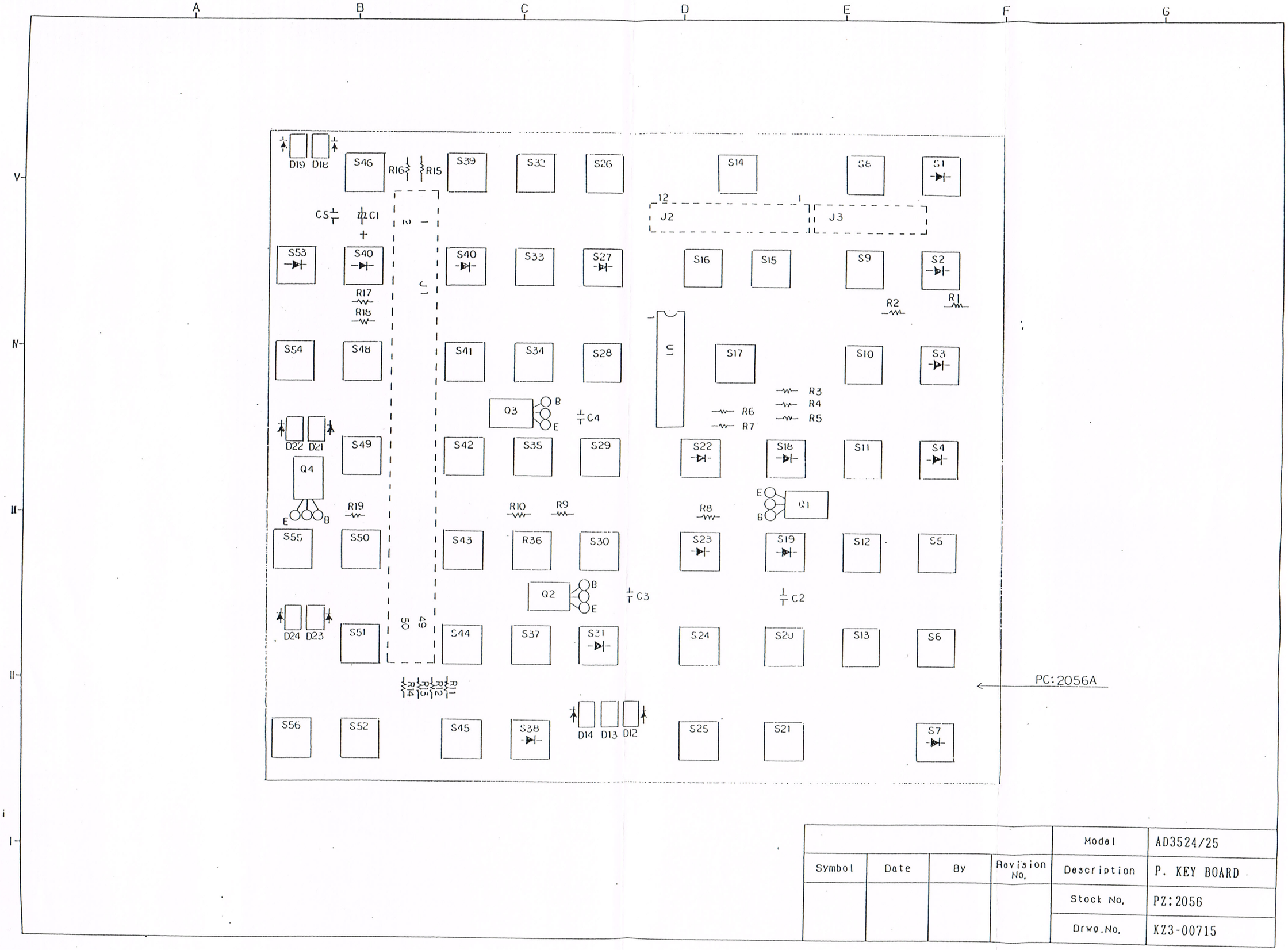
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P. S Board 3/4
				Stock No.	PZ: 2067-2068
				Drwg.No.	EC3-01244



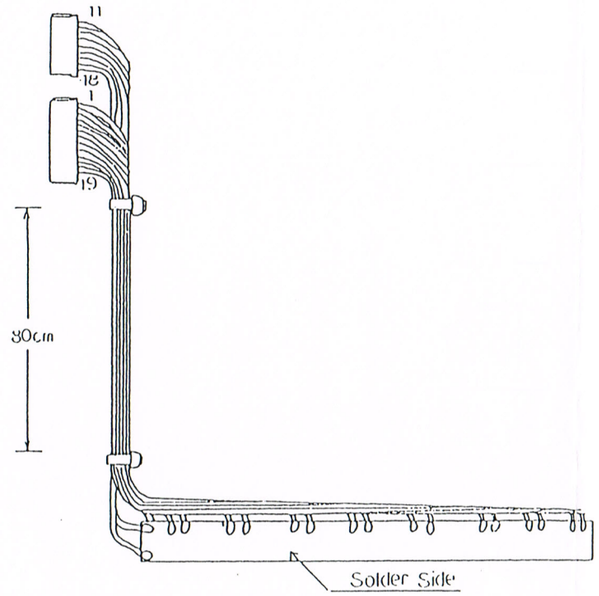
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P.S Board 4/4
				Stock No.	PZ : 2067-2068
				Drwg.No.	EC3-01244

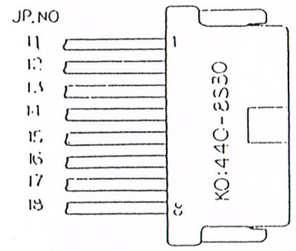


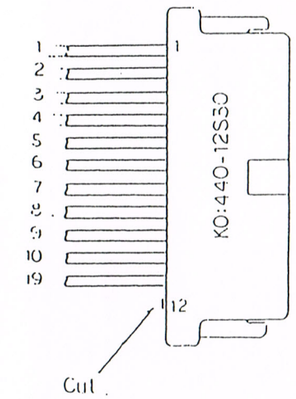
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	MAIN BOARD
				Stock No.	PZ:2055
				Drwo.No.	KZ2-00346

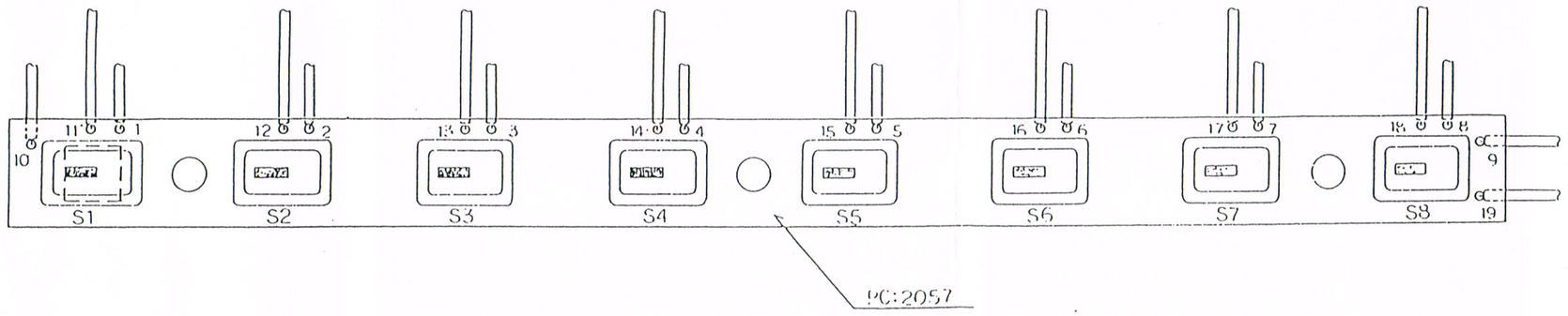


Symbol	Date	By	Revision No.	Model	AD3524/25
				Description	P. KEY BOARD
				Stock No.	PZ:2056
				Drwg.No.	KZ3-00715

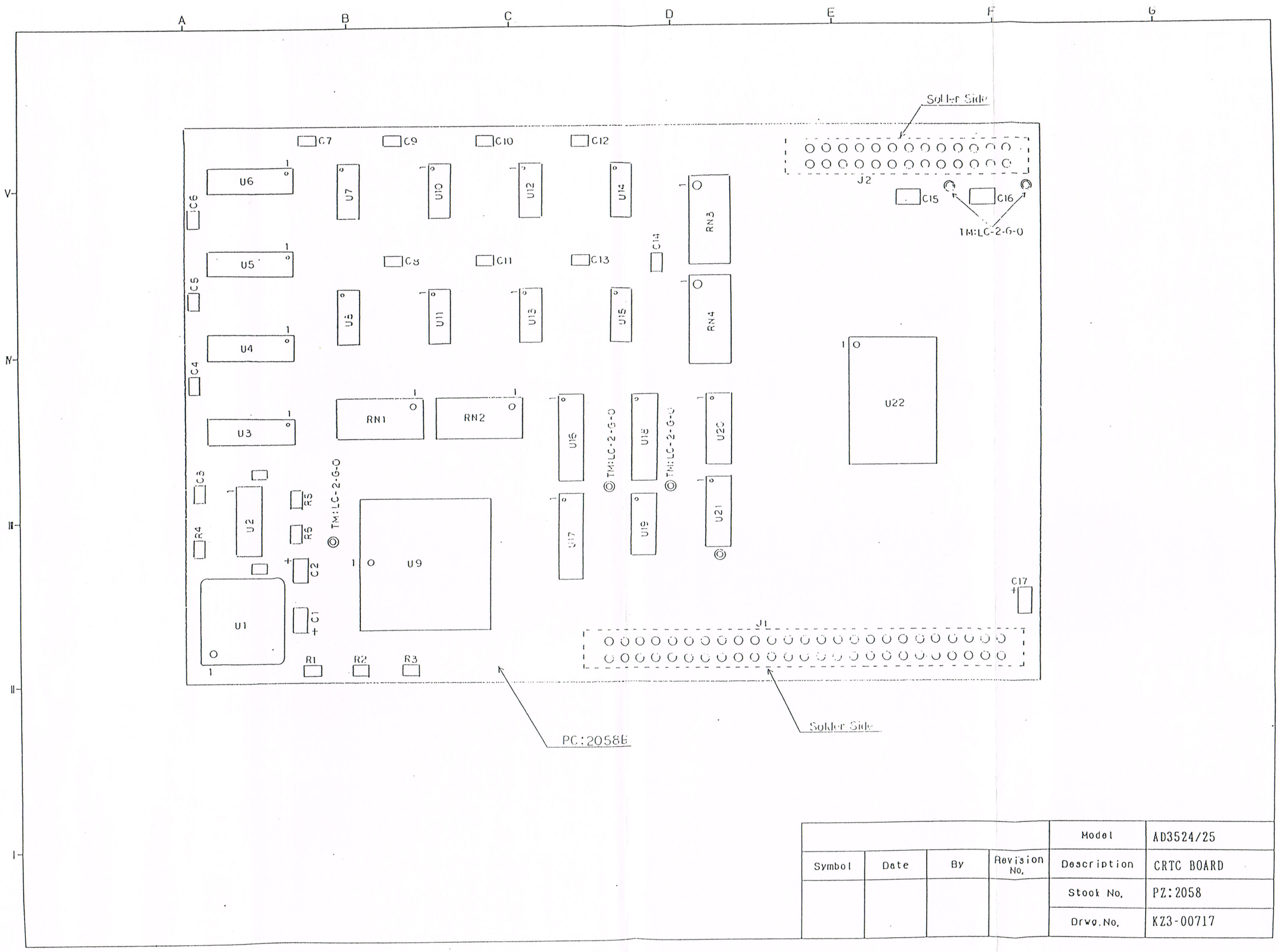




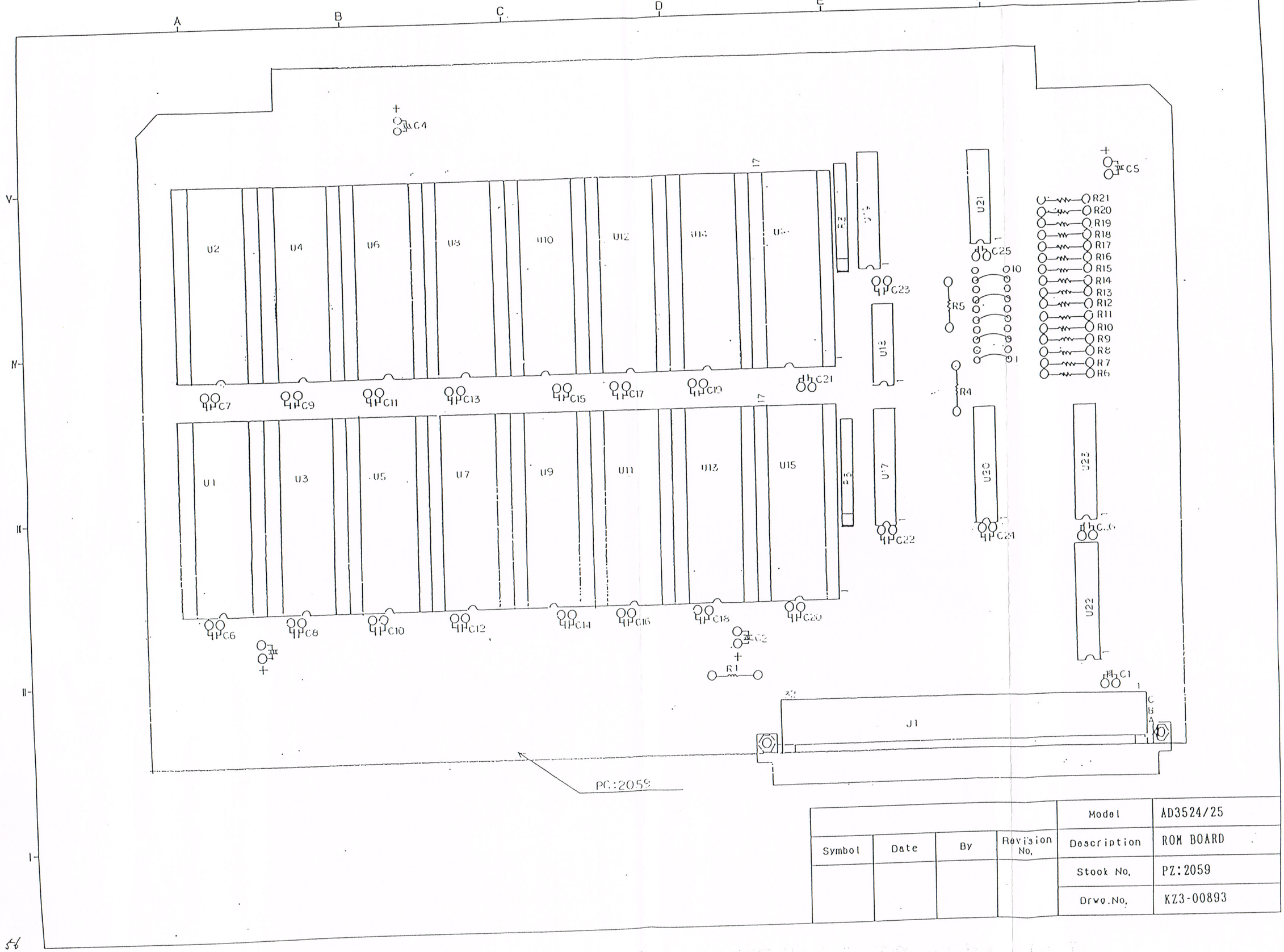




				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	SOFT KEY BOARD
				Stock No.	PZ:2057
				Drwg.No.	KZ3-00716



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	CRTC BOARD
				Stock No.	PZ:2058
				Drwg.No.	KZ3-00717



				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ROM BOARD
				Stock No.	PZ:2059
				Drwg.No.	KZ3-00893

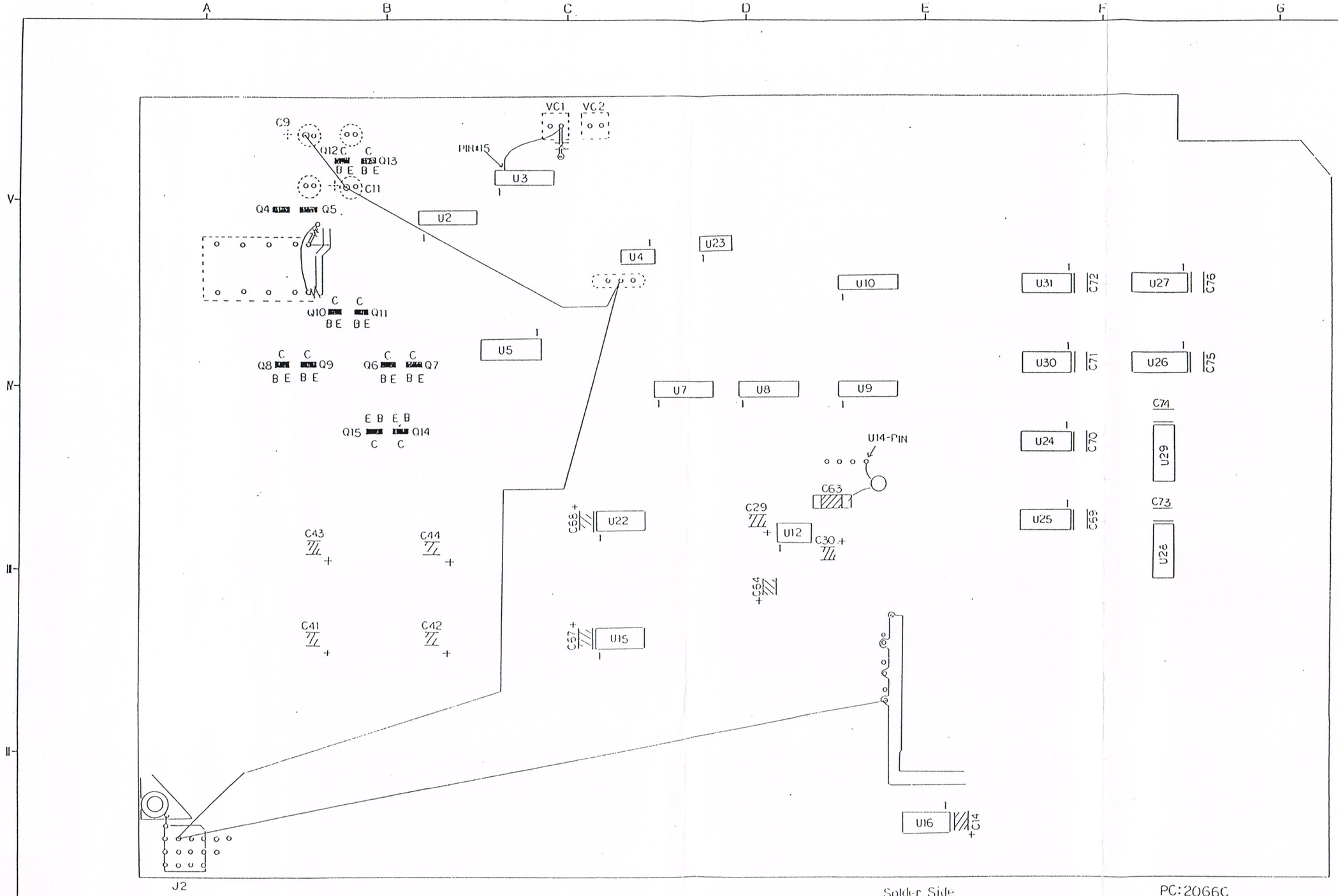
56

Parts Side

PC:2066C

Symbol	Date	By	Revision No.

Model	AD3524/25
Description	ANALOG BOARD 1/2
Stock No.	PZ:2066A/B
Drwg.No.	KZ2-00388

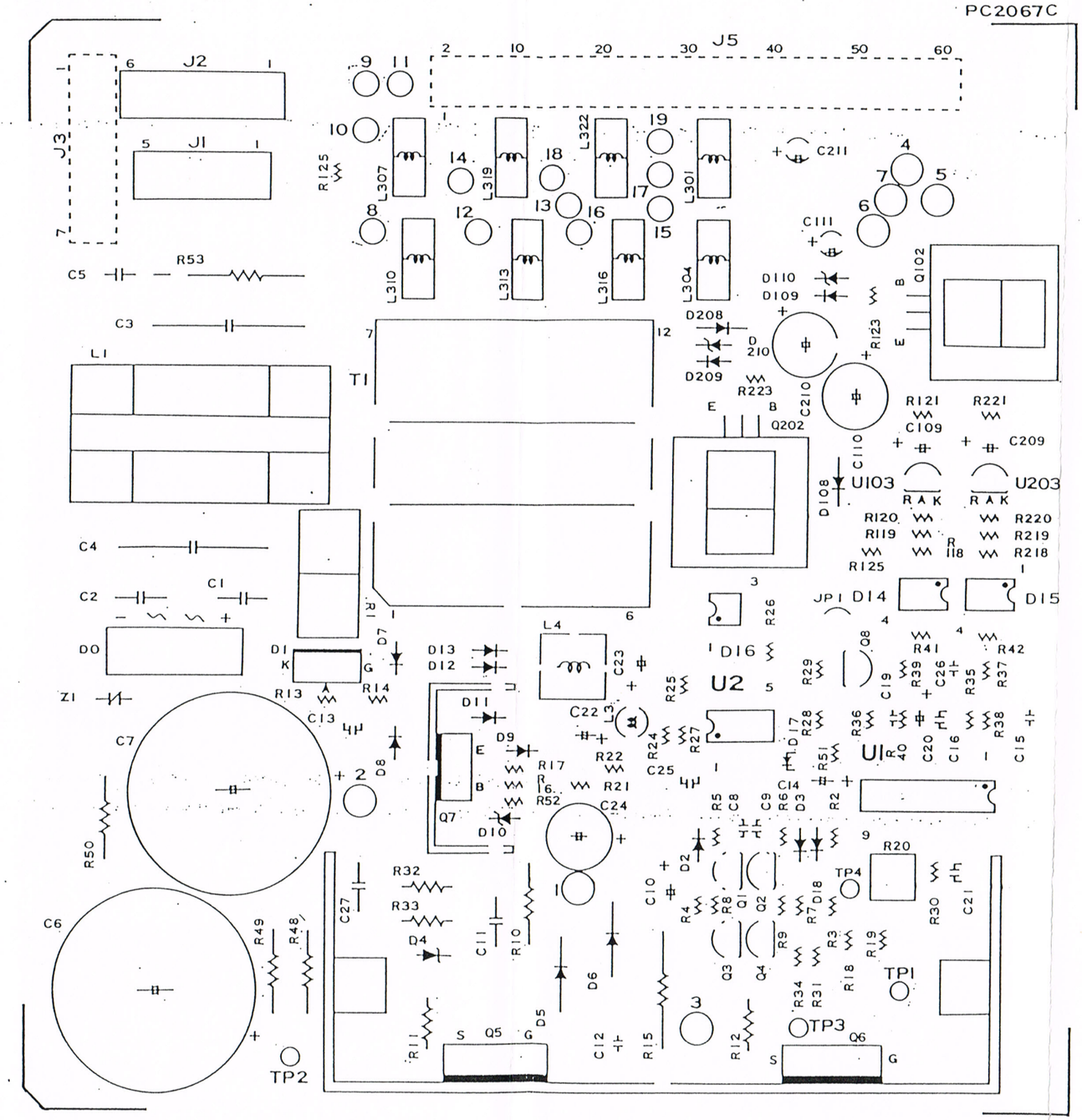


Solder Side

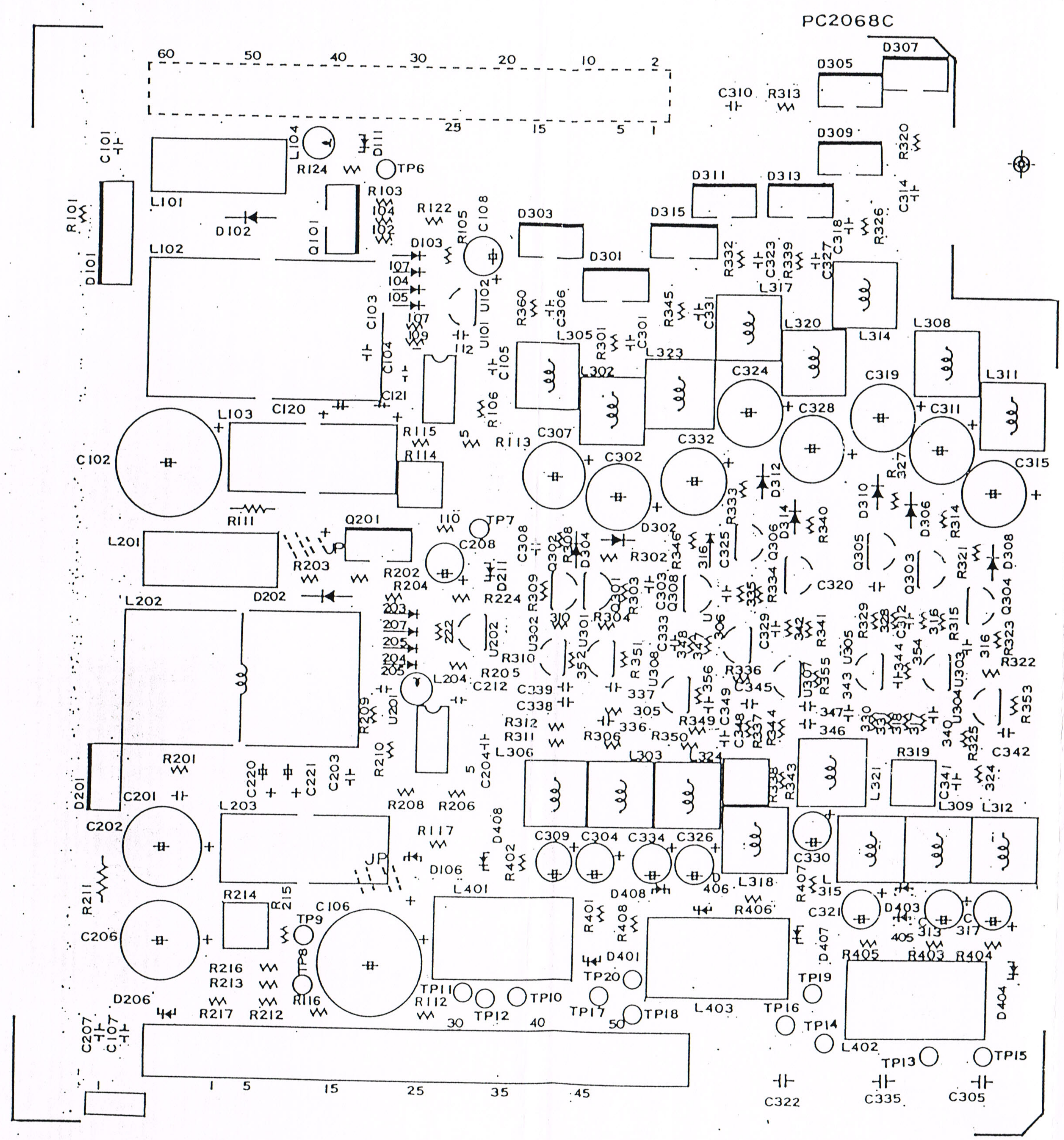
PC:2066C

				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	ANALOG BOARD 2/2
				Stock No.	PZ:2066A/B
				Drwg.No.	KZ2-00388

PC2067C



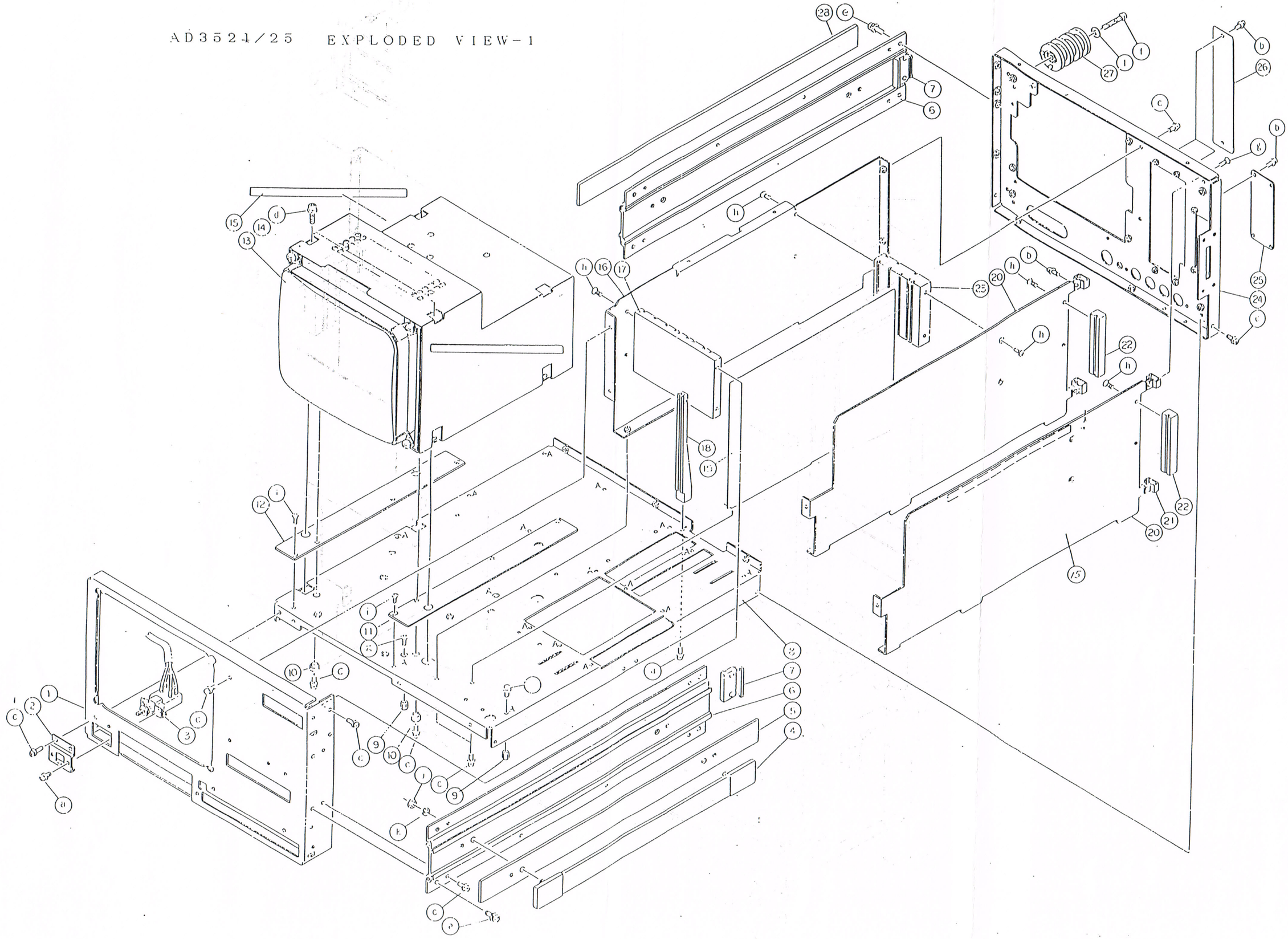
				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P.S BOARD IN
				Stock No.	PZ:2067
				Drwg.No.	KZ2-00348

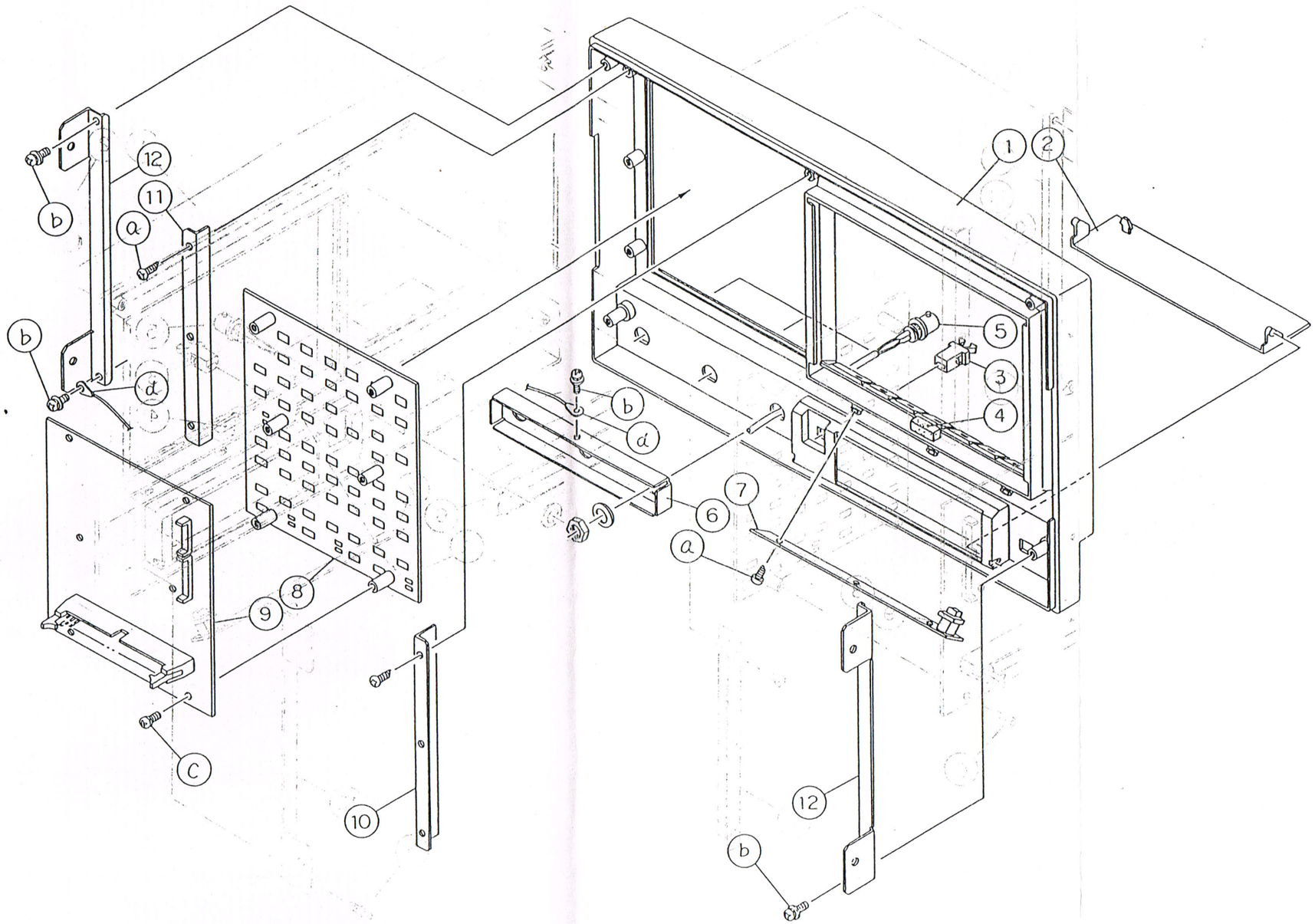


				Model	AD3524/25
Symbol	Date	By	Revision No.	Description	P.S BOARD OUT
				Stook No.	PZ:2068
				Drwg.No.	KZ2-00349

60

AD3524/25 EXPLODED VIEW-1




1
2
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11
12
a
b
c
d

AD3524/25 EXPLODED VIEW-3